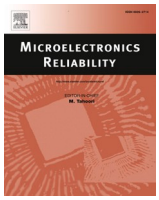
Microelectronics Reliability 178 (2026) 116040

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel



Research paper

A junction-engineered SCR-based ESD protection device for radio-frequency and high-speed serial link interface circuits

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ARTICLE INFO

Keywords:
Silicon-controlled rectifier (SCR)
Electrostatic discharge (ESD)
ESD implantation

ABSTRACT

With the continuous increase in operating frequency of RF integrated circuits (RF ICs) and high-speed serial link (HSSL), optimizing electrostatic discharge (ESD) protection robustness per unit capacitance has become critical. Traditional solutions, such as dual diodes, stacked diodes, and silicon-controlled rectifier (SCR), face limitations including high parasitic capacitance, elevated conduction resistance, and difficulties in maintaining low trigger voltages (V_{t1}) and sufficiently high holding voltages (V_h) above the latch-up threshold. These challenges render them less effective for high-frequency applications.

In this work, a P-type diode integrated with a P-type ESD (P-ESD) implantation layer is first fabricated and characterized. Building upon this, an enhanced diode-triggered SCR (DTSCR) incorporating the P-ESD implantation layer is proposed and implemented in 28-nm CMOS technology. The proposed DTSCR exhibits improved ESD performance, including reduced V_{t1}, lowered V_h, and enhanced human-body model (HBM) robustness normalized by the product of conduction resistance and parasitic capacitance. These results demonstrate the potential of the DTSCR with P-ESD implantation as a promising solution for parasitic capacitance efficiency and high-robustness ESD protection in RF ICs and HSSL applications.

1. Introduction

The operational frequency and corresponding data rate of radio-frequency integrated circuits (RF ICs) and high-speed serial link (HSSL) systems have continuously increased to meet the demands for higher data transfer rates and low-latency communication [1–3]. To support these requirements, advanced CMOS technologies have been employed to enable higher transconductance (g_m), improved cut-off frequency (f_t), and increased device integration for enhanced digital functionality in high-frequency applications [4–6]. However, although performance has benefited from technology scaling, critical reliability concerns such as electrostatic discharge (ESD) have not scaled accordingly. To comply with industrial standards, a minimum component-level ESD robustness of 0.5 kV to 2 kV under the human-body model (HBM) must be ensured [7]. Unfortunately, as CMOS technology has continued to scale, thinner gate oxides and lower breakdown voltages have made devices more vulnerable to ESD-induced damage [8].

In conventional RF and HSSL front-end designs, ESD protection has typically been achieved using dual diodes in conjunction with a power-rail ESD clamp circuit, as illustrated in Fig. 1(a) [9–11]. Although effective in enhancing ESD robustness, this approach requires larger device dimensions to reduce conduction resistance, which in turn increases parasitic capacitance and degrades signal integrity in high frequencies. To alleviate the parasitic loading, stack diode configurations have been introduced, as shown in Fig. 1(b), by placing two diodes in series to reduce total junction capacitance [12,13]. However, this method leads to increased conduction resistance and elevated clamping voltage, potentially exposing internal circuits to higher ESD stress.

In addition to diode-based protection, the silicon-controlled rectifier (SCR) is widely employed as the ESD protection device, which offers exceptional ESD robustness with minimal parasitic capacitance [14–19]. The SCR operational region under an ESD event is illustrated in Fig. 2, where the operation voltage is constrained by two critical limitations, the lower limit defined by V_{DD}, the bias voltage of the internal circuit, to minimize the latch-up risk, and the upper limit determined by the gate oxide breakdown voltage (V_{BD}), beyond which the excessive ESD voltage stress may lead to permanent gate oxide damage of the internal circuitry [20].

In this study, a P+/N-well diode (PDIO) incorporating a P-type ESD (P-ESD) implantation layer was first fabricated and characterized. The P-

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https://doi.org/10.1016/j.microrel.2026.116040
Received 3 September 2025; Received in revised form 24 January 2026; Accepted 30 January 2026
Available online 7 February 2026