Cost-Efficient Bidirectional ESD Protection for 650-V GaN Power HEMT With Co-Packaged Transient Voltage Suppressor

Chieh-Chen Ker, *Graduate Student Member, IEEE*, Chun-Yu Lin, *Senior Member, IEEE*, Ming-Dou Ker, *Fellow, IEEE*, Tsung-Yin Chiang, Chun-Chi Wang, and Ryan Jiang

***Abstract*—A cost-efficient electrostatic discharge (ESD) protection solution for the gate-to-source terminal of GaN-based power high-electron-mobility transistors (HEMTs) is proposed. High ESD robustness of the GaN-based power HEMT has been successfully achieved by co-packaging a transient voltage suppressor (TVS) inside the package together, while a 32.6% reduction in cost as comparing to that with on-die bidirectional ESD protection circuit can be gained. Human-body-model (HBM) ESD level exceeding ±7 kV has been verified, indicating the effectiveness of the proposed solution for protecting the gate-to-source terminal of GaN-based power HEMT.**

***Index Terms*—Electrostatic discharge (ESD), GaN-on-Si process, high-electron-mobility transistor (HEMT), human body model (HBM), human metal model (HMM), transient voltage suppressor (TVS).**

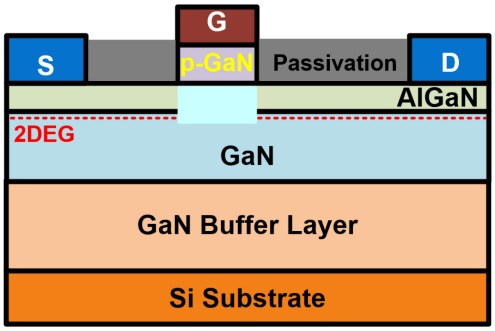

Fig. 1. The device structure of a p-GaN gate enhancement mode (E-mode) HEMT.

I. Introduction

GAN-BASED power high-electron-mobility transistors (HEMTs) have garnered considerable attentions in high-frequency and high-power-density electronic systems owing to their high electric breakdown field, high electron saturation velocity, and high carrier mobility provided by the two-dimensional electron gas (2DEG) channel [1]. The device structure of a p-GaN gate enhancement-mode (E-mode) HEMT is illustrated in Fig. 1. By incorporating a p-type GaN layer between the AlGaN barrier and the gate electrode, normally-OFF operation can be achieved, which is a highly desirable characteristic for power switching applications.

However, electrostatic discharge (ESD) remains a primary reliability concern, because ESD events can induce severe damage to GaN-based power HEMTs. In particular, the gate terminal is highly susceptible to ESD failures. Due to the presence of back-to-back diodes in the gate structure, which cannot effectively dissipate electrostatic charges, the gate is often damaged under ESD stress [2], [3], [4]. Significant damage has been observed under ESD stress as the failure analysis pictures illustrated in Fig. 2. The image of failure hot spot by backside OBIRCH is shown in Fig. 2 (a), and the corresponding sectional view on the damaged location by SEM is shown in Fig. 2(b), where the standalone GaN power HEMT was tested by a positive gate-to-source (+GS mode) HBM ESD stress of 350V. Therefore, improving the ESD robustness of GaN-based power HEMT, especially at the gate terminal, is essential for ensuring device reliability for safe applications.

To fully turn off the GaN-based power HEMT in the field applications, the gate voltage is often biased to the negative voltage level around –5 ∼ –10V. Therefore, the gate-to-source ESD protection solution must be designed with a bidirectional structure. Several on-die bidirectional gate-to-source ESD protection solutions to enhance ESD robustness of GaN-based power HEMT were reported [5], [6], [7]. In Fig. 3(a), the ESD protection circuit consists of two ESD protection HEMTs ($HEMT_{ESD1}$ and $HEMT_{ESD2}$) along with two resistors (R_1 and R_2). During an ESD event, the parasitic capacitances between the gate to drain (C_{GD}, C_{GD1}, and C_{GD2}) and the gate to source (C_{GS}, C_{GS1}, and C_{GS2}) enable voltage coupling from the gates of $HEMT_{ESD1}$, $HEMT_{ESD2}$, and the protected HEMT. This coupled voltage, in conjunction with the series resistor (R_1 or R_2), generates a transient response governed by the RC time constant. As a result, the gate voltage of $HEMT_{ESD1}$ and $HEMT_{ESD2}$ increases momentarily, activating their channels to provide a temporary turn-on path to discharge ESD current [5].

Received 23 October 2025; revised 1 December 2025; accepted 2 December 2025. Date of publication 5 December 2025; date of current version 20 March 2026. This work was supported in part by the National Science and Technology Council (NSTC), Taiwan, under Contract NSTC 112-2221-E-A49-147-MY3 and Contract 110-2622-8-009-017-TP1. *(Corresponding authors: Chun-Yu Lin; Ming-Dou Ker.)*

Chieh-Chen Ker, Chun-Yu Lin, and Ming-Dou Ker are with the Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu 300, Taiwan (e-mail: cy.lin@ieee.org; mdker@ieee.org).

Tsung-Yin Chiang and Chun-Chi Wang are with the Department of Analog and Memory Circuit Design, Elan Microelectronics Corporation, Hsinchu 300, Taiwan.

Ryan Jiang is with Amazing Microelectronic Corporation, Hsinchu 300, Taiwan.

Digital Object Identifier 10.1109/TDMR.2025.3640734

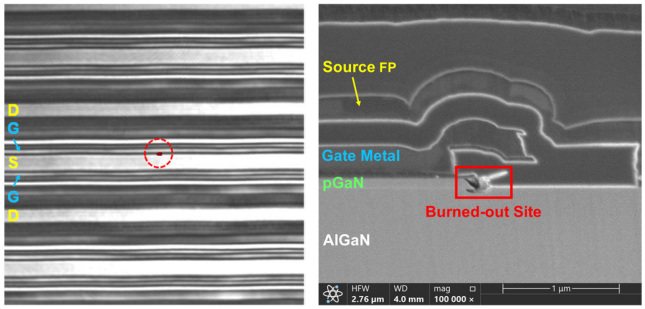

Fig. 2. The images of failure analysis by (a) backside OBIRCH and (b) SEM on the standalone GaN after +GS mode HBM testing.

In Fig. 3(b), the ESD protection circuit is implemented by using eight diode-connected HEMTs (D_1∼D_8), two resistors (R_1 and R_2), and a dual-gate HEMT (DG-HEMT). The operation of the circuit is controlled by two distinct triggering mechanisms: the forward trigger circuit and the reverse trigger circuit, which independently control the two gates of the DG-HEMT. The forward trigger circuit is composed of four diode-connected HEMTs (D_1∼D_4) and a resistor (R_1), while the reverse trigger circuit consists of the remaining four diode-connected HEMTs (D_5∼D_8) and a resistor (R_2). During a forward gate-to-source ESD event, a large transient voltage turns on D_1∼D_4, allowing current to flow through R_1. This current flow induces a voltage increase across G_1 and S_1, thereby activating the gate G_1. Simultaneously, since D_5∼D_8 remain in off state, the voltage difference between G_2 and S_2 remains minimal. Consequently, the upper HEMT within the DG-HEMT functions as a forward-biased diode in series with a resistor, effectively providing a turn-on path to discharge ESD current. The reverse ESD event can be discharged in the same manner [6]. Another structure employs a multi-gate HEMT with a dedicated detection circuit, which can also dissipate the ESD current without causing damage to the GaN-based power HEMT [7].

On the other hand, transient voltage suppressors (TVS) had been widely adopted in CMOS technology by co-packaging them with ICs to mitigate ESD issues [8]. In this work, a cost-effective ESD protection solution is proposed, wherein a TVS is co-packaged with a 650-V GaN power HEMT within the same package. This co-packaged configuration not only improves ESD robustness, but also offers a low-cost approach suitable for industrial applications. Furthermore, a detailed investigation on the selection criteria of the series gate resistance and the TVS is presented to ensure optimal compatibility with the 650-V GaN power HEMT. The proposed approach has been experimentally verified to demonstrate the enhanced ESD robustness without introducing any impact on the normal switching performance in a 240-W AC to DC power converter.

II. Test Structure and Measurement Setup

A standalone 650-V GaN power HEMT fabricated in a GaN-on-Si process is illustrated in Fig. 4(a). In contrast, a 650-V GaN power HEMT is co-packaged with a transient voltage suppressor (TVS) connected between the gate and

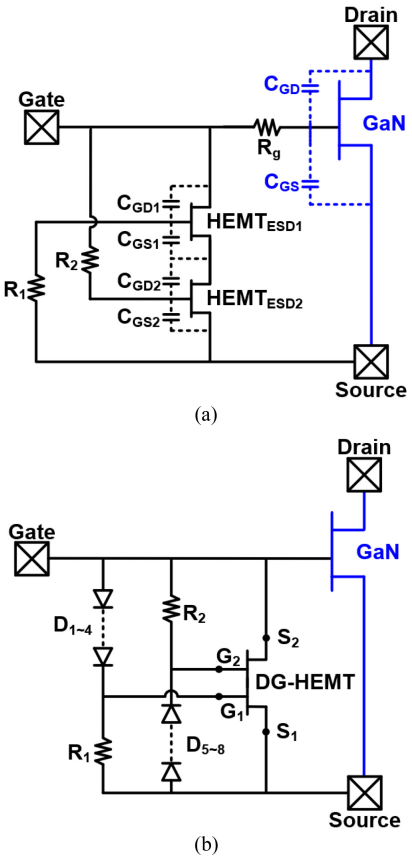

Fig. 3. The schematic diagram of the prior arts with (a) CR-coupling gate-to-source ESD protection circuit [5], and (b) gate-to-source ESD protection circuit with DG-HEMT [6].

source terminals, as shown in Fig. 4(b) and referred as GaN+TVS. The TVS used in this work is the AZ5725-01F [9], which is a bidirectional ESD clamp device capable of responding to both positive and negative gate-to-source voltage transients. The corresponding two-dimensional X-ray image of this co-package GaN+TVS configuration is provided in Fig. 4(c).

To characterize the ESD performance, transmission line pulse (TLP) measurement, human body model (HBM) test, and human metal mode (HMM) test are carried out under two stress conditions, as illustrated in Fig. 5(a) and Fig. 5(b). In the +GS mode, the gate of the 650-V GaN power HEMT is subjected to the positive stress while the source is grounded. Conversely, in the –GS mode, the gate is subjected to the negative stress while the source is grounded. For both test modes, the drain terminal is floating, under the consideration of pin-to-pin ESD stress. The HBM ESD test was performed by the HCE-5000 ESD tester in compliance with the JS-001-2024 standard [10] to evaluate the component-level ESD robustness of the DUTs (devices under test).

The HMM test [11], which is defined to stress the pins of electronic components such as integrated circuits, protection devices, or filters those are directly connected to external system ports and may experience system-level ESD stress waveforms. The HMM ESD test was conducted by using a system-level IEC ESD gun operated in the contact discharge mode [12] to assess the component-level ESD robustness of

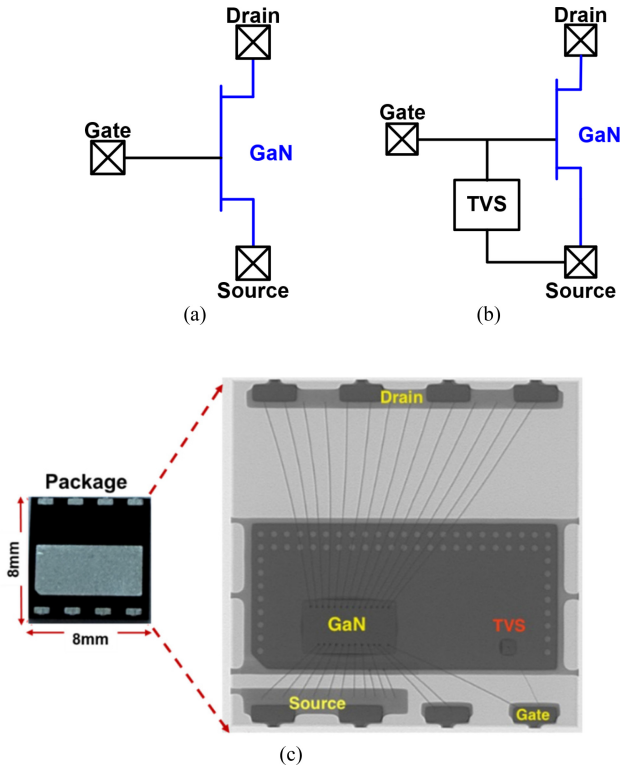

Fig. 4. The schematic diagram of (a) standalone GaN, (b) GaN co-packaged with TVS (GaN+TVS), and (c) 2D X-ray image of the GaN+TVS package.

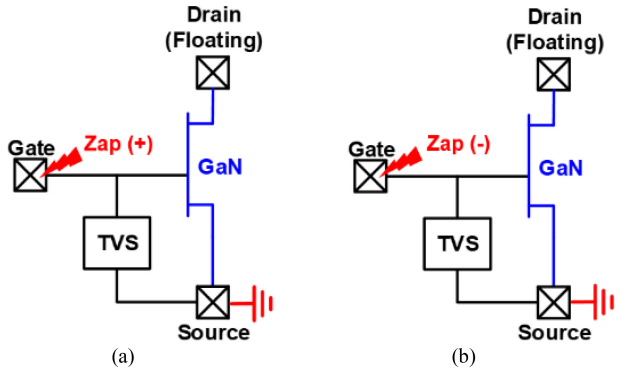

Fig. 5. Two test modes of (a) +GS mode and (b) –GS mode for TLP, HBM, and HMM test.

the DUTs, in accordance with the ANSI/ESD SP5.6-2019 test method [11].

III. Experimental Results

A. Gate-to-Source DC I-V Characteristic

The gate-to-source DC I-V characteristics of the DUTs are shown in Fig. 6. For the standalone 650-V GaN power HEMT, the turn-on voltages (V_{on}) measured at ±10 μA are +5.2 V and –140 V, respectively, as indicated by the black solid line. For the standalone TVS, the corresponding V_{on} values are +7.74 V and –7.88 V, as shown by the blue solid line. For the GaN+TVS configuration, V_{on} is measured to be +5.1 V and –8 V, respectively, as represented by the red dotted line. The positive gate-to-source DC I-V characteristic of GaN+TVS configuration is identical to that of the standalone

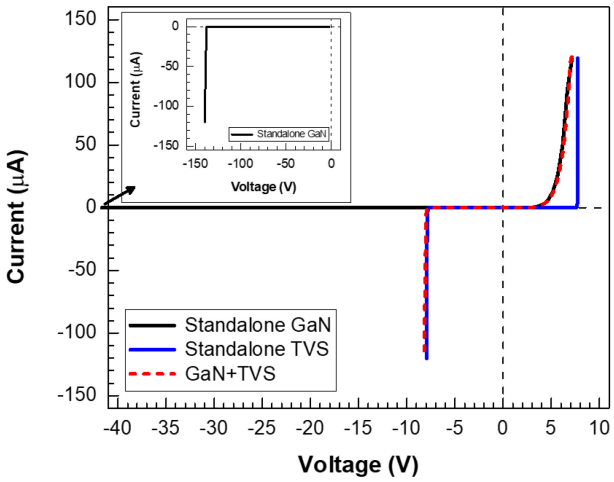

Fig. 6. Gate-to-Source DC I-V characteristics among the test structures of standalone GaN, standalone TVS, and GaN co-packaged with TVS (GaN+TVS).

GaN because the V_{on} of the standalone GaN is lower than that of the standalone TVS in the positive bias region, causing the standalone GaN to dominate conduction. In contrast, under negative bias, the V_{on} of the standalone GaN is much higher than that of the standalone TVS, resulting in the negative DC I-V characteristic of GaN+TVS configuration following the standalone TVS. In practical applications, the gate voltage of a 650-V GaN power HEMT typically ranges from –6 V to 6 V. For the GaN+TVS configuration, the leakage current under positive bias is dominated by the standalone GaN, while under negative bias, the leakage current remains low due to the –8 V V_{on} of the GaN+TVS configuration.

B. ESD Analysis on Standalone GaN

For the standalone GaN, the TLP measurement results under both positive and negative stress modes are shown in Fig. 7(a) and Fig. 7(b), respectively. In the +GS mode, the failure current (I_{t2}) is 39.2 mA. In the –GS mode, I_{t2} is 39.8 mA. The low I_{t2} observed in both modes is attributed to the presence of a back-to-back diode structure between the gate and the two-dimensional electron gas (2DEG) channel in the 650-V GaN power HEMT. In the +GS mode, the reverse Schottky barrier at the gate region inhibits hole injection into the 2DEG channel, resulting in inferior ESD robustness. In the –GS mode, hole accumulation is occurred at the interface between the gate metal and the p-GaN layer, while the heterojunction barrier of AlGaN/GaN prevents electrons injection into the 2DEG channel, also resulting in inferior ESD robustness [13].

The normal gate operating voltage of the 650-V GaN power HEMT is specified as ± 6 V in the field application. When the gate of 650-V GaN power HEMT is damaged by an ESD event, the typical failure mode is a short between the gate and source terminal. Therefore, the gate-to-source DC I-V curve serves as a simple and effective failure criterion to determine whether the gate terminal was damaged, or not. The shift of gate-to-source DC I-V curves after each HBM ESD stress on the standalone GaN under both stress modes is illustrated in Fig. 8(a) and Fig. 8(b), respectively. In Fig. 8(a),

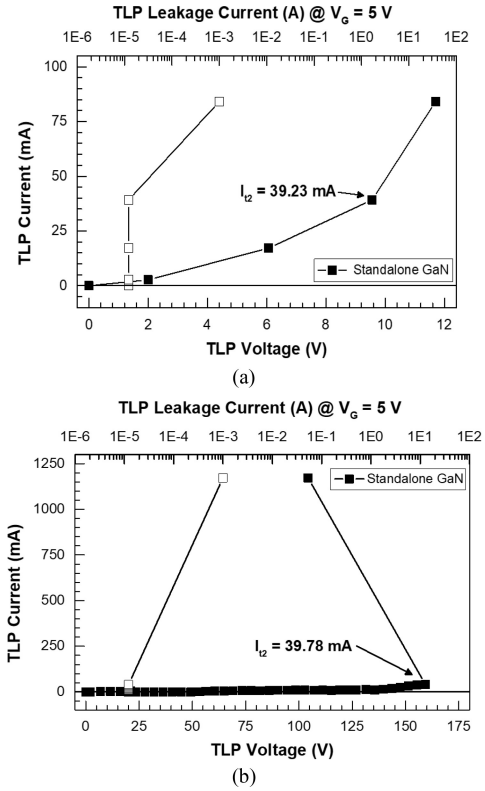

Fig. 7. TLP measurement results for the standalone GaN under (a) +GS mode and (b) –GS mode.

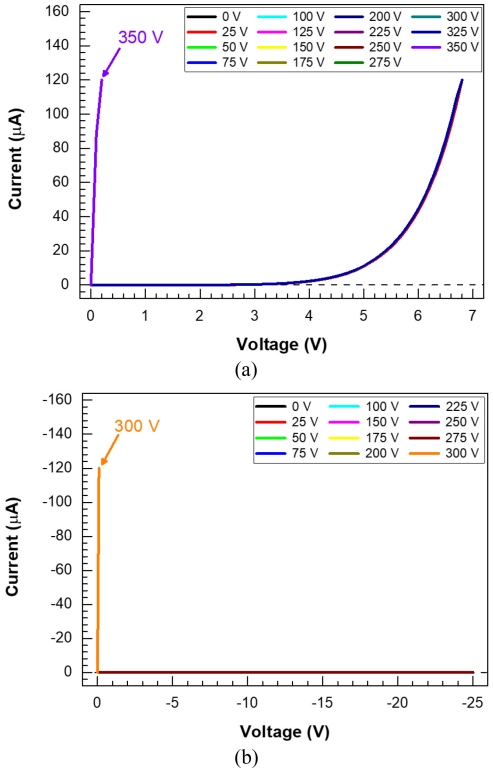

Fig. 8. The shift of gate-to-source DC I-V curves after each ESD voltage stress on the standalone GaN under (a) +GS mode, and (b) –GS mode, HBM test.

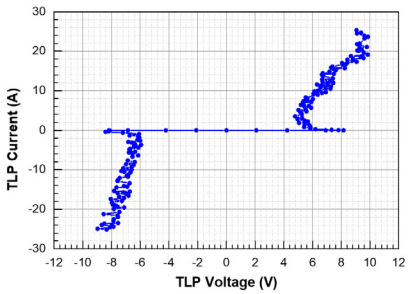

Fig. 9. TLP measurement results of bidirectional I-V curves of the standalone TVS (AZ5725-01F).

a noticeable increase in the gate-to-source leakage current is observed at the 350 V test level, even with low voltage bias. This behavior indicates a low-impedance path formation, suggesting a potential short circuit between the gate and source. Consequently, the HBM level for the standalone GaN under the +GS mode is determined to be 325 V. In contrast, the HBM ESD test result on the standalone GaN under the –GS mode is presented in Fig. 8(b). A similar abrupt rise in gate-to-source leakage current is recorded at the 300 V test level, resulting in an HBM level of 275 V for the –GS mode, even if the standalone GaN is realized in a huge device with dimension (W/L) of 84000 μm/2 μm.

C. ESD Analysis on Standalone TVS and GaN+TVS

The TLP measurement results for the standalone TVS are shown in Fig. 9, where the trigger voltages (V_{t1}, extracted at 100 mA) are 8.1 V and –8.2 V, respectively. Both values exceed the normal gate voltage operating range (–6 V to 6 V), indicating that the use of this TVS prevents false triggering during normal operation of the 650-V GaN power HEMT. The TLP measurement results for the GaN+TVS configuration under both stress modes are presented in Fig. 10(a) and Fig. 10(b). In the +GS mode, the I_{t2} and V_{t1} are 8.35 A and 7.98 V, respectively. In the –GS mode, the I_{t2} exceeds 26.33 A, while the V_{t1} is 8.17 V. These results clearly demonstrate that the GaN+TVS configuration achieves a significant enhancement in ESD robustness compared with the standalone GaN.

Since the dimension of the standalone TVS is only 1 mm × 0.6 mm × 0.45 mm [9], the TLP measurement of the standalone TVS was conducted by welding it on a test board. In contrast, the TLP measurement of the GaN + TVS configuration was conducted by placing the co-packaged GaN + TVS in the testing socket. The difference in the parasitic resistance of the testing path accounts for the slight variation on the TLP-measured curves between Fig. 9 and Fig. 10.

The shift in the gate-to-source DC I-V curves after each HBM ESD stress for the GaN+TVS configuration under both stress modes is illustrated in Fig. 11(a) and Fig. 11(b), respectively. Compared with the standalone GaN, the GaN+TVS configuration demonstrated a significantly improved HBM robustness. In the +GS mode, the HBM level is enhanced to 7 kV, while in the –GS mode, the HBM level exceeds 8 kV.

The shift in the gate-to-source DC I-V curves with logarithmic current scale after each HMM stress for the GaN+TVS configuration is illustrated in Fig. 12(a) and Fig. 12(b). In the +GS mode, a significant increase in gate-to-source leakage

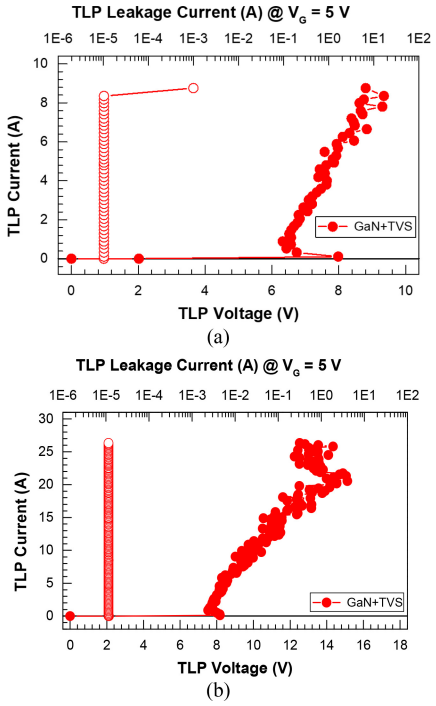

Fig. 10. TLP measurement results of the GaN+TVS configuration under (a) +GS mode and (b) –GS mode.

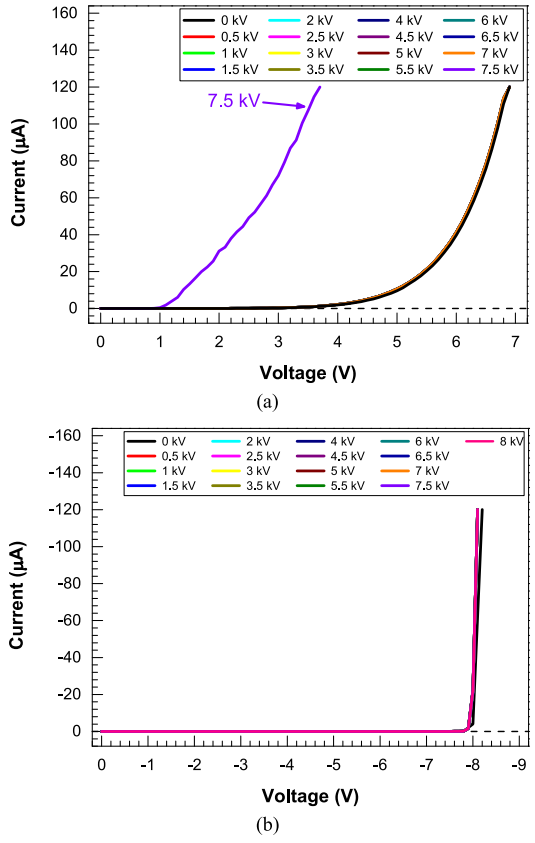

Fig. 11. The shift of gate-to-source DC I-V curves after each ESD voltage stress on the GaN+TVS configuration under (a) +GS mode, and (b) –GS mode, HBM test.

current is observed at the 1.5 kV test level, even under a small voltage bias. This behavior confirms the formation of a low-impedance path, indicating a potential short between

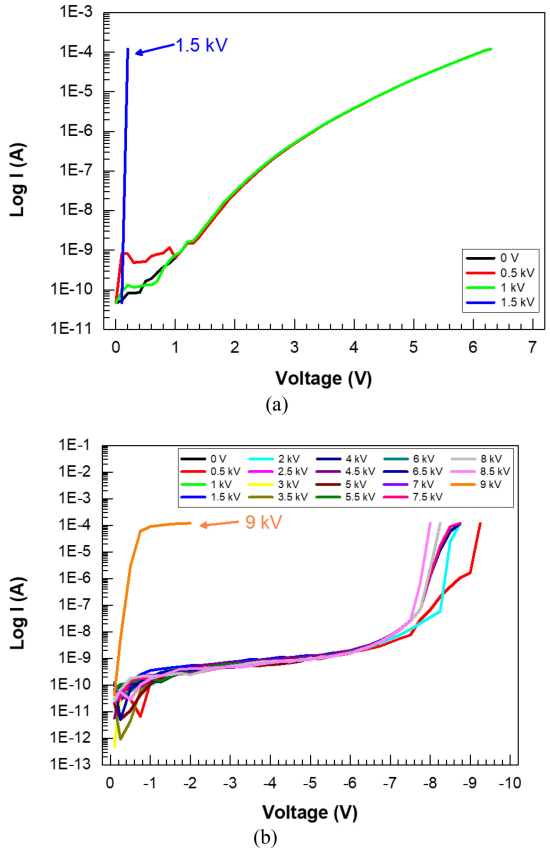

Fig. 12. The shift of gate-to-source DC I-V curves with logarithmic current scale after each ESD voltage stress on the GaN+TVS configuration under (a) +GS mode and (b) –GS mode, HMM test.

the gate and source. Consequently, the HMM level for the GaN+TVS configuration in the +GS mode is determined to be 1 kV. Similarly, in the –GS mode, the HMM level for the GaN+TVS configuration is determined to be 8.5 kV.

As shown in Table I, the standalone GaN exhibited an HBM level of no more than 325 V in both test modes, indicating the gate of 650-V GaN power HEMT is very sensitive to ESD stress. With the implementation of the proposed co-packaged GaN+TVS solution, the HBM level is significantly improved to a passing level of 7 kV in both test modes. In addition, the HMM level of 1 kV for the +GS mode and 8.5 kV for the –GS mode can be gained.

IV. Comparison

A. Comparison With On-Die Solution

Table II summarizes the key indices of the proposed co-packaged GaN+TVS solution in comparison with an on-die bidirectional ESD protection circuit [14], referred to as the on-die solution. Test results are performed with all DUTs placed in the same socket to ensure identical testing conditions. The schematic of the 650-V GaN power HEMT with on-die bidirectional ESD protection circuit is shown in Fig. 13(a), and its corresponding chip photo is presented in Fig. 13(b). As observed in Fig. 13(b), the integration of the bidirectional ESD protection circuit increases the overall chip layout area, which in turn may lead to higher manufacturing costs. The TLP measurement results for the on-die solution under both

TABLE I
SUMMARY OF TEST RESULTS ON THE PROPOSED SOLUTION

Test Results		Standalone GaN	GaN+TVS
TLP I_{t2} (A)	+GS mode	39.23m	8.35
	-GS mode	39.78m	> 26.33
HBM (kV)	+GS mode	0.325	7
	-GS mode	0.275	> 8
HMM (kV)	+GS mode	< 0.5	1
	-GS mode	< 0.5	8.5

TABLE II
COMPARISON AMONG THE PROPOSED SOLUTION AND THE ON-DIE SOLUTION

Bidirectional ESD Protection Design		Standalone GaN	GaN+TVS (This work)	On-die Bidirectional ESD Protection Circuit
TLP I_{t2} (A)	+GS	39.23m	8.35	6.11
	-GS	39.78m	> 26.33	11.11
HBM (kV)	+GS	0.325	7	> 8
	-GS	0.275	> 8	> 8
HMM (kV)	+GS	< 0.5	1	2.5
	-GS	< 0.5	8.5	5.5
Cost		100 %	105.1 %	137.7%

TABLE III
TEST RESULTS OF FIELD APPLICATION IN A 240-W AC-TO-DC POWER CONVERTER WITH 220-V AC INPUT

With Standalone GaN					
Load	Input Power		Output Power		Eff (%)
	I_{in} (A)	V_{in} (V)	I_o (A)	V_o (V)	
25 %	0.34	220.54	5	12.08	90.97
50 %	0.6	220.40	10	12.08	93.13
75 %	0.89	220.30	15.01	12.08	93.51
100 %	1.18	220.19	20.01	12.08	93.26
With GaN+TVS Configuration					
Load	Input Power		Output Power		Eff (%)
	I_{in} (A)	V_{in} (V)	I_o (A)	V_o (V)	
25 %	0.33	220.35	5	12.08	90.89
50 %	0.6	220.13	10	12.08	93.04
75 %	0.89	220.01	15.01	12.08	93.34
100 %	1.19	219.81	20.01	12.08	93.07

stress modes are shown in Fig. 14(a) and Fig. 14(b). In the +GS mode, the I_{t2} is 6.11 A. In the –GS mode, the I_{t2} is 11.11 A.

A substantial enhancement in ESD robustness is achieved by the proposed co-packaged solution relative to the standalone GaN. In addition, the overall implementation cost is reduced by 32.6%, as compared to that of the on-die solution, while superior ESD performance is maintained except for the +GS mode under HMM test. To further improve ESD levels in the +GS mode, it is suggested that the trigger voltage (V_{t1}) of the TVS should be lowered to enable earlier activation for more effective protection of the 650-V GaN power HEMT. However, careful consideration must be given to the ESD design window, wherein the V_{t1} of the TVS must remain above the maximum normal operating gate voltage to avoid unintended triggering during normal operation of the 650-V GaN power HEMT in field applications.

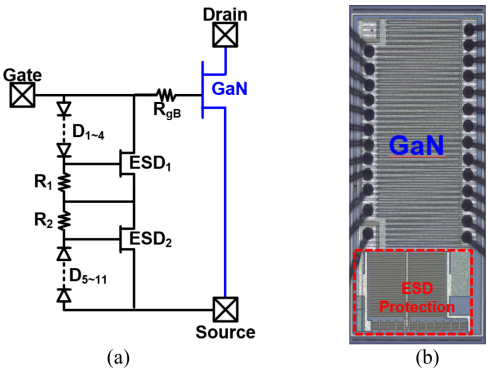

Fig. 13. The (a) schematic, and (b) chip photo, of the 650-V GaN power HEMT with on-die bidirectional ESD protection circuit.

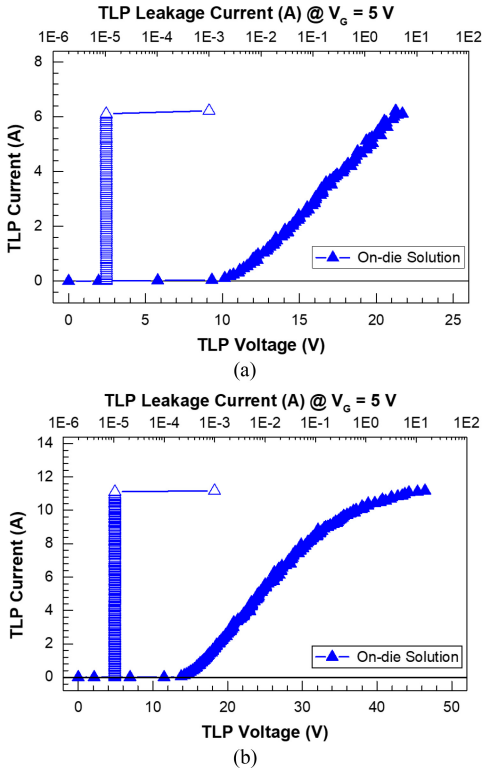

Fig. 14. TLP measurement results of the 650-V GaN power HEMT with on-die bidirectional ESD protection circuit under (a) +GS mode and (b) –GS mode.

B. Field Application

The proposed GaN+TVS configuration has been implemented in a 240-W AC-to-DC power converter (AC input: 110 V/220 V, DC output: 12 V). The block diagram of the 240-W AC to DC power converter is illustrated in Fig. 15, which incorporates a power factor correction (PFC) and an inductor-inductor-capacitor (LLC) resonant converter stage, as the application circuit diagram provided in the datasheet of TEA2017AAT/2 [15]. The gate driver is a digital configurable LLC and multimode PFC controller. The test results of power conversion efficiencies in the 240-W AC-to-DC power converter realized with the standalone GaN and the GaN+TVS configuration are summarized in Table III. The conversion

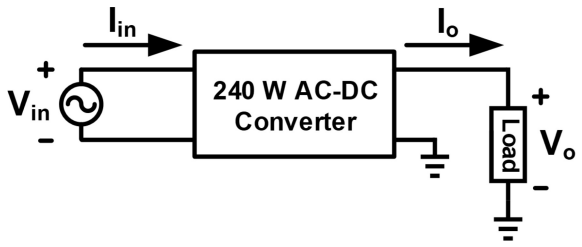

Fig. 15. Block diagram of the 240-W AC-to-DC power converter.

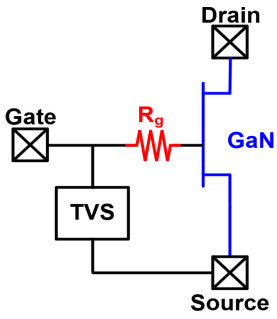

Fig. 16. The schematic of the added R_g to the GaN+TVS configuration.

efficiency is defined as

$$\text{Eff}(\%) = P_o/P_{in} \quad (1)$$

P_o is the output power and P_{in} is the input power, given by

$$P_o = V_o \times I_o \quad (2)$$

$$P_{in} = V_{in,rms} \times I_{in,rms} \times (\text{Power Factor for PFC}). \quad (3)$$

Here V_{in} and I_{in} denote the AC input voltage and current, while V_o and I_o represent the DC output voltage and current, as illustrated in Fig. 15.

As shown in Table III, the conversion efficiencies of the 240-W AC-to-DC power converter realized with the standalone GaN and the GaN+TVS configuration are nearly identical across different load conditions. These results indicate that the GaN+TVS configuration achieves excellent ESD robustness while preserving the high conversion efficiency advantage in field applications.

V. Optimization on Co-Packaged TVS With Series Gate Resistor

To further improve the HMM level in the +GS mode, the concept of system-efficient ESD design (SEED) [16] can be applied. In selecting the TVS device, both the normal gate operating voltage and the failure voltage V_{t2} of the standalone GaN must be considered. For effective protection, the TVS should be activated before the GaN device reaches breakdown. Thus, the trigger voltage V_{t1} of TVS should be as low as possible. However, the V_{t1} of TVS must remain above the normal gate operating voltage to prevent false triggering during normal operation. Under such conditions, the addition of a series gate resistor R_g is necessary, as illustrated in Fig. 16. Therefore, the following condition must be satisfied

$$\text{Normal operating voltage} < V_{t1,TVS} < \left(V_{t2,GaN} + I_{t2,GaN} \times R_g\right) \quad (4)$$

To determine the appropriate value of the series gate resistor R_g, the TLP characteristics of the standalone GaN must first be analyzed. As shown in Fig. 7(a), the +GS mode TLP curve exhibits no distinct V_{t1} and rapidly reaches the V_{t2}. In Fig. 16, R_g is placed between the TVS and the gate terminal of the 650-V GaN power HEMT device. This configuration increases the effective failure voltage ($V'_{t2,GaN}$) of the GaN device, expressed as

$$V'_{t2,GaN} = V_{t2,GaN} + \left(I_{t2,GaN} \times R_g\right) \quad (5)$$

For a given TVS, increasing failure voltage is equivalent to lowering the relative trigger voltage $V_{t1,TVS}$, enabling earlier activation of the TVS to protect the GaN device and thereby achieving a higher ESD level.

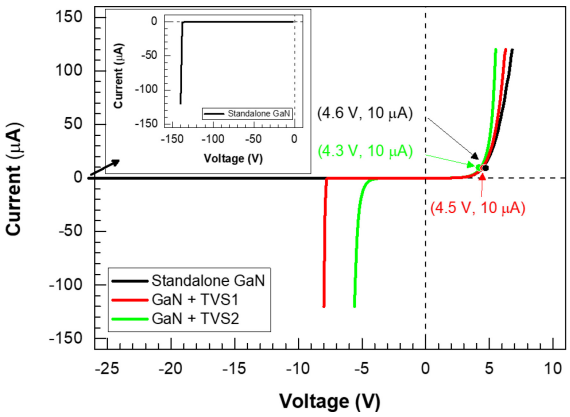

Fig. 17. The gate-to-source DC I-V characteristics among the test configurations under R_g of 0 Ω with TVS1 and TVS2.

An experiment is conducted to verify the proposed theory. The GaN device is realized with a larger dimension of W/L = 168000 μm / 2 μm. The TVS that used in Table II is here referred as TVS1. An alternative TVS with a lower V_{t1} of 6.8 V, referred as TVS2 [17], is employed. The gate-to-source DC I-V characteristics among the test configurations under R_g of 0 Ω with TVS1 and TVS2 are shown in Fig. 17.

As shown in Fig. 17, the turn-on voltage (V_{on}) measured at +10 μA of the standalone GaN device is 4.6 V, as indicated by the black line. The V_{on} value of the GaN+TVS1 and GaN+TVS2 are nearly identical to that of the standalone GaN, indicating that under positive bias conditions, the gate-to-source DC I-V characteristics of GaN+TVS1 and GaN+TVS2 follow those of the standalone GaN. In contrast, under negative bias conditions, the gate-to-source DC I-V characteristics of GaN+TVS1 and GaN+TVS2 follow the characteristics of their corresponding TVS.

The series gate resistor R_g is varied from 0 Ω to 50 Ω for the HMM test, and the corresponding results in the +GS mode are shown in Fig. 18. The blue line represents the GaN+TVS1, while the red line represents the GaN+TVS2. The +GS mode HMM level of GaN+TVS configuration with TVS1 or TVS2 can be effectively increased by the series gate resistor R_g. For the same R_g value, the GaN+TVS2 achieves a higher HMM level. This improvement is attributed to the lower V_{t1} of TVS2, which enables faster activation and more effective protection of the GaN device. For a given TVS, increasing the value of

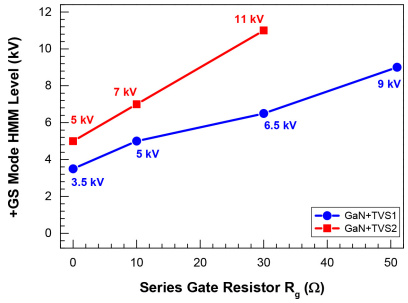

Fig. 18. The test results on +GS mode HMM level of GaN+TVS configuration with TVS1 or TVS2 under different series gate resistor R_g.

R_g results in a higher HMM level. This behavior is reasonable, as a larger R_g increases the effective failure voltage ($V'_{t2,GaN}$) of the GaN device, which is equivalent to lowering the relative $V_{t1,TVS}$, thereby enabling earlier activation of the TVS and enhancing the ESD robustness of the GaN device.

As reported in [5], the relationship between switching speed and the series gate resistance was discussed. It has been shown that no switching delay occurs when the series gate resistance is lower than 5 Ω. Moreover, the gate voltage waveforms, corresponding to series gate resistances of 15 Ω and 30 Ω, overlap with each other and only slightly differ from those obtained with a series gate resistance lower than 5 Ω. Therefore, the series gate resistance used with SEED method on the GaN with co-packaged TVS will be suggested to be below 30 Ω.

The series gate resistor R_g can be implemented in two ways. The first approach is to co-package a chip-style resistor together with the TVS and the GaN device inside a package. The second approach is to further develop a customized TVS die with an additional resistor integrated at the output of the TVS.

VI. Conclusion

A cost-efficient bidirectional gate-to-source ESD protection solution for GaN-based power HEMTs has been successfully verified. By co-packaging a transient voltage suppressor (TVS) between the gate and source terminal within the same package, the gate-to-source HBM ESD level of GaN-based power HEMTs can be significantly improved from 325V to over ±7 kV, while achieving a 32.6% cost reduction as compared to that with on-die bidirectional ESD protection circuit. As verified in the field applications, the power conversion efficiencies in a 240-W AC-to-DC power converter implemented with the standalone GaN and the GaN+TVS configuration are almost the same. These results indicate that the GaN+TVS configuration achieves excellent ESD robustness while preserving the high conversion efficiency advantages in field applications. Furthermore, an optimized analysis on the relationship between different TVS and the series gate resistor R_g has also been conducted. By appropriately selecting the V_{t1} of TVS and the value of R_g, the HMM level of GaN-based power HEMTs can be further enhanced.

Acknowledgment

The authors would like to thank *Materials Analysis Technology Inc.* (MA-tek), Taiwan, for the support of ESD test and failure analysis.

References

[1] K. J. Chen et al., "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017, doi: 10.1109/TED.2017.2657579.

[2] W.-M. Wu et al., "ON-state human body model ESD failure mechanisms in GaN-on-Si RF MIS-HEMTs," *IEEE Electron Device Lett.*, vol. 44, no. 8, pp. 1248–1251, Aug. 2023, doi: 10.1109/LED.2023.3290034.

[3] Z. Wang, J. J. Liou, K.-L. Cho, and H.-C. Chiu, "Development of an electrostatic discharge protection solution in GaN technology," *IEEE Electron Device Lett.*, vol. 34, no. 12, pp. 1491–1493, Dec. 2013, doi: 10.1109/LED.2013.2283865.

[4] C.-Y. Ke, W.-C. Wang, M.-D. Ker, C.-Y. Yang, and E. Y. Chang, "Investigation on ESD robustness of 1200-V D-mode GaN MIS-HEMTs with HBM ESD test and TLP measurement," in *Proc. IEEE Int. VLSI Symp. Technol. Syst. Appl. (VLSI-TSA)*, 2023, pp. 1–2, doi: 10.1109/VLSI-TSA/VLSI-DAT57221.2023.10134426.

[5] J.-H. Lee et al., "The influence of gate-series-resistor on the ESD protection and switching speed for 650V GaNHEMT circuit," in *Proc. IEEE Int. Symp. Phys. Failure Anal. Integr. Circuits (IPFA)*, 2024, pp. 1–6, doi: 10.1109/ IPFA61654.2024.10691316.

[6] Y. Ma et al., "Monolithically integrated bidirectional gate ESD protection scheme of p-GaN power HEMT by dual-gate device technology," *IEEE Trans. Power Electron.*, vol. 40, no. 2, pp. 2721–2725, Feb. 2025, doi: 10.1109/TPEL.2024.3494833.

[7] J. A. Salcedo, S. Parthasarathy, and S. Zhang, "Bidirectional heterojunction compound semiconductor protection devices and methods of forming the same," U.S. Patent 9 184 098, Nov. 2015.

[8] C.-H. Chuang and M.-D. Ker, "System-level ESD protection for automotive electronics by co-design of TVS and CAN transceiver chips," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 3, pp. 570–576, Sep. 2017, doi: 10.1109/TDMR.2017.2737943.

[9] "Datasheet of AZ5725-01F," Amazing Microelectronic Corp., Taipei, Taiwan, 2015.

[10] *Electrostatic Discharge (ESD) Sensitivity Testing—Human Body Model (HBM)—Device Level*, JEDEC/ESDA Joint Standard JS-001-2024, Oct. 2024.

[11] *Electrostatic Discharge Sensitivity Testing—Human Metal Model (HMM)—Component Level*, EOS/ESD Standard ANSI/ESD SP5.6-2019, 2019.

[12] *Electromagnetic Compatibility (EMC)—Part 4-2: Testing and Measurement Techniques-Electrostatic Discharge Immunity Test*, IEC Standard 61000-4-2, 2008.

[13] Y. Shi et al., "A comparative study on G-to-S ESD robustness of the ohmic-gate and Schottky-gate p-GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 70, no. 5, pp. 2229–2234, May 2023, doi: 10.1109/TED.2023.3257282.

[14] C.-C. Ker et al., "Gate-to-source ESD protection design for GaN-on-silicon power HEMT," *Microelectron. Rel.*, vol. 175, Dec. 2025, Art. no. 115948, doi: 10.1016/j.microrel.2025.115948.

[15] "Datasheet of TEA2017AAT/2," NXP Semiconductors Corp., Eindhoven, The Netherlands, 2023.

[16] H. Gossner and C. Duvvury, "System efficient ESD design," *Microelectron. Rel.*, vol. 55, no. 12, pp. 2607–2613, Dec. 2015.

[17] "Datasheet of AZ3103-01F," Amazing Microelectron. Corp., Taipei, Taiwan, 2015.

Chieh-Chen Ker (Graduate Student Member, IEEE) received the B.S. degree from the Department of Photonics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan, in 2025, where he is currently pursuing the Ph.D. degree with the Institute of Electronics. His research interests include the reliability design of integrated circuits and semiconductor devices, as well as analog circuits in the GaN-on-Silicon process.

Chun-Yu Lin (Senior Member, IEEE) received the Ph.D. degree from the Institute of Electronics, National Chiao Tung University, Taiwan, in 2009.

He was an Assistant Professor from 2013 to 2017, an Associate Professor from 2017 to 2021, and a Distinguished Professor from 2021 to 2024 with the Department of Electrical Engineering, National Taiwan Normal University. Since 2024, he has been with the Institute of Electronics, National Yang Ming Chiao Tung University, Taiwan. He also serves as the Secretary-General of Taiwan ESD Association.

Ming-Dou Ker (Fellow, IEEE) received the Ph.D. degree from the Institute of Electronics, National Chiao Tung University (NCTU), Hsinchu, Taiwan, in 1993.

He previously worked as the Department Manager with the VLSI Design Division, Industrial Technology Research Institute, Hsinchu. From 2012 to 2015, he was the Dean of the College of Photonics, NCTU. He has been the Chair Professor with the Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, where he is currently the Director of the Biomedical Electronics Translational Research Center, the Chairperson of the Department of Microelectronics, and the Associate Dean of the College of Electrical and Computer Engineering. In the technical field of reliability and quality design for microelectronic circuits and systems, he has authored/co-authored over 660 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability and quality of integrated circuits, which have been granted with hundreds of U.S. patents. He had been invited to teach and/or consult the reliability and quality design by hundreds of design houses and semiconductor companies in the worldwide IC industry. Some of his inventions or designs had been widely used in the modern IC products and the microelectronic systems. His current research interests include reliability design for nanoelectronics and gigascale systems, as well as the circuits and systems for biomedical applications. He served as a member of the Technical Program Committee and the Session Chair of numerous international conferences for many years, including IEEE International Symposium on VLSI Technology and Circuits, IEEE International Solid-State Circuits Conference, IEEE International Symposium on Circuits and Systems, and IEEE International Reliability Physic Symposium. He also served as the Distinguished Lecturer in the IEEE Circuits and Systems Society from 2006 to 2007 and in the IEEE Electron Devices Society from 2008 to 2020. He has served as an Associate Editor for IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, a Guest Editor for *Frontiers in Neuroscience* on the research topic of microelectronic implants for central and peripheral nervous system, and a Guest Editor for IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY on the special issue of "Electrostatic Discharge and Immunity—From IC to System." He was the Founding President of Taiwan ESD Association, the third President of Taiwan Engineering Medicine Biology Association, and the 21st Vice-President of IEEE Taipei Section. He is currently serving as an Editor for IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY and the IEEE JOURNAL OF THE ELECTRON DEVICES SOCIETY.

Tsung-Yin Chiang received the M.S. degree in engineering and system science from National Tsing Hua University, Hsinchu, Taiwan, in 2005. Since then, he has been with Elan Microelectronics Corporation, where he currently works with the Analog and Memory Department. His research interests encompass analog circuit design, non-volatile memory circuits, ESD protection strategies, and cell development. He is also actively engaged in GaN device ESD protection and testing.

Chun-Chi Wang received the M.S. degree in electrical engineering from National Chung Kung University, Tainan, Taiwan, in 1997. From 1999 to 2002, he served as a Technical Integrated Supervisor Engineer with Macronix International Corporation (MXIC), Hsinchu. He contributed to the development of MXIC nonvolatile cell/CMOS devices. In 2002, he joined Elan Microelectronic Corporation, Hsinchu, assuming responsibilities in analog and nonvolatile memory circuit design with the Analog and Memory Circuit Design Department. In 2011, he supported Elan's ESD group in developing ESD protection devices and circuits for Elan's Touch Pad/Screen/Fingerprint Sensors applications. As of 2015, he took on the role of a Team Leader, overseeing projects related to the analog circuits, including low drift offset amplifiers, bandgaps, temperature sensors, low-power relaxation oscillator, high-voltage gate driver, and charge pumping for power circuits. In 2019, he again devoted his efforts to studying ESD devices with a high-voltage BCD process. By 2021, he was also involved in the ESD development of GaN processes. He is currently a Manager in Analog and Memory Circuit Design Department, Elan. He is an inventor of 12 U.S. patents. His research interests encompass IC ESD plan requirements with ESD device estimation, and analog circuit design.

Ryan Jiang received the M.S. and Ph.D. degrees from the Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, in 1992 and 1998, respectively.

He worked with the Computer and Communication Research Laboratories and SoC Technology Center, Industrial Technology Research Institute, Taiwan, from 1999 to 2003. From 2003 to 2005, he joined two IC design companies, respectively, to develop analog and mixed-signal IC products. In 2006, he founded an IC design company, called Amazing Microelectronic Corporation, and has served as its President. He has proposed many inventions to improve reliability and quality of integrated circuits, which have granted with 63 U.S. patents and 56 Taiwan patents. He also published four IEEE journal papers and 20 international conference papers. His current research topics include ESD protection design, analog IC design, analog circuits behavioral modeling, hardware implementation of neural network, and semiconductor device physics. He was elected as the President of Taiwan ESD Association from 2005 to 2009, and as the Executive Director of BoG from 2011 to 2012. He is currently the Current Supervisor of BoG in the Taiwan ESD Association.