IEEE Open Journal of the
Solid-State Circuits Society

Received 27 November 2025; revised 13 February 2026; accepted 20 February 2026. Date of publication 24 February 2026; date of current version 11 March 2026.

Digital Object Identifier 10.1109/OJSSCS.2026.3667840

ESD Protection Design: Fundamentals and Advanced Strategies

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(Invited Paper)

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This work was supported by the National Science and Technology Council, Taiwan, under Contract NSTC 113-2221-E-A49-190-MY3, Contract 112-2221-E-A49-147-MY3, and Contract 110-2622-8-009-017-TP1.

ABSTRACT Electrostatic discharge (ESD) remains a critical reliability issue in CMOS technologies. This article reviews the fundamentals of ESD phenomena and introduces representative on-chip protection structures. To address the shrinking margin between supply voltage and gate oxide breakdown, the concept of the ESD design window is introduced as a fundamental constraint for selecting and sizing protection devices. The inherent tradeoff between ESD robustness and latch-up immunity is also addressed, highlighting strategies to prevent accidental activation during normal operation. It is further indicated that effective ESD protection is a comprehensive chip-level requirement that extends beyond I/O pads to include robust power-rail clamping and internal protection. Diode-based protection, silicon-controlled rectifier (SCR)-based devices, and MOS clamps are discussed with emphasis on their operating principles, discharge paths, and design tradeoffs. The coordination between I/O protection and power-rail clamps is highlighted as an essential requirement for forming complete discharge paths during ESD events. In addition to presenting the key device and circuit concepts, this article also clarifies how these structures are typically integrated into practical chip designs, providing readers with both intuitive understanding and circuit-level design guidelines that can be directly applied in design practice. Finally, future challenges are outlined, including the impact of advanced technology scaling, 3-D integration, chiplet-based architectures, and increasingly stringent system-level standards. By combining fundamental insights with circuit-level perspectives, this article aims to serve as a clear and accessible tutorial foundation, helping circuit designers and researchers build a comprehensive understanding of ESD protection for modern and future semiconductor technologies, and supporting continued progress in reliable electronic system design.

INDEX TERMS CMOS integrated circuits (ICs), electrostatic discharge (ESD), on-chip electrostatic discharge (ESD) protection design.

I. INTRODUCTION

ELECTROSTATIC discharge (ESD) has long been recognized as one of the most critical reliability concerns in integrated circuit (IC) products [1], [2]. Even a single discharge event can permanently damage thin gate oxides, interconnects, or junctions, leading to catastrophic device failure or latent reliability degradation in the field. As modern ICs are deployed in increasingly diverse applications—from mobile systems and high-performance computing to automotive and Internet of Things (IoT) platforms—the robustness of on-chip ESD protection has become an indispensable requirement for ensuring product reliability and customer confidence.

Technology scaling, however, has introduced profound challenges to ESD protection design [3], [4], [5]. To illustrate the increasing challenge, Fig. 1 shows the typical gate oxide breakdown voltage under ESD-like pulses across successive CMOS technology nodes, revealing a continuous reduction in withstand voltage as devices scale [6], [7]. This trend highlights the shrinking design margin, where the ESD design window must be carefully managed to ensure protection devices trigger and clamp between the supply voltage and the declining oxide breakdown threshold. As CMOS nodes advance into nanometer regimes, devices must operate with ultrathin gate oxides, reduced breakdown voltages, and lower design margins. At the same time, higher integration density

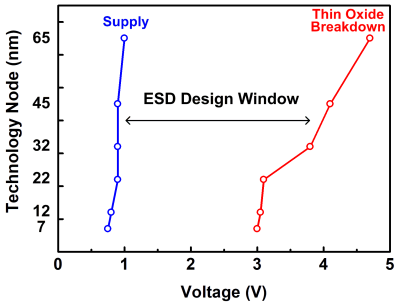

FIGURE 1. Scaling of the ESD design window across CMOS technology nodes.

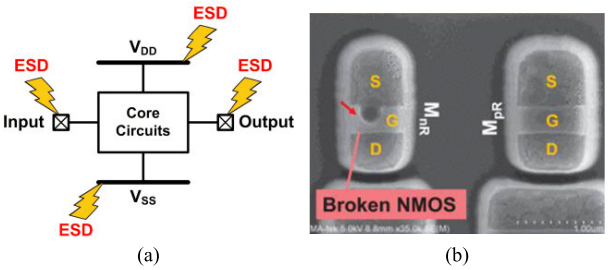

FIGURE 2. (a) Block diagram of I/O pads and supply rails as ESD entry points and (b) ESD damage on an nMOS device after −500 V CDM stress [8].

and heterogeneous system-on-chip architectures significantly increase the number of vulnerable interfaces. Emerging technologies such as FinFETs, gate-all-around (GAA) devices, 3-D ICs, and advanced packaging further complicate ESD design, as their unconventional device structures and current paths alter the behavior of protection devices under stress. In addition, as illustrated in Fig. 2(a), the primary ESD entry points occur at the chip's I/O pads and supply rails, accounting for both one-node and two-node stress constraints that require specific protection strategies. Without the efficient protection, Fig. 2(b) illustrates the resulting ESD damage on an nMOS device after −500 V charged-device-model (CDM) stress [8]. The traditional protection techniques may be less effective and demand new design methodologies to ensure robustness without sacrificing area efficiency or performance.

This article provides a structured overview of ESD protection design from both fundamental and advanced perspectives. The discussion begins with the essential principles of ESD phenomena and standard test models, followed by device physics, circuit-level design guidelines, and layout considerations. Advanced protection strategies suitable for mixed-voltage, high-frequency, and scaled technologies are subsequently introduced. Reliability case studies, modeling approaches, and emerging challenges in future technology nodes are also highlighted, offering practical insights to solid-state circuit designers addressing the realities of ESD in modern integrated systems.

II. ESD PHENOMENA AND TEST METHODS

A. CHARGE GENERATION AND DISCHARGE MECHANISMS

ESD originates from the accumulation of electric charge on insulators, conductors, or semiconductor devices, followed by a sudden discharge when a potential difference exceeds the breakdown threshold of an intervening medium. In practical scenarios, charges are generated by triboelectric effects (e.g., human handling), inductive charging, or device processing steps. The amount of stored energy is often sufficient to damage thin gate oxides, interconnects, or junctions in ICs.

When discharge occurs, the current is released through direct conductive paths, either externally through a tester or handling environment, or internally through junctions and interconnects inside the IC. These events feature fast transients of several amperes within nanoseconds, often leading to localized heating, oxide rupture, or metallization damage; specific quantitative details are provided in Section II-B. Because the time constants, peak currents, and energy involved can vary depending on the charging scenario, standardized stress models have been defined to represent typical conditions.

B. COMMON ESD STRESS MODELS AND TEST STANDARDS

To ensure reproducible evaluation of device robustness, several standardized models have been developed to emulate typical charging and discharge conditions. These are generally categorized into component-level models—including the human body model (HBM), machine model (MM), and CDM—and system-level models, such as the human metal model (HMM).

1) HUMAN BODY MODEL

HBM represents a charged human touching a device. Different industry standards are applied depending on the application domain. According to U.S. Military Standard, HBM testing is primarily specified for discrete components and certain driver ICs [9]. For consumer-grade electronic products, HBM qualification generally follows JEDEC standards [10]. In contrast, for automotive applications, reliability requirements are defined by the Automotive Electronics Council standard for ICs [11]. In these standards, the equivalent circuit of HBM is a 100 pF capacitor discharged through a 1.5 kΩ resistor. As 2 kV is widely adopted as a standard HBM stress level in reliability qualification, the resulting current pulse for a 2 kV HBM typically peaks at approximately 1.3 A with a rise time of ∼10 ns [12], [13]. HBM is historically the most widely adopted qualification model and remains the baseline for handling robustness.

2) MACHINE MODEL

MM represents a direct discharge from a metallic object, such as automated handling equipment [14]. The model uses a 200 pF capacitor and essentially no series resistance, leading to a faster rise time and higher peak current compared

to HBM. The MM has become less commonly specified in recent years, because the original failure mechanisms it simulated are now either eliminated by modern ESD controls or better represented by HBM and CDM methods [7], [15].

3) CHARGED-DEVICE-MODEL

CDM represents the case where the device itself becomes charged and then discharges upon contact with ground or another conductor. Unlike multipin stress models, CDM is fundamentally a one-pin test mode, where the discharge occurs through a single pin while the rest of the device remains floating. For consumer electronic products, CDM testing and qualification are typically carried out in accordance with JEDEC standards [16]. On the other hand, automotive ICs will comply with the reliability requirements specified by the Automotive Electronics Council [17]. The discharge characteristics are heavily influenced by the package type and size; specifically, the package's parasitic capacitance and lead inductance significantly contribute to the peak current and oscillation frequency of the waveform. The equivalent circuit consists of the device capacitance and discharge inductance, leading to subnanosecond rise times and very high peak currents at ampere level. As 500 V is used as a CDM stress level in reliability qualification, the resulting current pulse with a 6.8 pF load may peak as high as 7.2 A with a rise time of <0.25 ns [18]. CDM has become the dominant concern in modern IC qualification, as shrinking technology nodes and increasing integration levels make devices more vulnerable to fast discharge events.

4) HUMAN METAL MODEL

Expanding beyond component-level standards, the HMM characterizes ESD robustness by emulating a person discharging through a metallic interface [19]. The HMM transients exhibit much higher peak currents and accelerated rise times compared to HBM. This makes HMM a critical metric for assessing the protection levels of externally accessible pins [20].

The simplified equivalent circuits for HBM, MM, and CDM are illustrated in Fig. 3, emphasizing the capacitance and resistance of each model. A comparison of typical current waveforms for HBM and CDM is shown in Fig. 4. While MM was historically included in qualification flows, it is not emphasized in waveform comparisons because it has largely been phased out of current industry practice. Therefore, Fig. 4 focuses on the typical current waveforms for HBM and CDM. The HBM waveform is slower with a lower peak current, while CDM exhibits a sharp, high-amplitude spike, demonstrating the distinct challenges each model poses to IC protection design.

C. ALTERNATIVE TEST METHODS AND STANDARDS

At the qualification level, the HBM and CDM remain the industry standards to guarantee a minimum robustness of IC

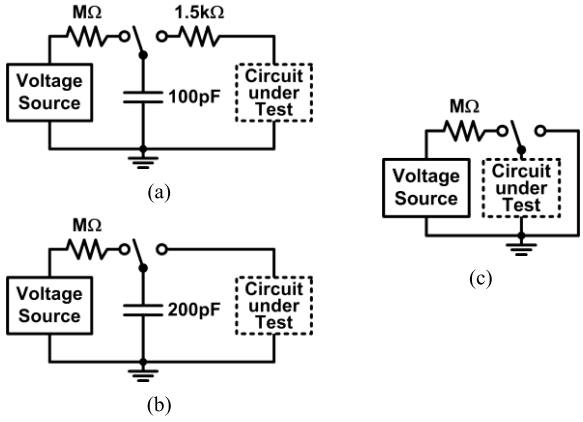

FIGURE 3. Equivalent circuits of standardized ESD stress models (a) HBM, (b) MM, and (c) CDM.

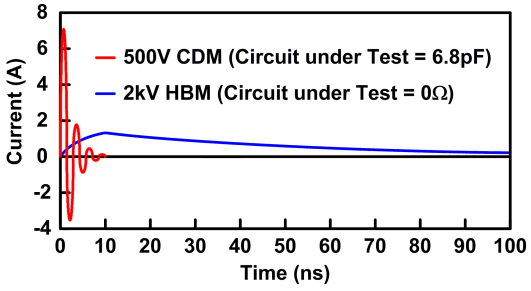

FIGURE 4. Discharge current waveforms of 2 kV HBM and 500 V CDM.

products. While these models are essential for device-level qualification, they provide limited insight into the detailed behavior of protection devices under stress.

For characterization and design purposes, transmission-line-pulse (TLP) testing has become a fundamental methodology [21], [22], [23]. TLP applies rectangular current pulses, typically with a rise time of 1–10 ns and a duration of 100 ns, allowing extraction of quasi-static I–V characteristics by averaging current and voltage data within a specific capture window to emulate steady-state device behavior under ESD-like stress. The measured TLP curve directly shows device trigger voltage, holding voltage, turn-on resistance, and failure current. This makes TLP an indispensable tool for comparing protection devices and validating circuit-level design choices. A simplified TLP setup is illustrated in Fig. 5, showing the generation of TLP I–V characteristics: a pulse from the voltage source is applied to the circuit under test through the 50 Ω line, and the resulting current and voltage responses are measured to construct the I–V curve.

As ESD events, especially CDM, often involve much faster transients, very-fast-TLP (VF-TLP) has been developed to extend this methodology [24], [25]. VF-TLP generates subnanosecond rise time pulses with widths on the order of a few nanoseconds, enabling the characterization of device response under CDM-like conditions. This allows designers to extract the voltage overshoot directly from the transient

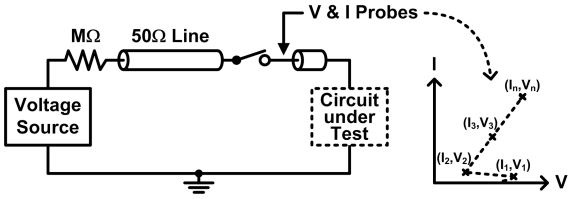

FIGURE 5. Simplified TLP system architecture and the pulse-based I–V measurement principle.

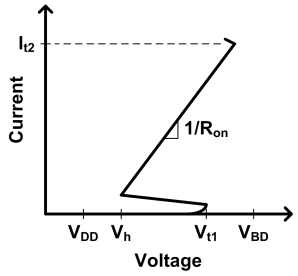

FIGURE 6. TLP I–V curve highlighting V_{t1}, V_h, R_{on}, and I_{t2}.

time response, while also capturing turn-on speed and clamping efficiency, all of which are critical for advanced nodes and high-speed I/O protection.

TLP and VF-TLP data provide quantitative information about device triggering voltage, holding voltage, on-resistance, and failure current levels. By comparing these extracted parameters with realistic stress waveforms, designers can estimate whether an on-chip protection structure is likely to sustain actual operating environments. Fig. 6 shows a typical TLP I–V curve with key parameters, including trigger voltage (V_{t1}), holding voltage (V_h), turn-on resistance (R_{on}), failure current (I_{t2}), circuit supply voltage (V_{DD}), and gate oxide breakdown voltage (V_{BD}) **[26]**. These parameters provide the link between laboratory stress data and practical circuit-level protection design. The ESD design window is defined by the V_{DD} and the V_{BD}. To ensure effective protection, the device parameters V_{t1}, V_h, and I_{t2} must be carefully optimized to fit within this window, ensuring the device triggers and holds above V_{DD} to avoid false conduction while clamping the transient voltage safely below V_{BD}.

D. FAILURE CRITERIA AND INTERPRETATION FOR DESIGNERS

Determining whether a device has ''failed'' under ESD stress is inherently dependent on both the applied test methodology and the functional requirements of the target product. Standard ESD test methods typically define failure in terms of parametric shifts—such as variations in leakage current, I–V characteristics, or other DC parameters—used as quantitative criteria for device degradation. From a system or product perspective, the acceptable level of degradation is governed by functional performance requirements, including parameters such as timing stability, gain, noise figure, communication integrity, or other application-specific metrics [27]. Parametric failure criteria provide precise, repeatable measurements that are useful for characterizing device robustness, whereas functional performance criteria better reflect real-world system impact but can be less consistent and harder to quantify. Furthermore, ESD stress can cause latent damage, where the device remains functional immediately after the event but suffers from internal physical defects that accelerate aging and lead to premature field failure.

For circuit designers, interpreting failure data requires linking the underlying physical mechanisms to critical design parameters. For example, a low trigger voltage may result in unintended leakage during normal operation, while insufficient holding voltage can increase susceptibility to latch-up. Similarly, the I_{t2} parameter defines the maximum survivable current, directly influencing the sizing and selection of protection devices. By understanding both the test methodology and the defined failure criteria, designers can translate ESD test results into actionable design decisions that balance robustness, leakage, and overall functional performance.

E. COMPREHENSIVE ESD ROBUSTNESS EVALUATION

In ESD qualification of ICs, all relevant discharge paths within the device must be thoroughly evaluated [9], [10], [11]. For I/O pads, four primary test modes are commonly used: positive-to-V_{SS} (PS), negative-to-V_{SS} (NS), positive-to-V_{DD} (PD), and negative-to-V_{DD} (ND), as shown in Fig. 7(a)–(d) [28], [29], [30]. In addition, I/O-to-I/O testing is performed to assess discharge between pins and ensure that no signal path is vulnerable under transient conditions [28], [29]. For high-pin-count devices, a ''Group Pins'' test methodology is often employed to improve testing efficiency; in this approach, multiple pins—typically those within the same power domain or functional group—are stressed simultaneously against a common reference pin or rail. Within the power domain, V_{DD}-to-V_{SS} testing is conducted to assess the basic robustness of the supply network, as shown in Fig. 7(e) and (f) [30]. Stress between multiple supply rails, such as V_{DD1}-to-V_{DD2}, is also performed to evaluate the robustness of the internal power network [31], [32]. It should be noted that this discussion excludes charge CDM testing; CDM tests are performed separately and involve both positive and negative discharge on each individual pin to evaluate pin-level susceptibility to fast pin-to-ground discharge events [16], [17].

When an IC is specified with an ESD rating of, for example, 2 kV, this requirement applies to all defined modes. Each mode must pass at the specified voltage level, ensuring that the device exhibits uniform robustness across all I/O and power configurations. This includes the Group Pins configuration, where the cumulative leakage or functional shift of the group must stay within specified limits to ensure no individual pin has been compromised. This approach guarantees that the declared ESD specification accurately reflects the minimum withstand capability of the IC across its complete set of internal discharge paths.

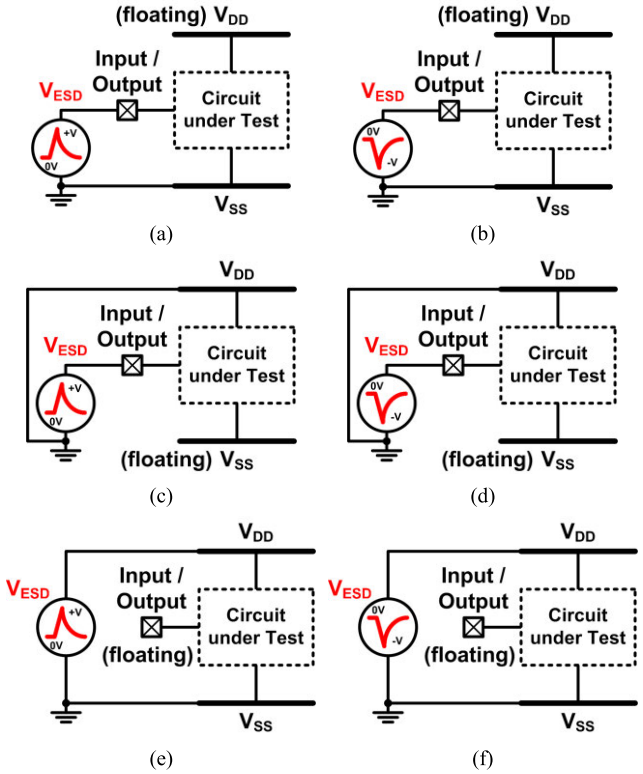

FIGURE 7. Common test modes applied to I/O and power rails (a) PS, (b) NS, (c) PD, (d) ND, (e) positive V_{DD}-to-V_{SS}, and (f) negative V_{DD}-to-V_{SS}.

F. CIRCUIT AND SYSTEM-LEVEL PRACTICAL CONSIDERATIONS

ESD robustness remains a critical requirement across semiconductor products. While HBM provides a baseline qualification target for manual handling, CDM better reflects risks in automated assembly and high-speed systems. For advanced CMOS nodes with thin gate oxides and low supply voltages, CDM failures often dominate due to their extremely fast and intense current transients. At the system level, ESD events can also couple into IC pins through cables, connectors, and PCB traces, creating stress beyond device-level qualification standards. Consequently, chip-level protection must be co-designed with package and board-level safeguards to ensure end-product compliance with standards such as IEC 61000-4-2 [33].

From a circuit design perspective, these requirements directly impact I/O buffer topology, pad-ring layout, and clamp circuit architectures. Effective ESD protection must balance robustness with leakage, capacitance, and performance, making the understanding of ESD fundamentals essential for guiding practical circuit-level design choices. In advanced nodes, the reduced voltage headroom and thinner gate dielectrics further tighten these tradeoffs, requiring innovative device structures and circuit techniques. Moreover, high-speed and RF interfaces impose strict capacitance limits, forcing designers to integrate protection structures with minimal parasitic loading. As a result, ESD considerations are not isolated reliability checks but an integral part of the overall circuit architecture, influencing how modern solid-state circuits are conceived, optimized, and qualified.

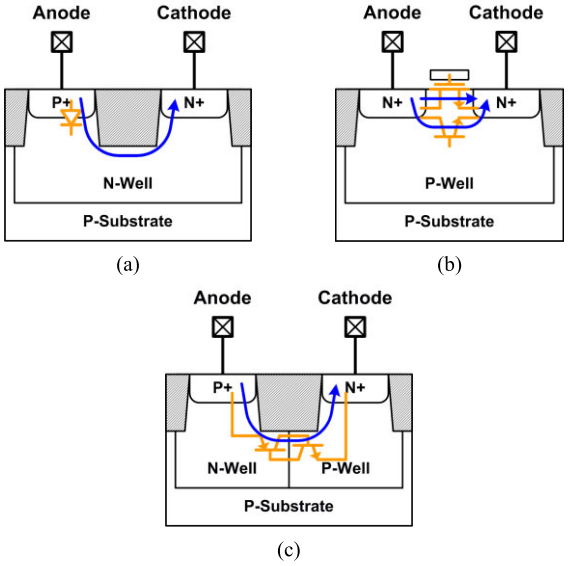

FIGURE 8. Cross sections and equivalent circuits of common ESD devices (a) diode, (b) nMOS, and (c) SCR.

III. ESD PROTECTION DEVICE PHYSICS AND BEHAVIOR

A. COMMON ON-CHIP ESD PROTECTION DEVICES

On-chip ESD protection structures are indispensable in CMOS technologies because they can be implemented within standard design rules while still providing a rapid, low-impedance path for discharging large transient currents away from sensitive circuits. The most commonly adopted elements include diodes [30], [34], [35], [36], [37], [38], [39], MOSFETs [40], [41], and silicon-controlled rectifiers (SCRs) [42], [43], [44], [45], [46], [47], [48], as illustrated in Fig. 8, each offering distinct advantages and challenges in design. Their corresponding I–V characteristics are shown in Fig. 9, which reveal the conduction behavior of these devices under ESD stress.

1) DIODES

Diodes, shown in Fig. 8(a) with their I–V curve in Fig. 9(a), are the simplest and most frequently used ESD protection devices [34], [35], [36], [37], [38], [39]. The active regions are electrically isolated by the shallow trench isolation (STI), indicated in gray in Fig. 8. The diodes are typically placed between the I/O pad and the power or ground rails, providing a low-impedance conduction path during a positive ESD pulse. The I–V curve demonstrates the exponential forward conduction once the pad voltage exceeds the threshold of approximately one diode drop above the rail. Under negative ESD stress, however, the diode relies on avalanche breakdown to conduct current, and its discharge capability is significantly weaker due to the higher turn-on resistance and

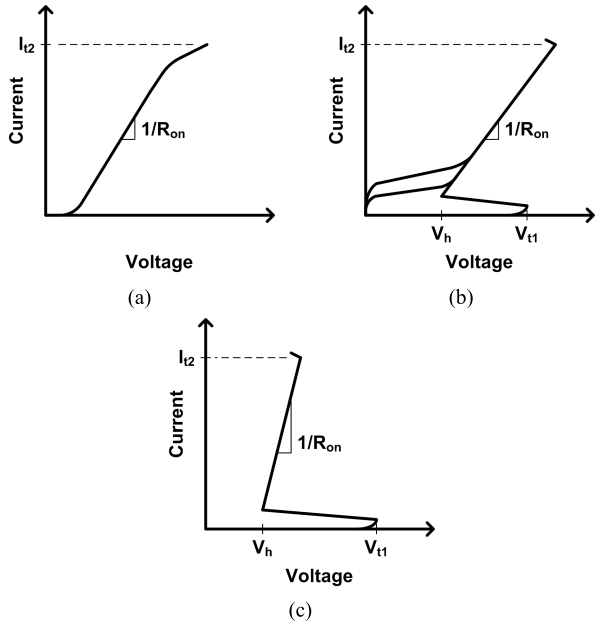

FIGURE 9. Typical I–V characteristics of (a) diode, (b) nMOS, and (c) SCR.

limited robustness in reverse mode. As a result, diodes are highly effective for positive stress but less reliable for handling negative stress on their own. Their overall performance is still constrained by device area and parasitic capacitance; larger diodes can sustain more current but increase capacitance at the I/O node.

2) MOSFETs

MOSFET-based protection devices, represented by the nMOS in Fig. 8(b) with its corresponding I–V curve in Fig. 9(b), provide an important discharge path that combines both MOS channel conduction and parasitic bipolar conduction [30], [40], [41]. The gate connection is specifically configured—either tied to the ground for a gate-grounded nMOS (GGNMOS) or connected to a triggering circuit—to determine the specific voltage at which the device activates. During an ESD event, the MOS channel may conduct when triggered through external circuitry such as *RC*-coupled clamps, offering a controllable low-impedance path. At the same time, avalanche breakdown of the drain-substrate junction can activate the parasitic lateral n-p-n transistor, driving the device into snapback. Consequently, this device operates not merely as a conventional MOSFET but as a bipolar-MOS (BIMOS) hybrid during an ESD event, leveraging the parasitic BJT path to achieve high current-handling capability. This dual conduction mechanism is reflected in the I–V characteristic, where the device transitions from an initially high-impedance state to a low-resistance conduction state defined by the trigger voltage and holding voltage. The coexistence of channel conduction and parasitic bipolar action makes nMOS devices both versatile and robust in handling ESD currents. To ensure stable operation and prevent localized failure, techniques such as multifinger segmentation, ballast resistors, and silicide blocking are commonly applied to enhance current uniformity and thermal reliability.

3) SILICON-CONTROLLED RECTIFIERS

SCR-based protection devices, depicted in Fig. 8(c) and corresponding to the I–V curve in Fig. 9(c), exhibit exceptionally high current-handling capability per unit area due to their regenerative conduction mechanism and very low on-state resistance [42]. Nevertheless, their relatively high trigger voltage can delay turn-on during an ESD event, potentially exposing the protected circuitry to excessive stress. To address this limitation, several structural variants have been developed to lower the trigger voltage while maintaining robustness [43], [44], [45]. In addition, the inherently low holding voltage of conventional SCRs raises latch-up concerns when it overlaps with the normal operating range [46], [47]. In spite of these challenges, the low parasitic capacitance of SCR-based devices renders them highly suitable for high-speed and RF applications, provided that thorough verification is performed to ensure stable and reliable operation [48].

4) RESISTORS

Although resistors are not explicitly illustrated in Fig. 8, they play an important complementary role when combined with the primary protection structures. Depending on their function, these components are typically implemented as unsilicided polysilicon resistors for *RC*-trigger networks, or as diffusion resistors for ballasting to ensure current uniformity across multifinger structures. Small series resistors can also be used to suppress voltage overshoot and limit peak current in the signal path [49], yet their inherent resistance and capacitance may degrade signal integrity, so their values must be carefully optimized. Shunt resistors are employed [50], and resistors in *RC*-trigger networks facilitate the rapid activation of rail clamps [51], [52].

B. KEY PHYSICAL INSIGHTS RELEVANT FOR CIRCUIT DESIGNERS

In practice, robust on-chip ESD protection relies on the coordinated use of multiple device types. Diodes provide the fastest pad-to-rail discharge path, MOSFETs extend conduction through snapback or triggered clamps across the power rails, and SCRs deliver superior current-handling capability when area efficiency is critical. Together with careful management of electrothermal effects, these elements form the foundation of reliable and scalable ESD protection strategies in advanced CMOS technologies.

For circuit designers, a clear understanding of these physical mechanisms is essential to making effective tradeoffs. Diodes offer simple and fast protection but add junction capacitance, which limits their suitability for high-frequency I/O. nMOS devices are highly versatile and provide strong discharge capability, particularly for power-rail clamps, but

they exhibit even larger parasitic capacitance than diodes, making them less attractive for high-frequency I/O. In addition, careful layout is required to ensure uniform triggering and to avoid single-finger burnout. SCRs provide excellent current efficiency, but their trigger and holding voltages must be engineered to align with the supply rails to prevent latch-up. Resistive elements can aid current sharing and timing control, but they introduce voltage drops and area overhead that must be considered.

It is, therefore, critical to recognize that ESD protection devices do not behave as ideal switches. Their conduction characteristics are governed by parasitic bipolar effects, snapback dynamics, and electrothermal interactions. These physical insights inform the sizing, triggering schemes, and layout practices necessary to integrate protection structures effectively, ensuring robust ESD resilience without compromising normal circuit performance.

IV. ESD PROTECTION CIRCUIT DESIGN PRINCIPLES

A. WHAT DEFINES "GOOD" ESD PROTECTION

A "good" ESD protection design is not only about surviving qualification tests but also about ensuring long-term circuit reliability with minimal penalty. Its quality can be evaluated along four key dimensions [53].

1) ROBUSTNESS

Robustness refers to the intrinsic ability of the clamp device to safely conduct the full ESD current without failure. This depends on several factors, including the device's area, current distribution uniformity, and thermal handling capability. In the context of the ESD design window, robustness is quantitatively defined by the I_{t2}, which must exceed the peak current of the target ESD specification. Proper layout and sizing ensure that no single device region experiences excessive current density or localized heating that could lead to permanent damage. Material choices and process variations also influence robustness, making it critical to design with realistic worst-case conditions in mind.

2) EFFECTIVENESS

Effectiveness measures how well the protection network limits its voltage at the protected node to safe levels. A highly effective ESD network prevents destructive overstress of sensitive circuits connected in parallel to the protection structures. To achieve this, the device must operate strictly within the ESD design window: the V_{t1} must remain below the V_{BD} to prevent dielectric failure, while the V_h must be maintained above the V_{DD} to provide immunity against latch-up events. This requires careful placement of clamps, proper triggering thresholds, and coordination across multiple device types to ensure that voltage spikes are shunted quickly and efficiently to the power rails or ground.

3) SPEED

Speed is crucial because ESD events, particularly CDM transients, can rise to damaging levels in subnanosecond timescales. The protection clamp must activate fast enough to suppress voltage overshoot before it exceeds the breakdown limits of on-chip devices. Factors affecting speed include device parasitics, trigger voltage, and layout-dependent *RC* delays, all of which must be optimized to achieve near-instantaneous conduction.

4) TRANSPARENCY

Transparency denotes the ability of the protection circuit to remain effectively invisible during normal operation. This includes minimizing added capacitance on high-frequency/high-speed I/O lines, avoiding leakage currents in low-power designs, ensuring proper behavior during power-on or hot-plug events, and maintaining tolerance to multiple voltage domains in mixed-signal circuits. A transparent ESD design protects without compromising the intended electrical performance or functional specifications of the system.

Taken together, these criteria define what makes an ESD protection circuit both robust under stress and nonintrusive during normal operation. Achieving a balance among robustness, effectiveness, speed, and transparency is the central challenge for circuit designers, particularly in advanced CMOS technologies where device dimensions are shrinking, and operational margins are tight.

B. TRADEOFFS: AREA, LEAKAGE, CAPACITANCE, SPEED

The design of ESD protection circuits inevitably involves a set of tradeoffs among robustness, leakage, parasitic capacitance, and speed. From a circuit design perspective, the width and area of protection devices play a critical role: wider MOS transistors or larger diode junctions can conduct higher current densities, thereby enhancing robustness, but this improvement comes at the expense of silicon area and manufacturing cost. Furthermore, larger devices usually exhibit increased junction capacitance, which directly limits the bandwidth of high-frequency interfaces such as RF transceivers or SerDes channels.

Leakage current is another fundamental constraint. Low-threshold diodes or MOS clamps provide fast triggering and better robustness, but their off-state leakage degrades power efficiency, which is unacceptable in ultralow-power systems. To address this challenge, designers often employ dynamic triggering methods, such as *RC*-triggered clamps or gate-coupled MOSFETs, which remain "off" in normal operation and only activate during an ESD transient. These approaches minimize standby leakage without compromising the required robustness.

The tradeoff between speed and stability is particularly evident in CDM protection. Circuit structures with very fast triggering—such as gate-coupled nMOS devices—can respond within picoseconds and protect against rapid voltage

transients. However, their sensitivity also raises the risk of false activation during normal I/O transitions or hot-plug events. To mitigate such risks, the distinction between dynamic and static triggering mechanisms is critical. While dynamic sensing provides rapid activation by responding to the fast rise time of an ESD event, it can be prematurely triggered by the steep voltage slopes encountered during hot-plugging. Conversely, static sensing offers higher stability in these scenarios by ensuring the clamp only activates when a specific voltage threshold is exceeded. A more detailed comparative analysis of these triggering strategies, specifically within power-rail ESD protection circuits, will be provided in Section V-C. Careful selection of *RC* time constants, triggering thresholds, and device sizing is essential to achieve reliable operation without performance penalties.

V. ESD PROTECTION CIRCUIT DESIGN METHODOLOGIES AND LAYOUT CONSIDERATIONS

A. DESIGN METHODOLOGIES AND PROTECTION STRATEGIES

A systematic ESD design begins with an analysis of the IC's most vulnerable nodes and the possible discharge paths. Modern ICs typically adopt a two-level protection strategy consisting of local I/O clamps and global power-rail clamps. I/O clamps, placed directly at the bond pads, serve as the first line of defense against surges entering through signal lines. Depending on the application, these clamps may be realized with simple diode strings to the supply rails [34], [35], [36], [37], [38], [39], grounded-gate nMOS (ggNMOS) transistors [40], [41], or SCR [42], [43], [44], [45]. For RF and high-speed interfaces, designers often adopt low-capacitance devices to minimize the parasitic loading on sensitive signal lines [48], [54].

It is important to emphasize that effective ESD protection is not limited to I/O interfaces; rather, it requires a holistic chip-level approach to safeguard internal circuits and power domains. The second layer of protection is provided by power-rail ESD clamps, which actively guide the majority of the ESD current to ground. By using a dedicated power-rail ESD protection circuit, the ESD current can be efficiently directed along a controlled low-impedance path, significantly enhancing the whole-chip ESD protection level [55]. Furthermore, the parasitic resistance of the power and ground rails must be accounted for in this holistic approach; excessive rail resistance can cause significant IR drops during high-current ESD events, potentially elevating the voltage at the internal nodes beyond the failure threshold. By minimizing these resistance paths and optimizing the placement of rail clamps, the ESD current can be efficiently directed along a controlled low-impedance path. A widely used implementation is the *RC*-triggered MOS clamp, where an *RC* differentiator senses the rapid voltage rise associated with an ESD surge and activates a large MOS transistor to provide a low-impedance discharge path [51], [52]. Alternative solutions include triggered SCRs or hybrid clamps, which combine compact area and high robustness [42], [43]. The overall architecture of this whole-chip ESD protection strategy is summarized in Fig. 10, where input/output protection devices cooperate with a global power-rail ESD protection to form a complete ESD protection circuit.

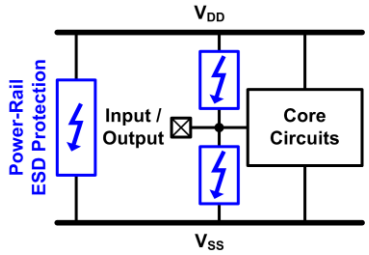

FIGURE 10. Whole-chip ESD architecture combining I/O and power-rail ESD protection circuits.

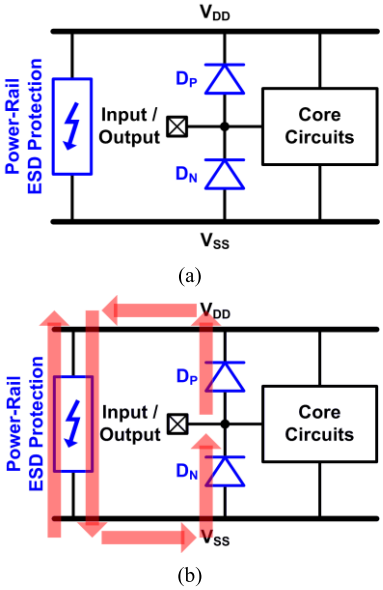

FIGURE 11. (a) Diode-based I/O protection circuit and (b) its discharging paths.

B. EXAMPLE OF I/O ESD PROTECTION CIRCUITS

One of the most common solutions is the diode-based protection structure [34], [35], [36], [37], [38], [39]. As shown in Fig. 11(a), the I/O pad is connected to V_{DD} through the forward diode (D_p) and to V_{SS} through the reverse diode (D_n). During an ESD event, these diodes turn on and divert the surge away from the core circuits. While diode protection is fast and effective, its tradeoff lies in the added junction capacitance, which may limit applicability in very-high-frequency designs. Furthermore, diodes alone cannot provide a direct I/O-to-V_{SS} discharge path. Instead, the discharge current must pass through D_p into V_{DD} and then rely on a power-rail ESD protection circuit to complete the discharge to V_{SS}, as illustrated in Fig. 11(b). By incorporating an efficient power-rail ESD protection circuit, the discharge current from the I/O pad can be quickly directed through the forward diode into the V_{DD} or V_{SS} line and then discharged via the

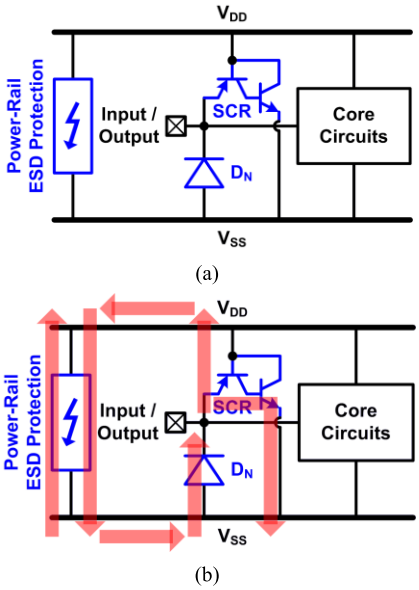

FIGURE 12. (a) SCR-based I/O protection circuit and (b) its discharging paths.

power-rail ESD protection circuit. This mechanism allows the ESD devices connected at the I/O pad to remain small, since the ESD current is discharged through the forward diode with relatively low clamping voltage. Even with compact ESD devices at I/O pad, the overall protection level can still reach several kilovolts in HBM testing when the power-rail ESD protection circuit assists the discharge. This cooperative discharge mechanism thus enables a low-capacitance ESD protection structure to achieve both high ESD robustness and minimal parasitic loading, making it suitable for high-frequency applications.

To further enhance robustness, SCR-based devices are also widely adopted because of their strong current-handling capability and compact layout efficiency [42], [43], [44], [45]. The discharge paths of an SCR may exist between the I/O pad and either V_{DD} or V_{SS}. One example is illustrated in Fig. 12(a), where the SCR device provides a direct I/O-to-V_{SS} discharge path, and its intrinsic p-n junction offers an additional I/O-to-V_{DD} path. In parallel, D_N conducts from V_{SS} to I/O, and the power-rail ESD protection circuit completes the discharge between V_{DD} and V_{SS}. The discharging paths are illustrated in Fig. 12(b). This combined protection strategy enables fast initial conduction through the diodes while leveraging the SCR to sustain high current flow, thereby improving overall ESD robustness. Nevertheless, designers must ensure that the SCR holding voltage remains higher than the nominal supply voltage to avoid latch-up [46], [47].

While this cooperative mechanism is straightforward within a single power domain, modern SoCs frequently use multiple power supply rails (V_{DD1}, V_{DD2}, etc.) to optimize performance and power. In such multipower domain environments, additional back-to-back diode strings or cross-domain clamps must be implemented to facilitate discharge between

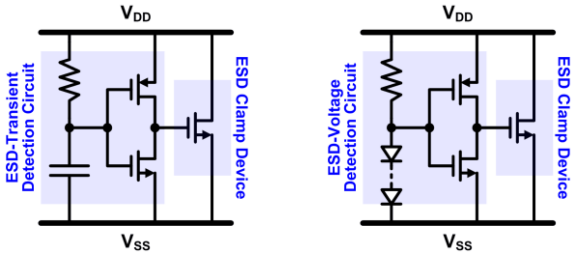

FIGURE 13. Power-rail ESD protection circuits with ESD clamp device and (a) ESD-transient rise time sensing and (b) voltage-level sensing.

disparate supply rails, ensuring that internal circuits are not damaged by interdomain voltage differentials [31], [32].

C. EXAMPLE OF POWER-RAIL ESD PROTECTION CIRCUITS

A typical power-rail ESD protection circuit consists of an ESD-transient detection circuit and an ESD clamp device. The detection circuit may be designed to sense either the steep voltage rise associated with an ESD event or the absolute voltage level across the supply rails. The clamp device itself is typically realized using a large nMOS transistor—often referred to as "BigFET."

The *RC*-inverter-nMOS implementation, illustrated in Fig. 13(a), represents one of the most straightforward approaches [51]. In this design, an *RC* network monitors the transient rise time on the power rails, and the output of an inverter is used to drive a large nMOS transistor that provides a low-impedance discharge path between V_{DD} and V_{SS}. From a latch-up perspective, the *RC* time constant must be carefully tuned; if the turn-off delay is too long, the BigFET may remain conductive after the ESD event subsides, potentially sustaining a low-impedance path that triggers a localized latch-up event or thermal runaway under normal bias. Alternatively, a voltage-level detection circuit can be employed, as illustrated in Fig. 13(b). In this scheme, the detection unit monitors the absolute voltage across the supply rails instead of relying on the transient rise time [55], [57]. To ensure latch-up immunity, the activation threshold of this voltage-level detector must be set higher than the maximum allowable V_{DD} to prevent the clamp from being triggered by power supply noise or ripples during normal operation. When the rail voltage exceeds a predetermined threshold during an ESD event, the detection circuit activates the BigFET device, thereby creating a robust discharge path from V_{DD} to V_{SS}. These approaches allow the clamp device to remain inactive during normal power-on conditions.

Furthermore, in applications such as artificial intelligence (AI) server circuit boards, where hot-swap or board replacement operations are frequent, it is critical to prevent false triggering of power-rail ESD protection circuits during fast power-on events. Rapid powering-on of a board can generate voltage transients that resemble ESD stress, which

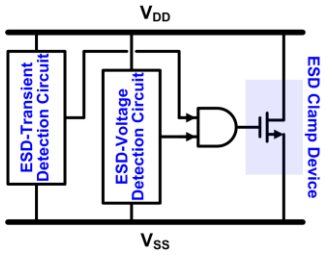

FIGURE 14. Power-rail ESD protection circuit with BigFET ESD clamp device and both ESD-transient and ESD-voltage detection circuits.

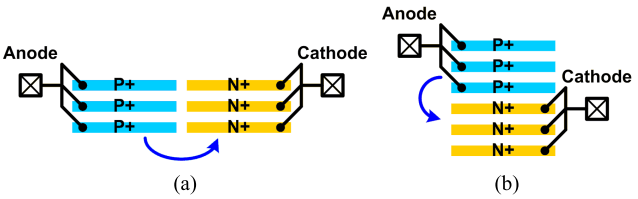

FIGURE 15. FinFET diode layouts (a) nonrotated and (b) rotated for reduced resistance.

may inadvertently activate conventional power-rail ESD protection circuits and cause unnecessary current conduction, potential voltage droop, or even device damage. To address this challenge, a specialized power-rail ESD protection circuit with dynamic timing-voltage detection can be employed. This circuit continuously monitors the ramp of the supply voltage during power-on and compares it against a pre-defined timing and voltage threshold. Only when the detected event exceeds the genuine ESD criteria does the clamp activate, providing a controlled low-impedance discharge path. This approach not only ensures that the IC remains protected against real ESD strikes but also prevents false conduction that could disrupt normal board operation during hot-swap or rapid initialization procedures. Fig. 14 illustrates a conceptual schematic of this fast power-on aware power-rail ESD clamp, showing the dynamic timing-voltage detection circuit interfaced with the main ESD clamp device [58], [59], [60]. By integrating such a mechanism, the whole-chip ESD protection level is significantly enhanced, particularly in environments requiring frequent hot-swap operations, without compromising device reliability or standby power performance.

D. LAYOUT CONSIDERATIONS AND CIRCUIT-LAYOUT COUPLING

Even the most carefully designed clamp circuits can fail if the layout implementation is inadequate. Since ESD events involve extremely high transient currents, the parasitic resistances of interconnects strongly influence actual performance. Fig. 15 compares two diode layouts in FinFET technology [61], [62]. In Fig. 15(a), the diode is aligned along the fin direction, whereas in Fig. 15(b), the diode is rotated to be perpendicular to the fins. This rotated configuration allows current to flowthrough multiple fins in parallel, reducing the effective series resistance and enhancing the device's current-handling capability [63]. Consequently, the rotated diode structure improves the uniformity of ESD triggering and provides more reliable protection, mitigating the adverse impact of parasitic resistances in advanced FinFET circuits.

Similarly, MOS-based clamps are typically implemented in multifinger configurations [40], [41]. Without careful design, current crowding may cause one finger to fail prematurely, compromising the robustness of the entire device. In power-rail protection, large-width MOS transistors, often referred to as BigFETs, are used to handle the high current conduction required during an ESD surge. However, these BigFETs must be carefully laid out to avoid resistive bottlenecks and ensure uniform gate biasing [64], [65]. Therefore, the co-design of circuit topology and layout is essential to achieve the intended protection performance.

VI. ADVANCED ESD PROTECTION STRATEGIES

A. CDM-SPECIFIC DESIGN APPROACHES

As CDM events exhibit subnanosecond rise times and ampere-level peak currents, protection devices must switch on almost instantaneously. Conventional HBM-oriented clamps may be inadequate, since their slower response can result in voltage overshoot that threatens thin gate oxides. CDM-tailored solutions therefore emphasize speed and locality, typically employing a two-stage protection hierarchy. In this architecture, a primary stage—consisting of large-area diodes or SCRs—is designed to shunt the bulk of the high-current ESD surge, while a secondary stage—usually a smaller, faster clamp placed directly at the gate of the input buffer—is used to limit the residual voltage below the gate oxide breakdown level. For example, low-capacitance diode strings provide immediate conduction paths with minimal loading on I/Os, as shown in Fig. 16 [66], [67]. In addition, distributed rail clamps are placed closer to pads to reduce inductive delay along supply lines, while local clamps at sensitive nodes are often required to further suppress residual voltage spikes before they propagate into core circuits [68]. Furthermore, CDM protection is not restricted to the I/O periphery; it must also be implemented within the chip core to safeguard internal logic and power-crossing interfaces. In large-scale SoCs, fast-acting core clamps and local decoupling capacitors are strategically distributed throughout the core area to suppress internal voltage transients and protect sensitive thin-oxide transistors from charge-device discharges occurring deep within the silicon. To further enhance robustness, triggered SCRs with fast turn-on assist circuits are frequently employed, combining rapid response with strong current-handling capability [69]. Moreover, active detection schemes have been investigated, where circuits sense the steep voltage ramp associated with CDM discharge and directly bias protection devices into conduction [70].

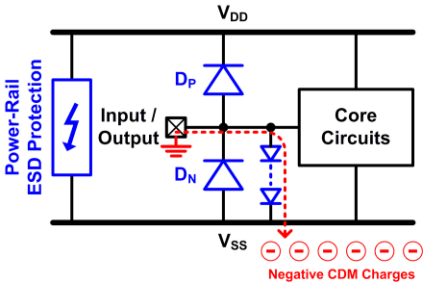

FIGURE 16. Local clamp for CDM protection with fast triggering near sensitive nodes.

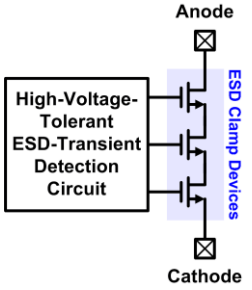

FIGURE 17. High-voltage-tolerant ESD protection using cascoded and bias-assisted devices.

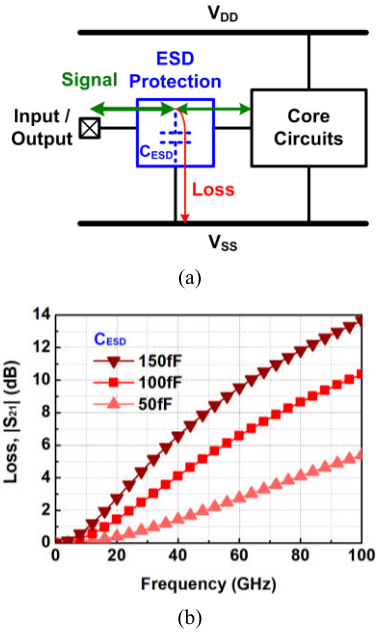

FIGURE 18. (a) Illustration of signal degradation due to parasitic capacitance from ESD protection circuits at a high-frequency I/O. (b) Simulated insertion loss versus frequency.

B. MIXED-VOLTAGE I/O WITH HIGH-VOLTAGE-TOLERANT ESD PROTECTION

In advanced SoCs, I/O interfaces often connect low-voltage core circuits to higher-voltage external domains such as 2.5 or 3.3 V. High-voltage-tolerant ESD protection is therefore required to handle electrostatic stress without introducing leakage or overstress during normal operation [52], [71], [72], [73]. This is typically achieved using cascoded transistors, stacked diode strings, or gate-bias-controlled devices that block conduction at normal voltages but provide fast, low-impedance paths during ESD events. Thick-oxide devices or dynamic biasing can further enhance voltage tolerance while maintaining rapid turn-on for ESD robustness. Fig. 17 illustrates a high-voltage-tolerant ESD protection schematic, highlighting stacked devices and biasing techniques that enable reliable ESD conduction across multiple voltage domains. The use of high-voltage I/O increases the risk of latch-up due to the presence of parasitic bipolar transistors formed between the high-voltage nodes and the substrate. To mitigate this, the holding voltage of the protection devices must be carefully engineered to exceed the maximum supply voltage, and stringent layout techniques—such as the implementation of deep n-well isolation and heavily doped guard rings—are required to reduce the gain of parasitic paths and prevent regenerative current conduction.

C. HIGH-SPEED AND HIGH-FREQUENCY APPLICATIONS

In nanoscale CMOS processes, one of the major concerns for high-speed and high-frequency circuits is the parasitic capacitance introduced by ESD protection devices. Such parasitics not only attenuate the signal at the I/O interface but also cause impedance mismatch and phase distortion, thereby degrading signal integrity [74]. Fig. 18(a) illustrates the signal loss at the I/O of a core circuit due to the parasitic capacitance (C_{ESD}) of the ESD protection circuit. The simulation results in Fig. 18(b) demonstrate the frequency-dependent loss of the ESD protection circuit [75]. As frequency increases, the capacitive effect becomes more pronounced, resulting in a significant rise in insertion loss. This excessive loss severely degrades the signal integrity and indicates that the design is not suitable for high-frequency applications without further optimization. To address these concerns, several design techniques have been employed to minimize the interaction between ESD devices and sensitive signal paths [54]. Moreover, conventional diode-based clamps become less effective in low-voltage CMOS due to their relatively high forward voltage drop, motivating the development of alternative approaches such as dynamic triggering circuits and optimized SCR structures that combine fast response with reduced loading [76], [77], [78].

An effective configuration for high-frequency I/O protection incorporates a series inductor either in conjunction with a shunt capacitor [79] or positioned between two shunt capacitors, as illustrated in Fig. 19 [45], [80], [81], [82], [83]. This arrangement forms a π-type matching network in which the shunt capacitances are typically provided by diodes or SCRs, while the series inductor is used to adjust the I/O impedance. The combined effect enables broadband impedance matching and mitigates signal loss at high frequencies, both of which are essential for high-speed interfaces. During an ESD event, the diodes or SCRs, together with the power-rail ESD

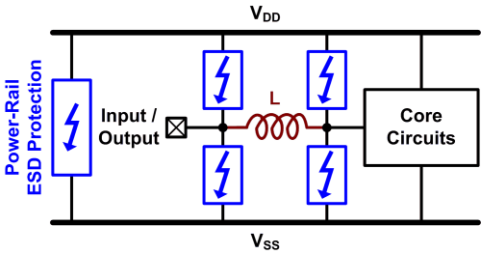

FIGURE 19. π-type matching network integrating shunt ESD devices with a series inductor.

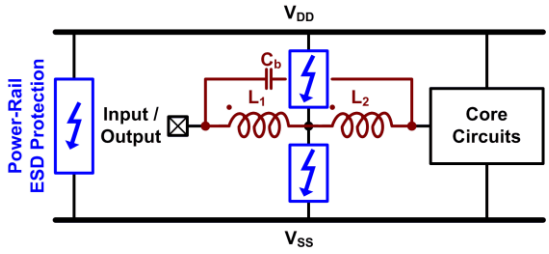

FIGURE 20. T-coil-based ESD protection circuit achieving broadband impedance matching.

protection circuit, provide the primary discharge path for the ESD current. The series inductor further limits the magnitude of ESD surge currents that could otherwise penetrate into the core circuits. Under normal operation, the inductor also shapes the frequency response of the I/O path, thereby preserving signal integrity.

For wideband applications, specialized circuit techniques have been introduced to mitigate parasitic effects while maintaining robust ESD protection. A representative example is the T-coil-based ESD protection network [84], [85], [86], [87]. As shown in Fig. 20, the T-coil consists of two coupled inductors (L_1 and L_2) placed between the I/O pad and the circuit input, with a shunt ESD device connected at the intermediate node. This configuration enables broadband impedance matching by compensating for the parasitic capacitance of the ESD device and interconnects, thereby improving return loss and minimizing signal reflections. Additionally, the intrinsic coupling capacitance between L_1 and L_2 supports the resonance behavior of the T-coil, further extending bandwidth. During an ESD event, the shunt device provides the discharge path. In terms of CDM protection, the T-coil network functions as an integrated voltage-clamping filter; the mutual inductance and bridge capacitance of the T-coil can be optimized to delay and attenuate the incoming ESD surge. This ensures that the primary shunt device triggers effectively while the secondary residual voltage remains within the safe operating window of the core circuits. Under normal operation, the T-coil network preserves signal integrity across a wide frequency range. Such co-optimized structures demonstrate how ESD robustness and high-frequency performance can be simultaneously achieved in advanced circuit applications.

VII. FUTURE CHALLENGES

A. IMPACT OF CONTINUED TECHNOLOGY SCALING

As CMOS technologies continue to scale into advanced nanometer nodes, ESD protection design faces increasing challenges. The continual reduction in gate oxide thickness and supply voltage limits the voltage margin available for robust ESD protection. Traditional clamp devices, such as large MOSFETs or diode-based structures, suffer from excessive leakage, reduced breakdown voltage, and degraded current-handling capability in these nodes. Crucially, the design of the power distribution network (PDN) becomes a dominant factor in determining whole-chip robustness. In advanced nodes, the increased resistance of narrow metal interconnects necessitates a co-design approach where the PDN is optimized for low impedance to minimize IR drops during ESD transients. Furthermore, the reliability of these interconnects is increasingly threatened by ESD-induced electromigration, where the energy-handling capability of various metal geometries decreases as ESD voltage levels rise, necessitating careful optimization of metal width, length, and routing angles to prevent permanent failure [88]. Moreover, the variability of device characteristics under process corners further complicates the design of reliable ESD clamps. Future research must therefore focus on developing novel device structures and circuit techniques that balance leakage, area efficiency, and robustness while remaining compatible with advanced CMOS design rules.

B. ESD CHALLENGES IN 3-D ICs

3-D ICs present new ESD protection concerns due to their unique architecture. Through-silicon vias (TSVs) and die stacking introduce additional current paths and parasitic coupling mechanisms that can exacerbate ESD stress conditions. Unlike traditional 2-D layouts, ESD currents in 3-D ICs may propagate across multiple dies or through the package stack, leading to complex discharge scenarios [89], [90]. Effective ESD mitigation in these systems relies heavily on the PDN solution, which must provide low-impedance vertical and horizontal discharge paths through the TSVs and microbumps. A robust 3-D PDN strategy involves strategically placing decoupling capacitors and interdie rail clamps to stabilize the voltage across the stack and prevent inductive ringing during rapid ESD events. Furthermore, heterogeneous integration in 3-D systems combines dies with different voltage domains and process technologies, which increases the risk of cross-die damage during ESD events. Addressing these challenges requires both device-level and system-level co-design strategies, as well as new testing methodologies tailored for 3-D architectures.

In addition to monolithic 3-D integration, chiplet-based architectures pose similar ESD challenges. In chiplet systems, multiple dies fabricated in different technology nodes are integrated through interposers or advanced packaging. Beyond traditional silicon interposers, fan-out panel-level packaging (FOPLP) has emerged as a key technology for

heterogeneous integration, where ESD protection circuits can be integrated directly into the redistribution layer using thin-film transistors to safeguard core CMOS components [91], [92]. Such heterogeneous integration introduces diverse voltage domains and interchip interconnects that can become vulnerable discharge paths under ESD stress. Unlike traditional single-die protection, ESD design for chiplets requires coordinated strategies across chip, interposer, and package levels to ensure reliable operation.

C. SYSTEM-LEVEL ESD CONSIDERATIONS

While chip-level ESD qualification is traditionally based on HBM or CDM testing, modern electronic products must also meet stringent system-level ESD standards such as IEC 61000-4-2 [33]. At the system level, ESD events are characterized by higher peak currents and faster rise times than traditional component-level models. This discrepancy means that even a chip that passes HBM testing may fail in the actual system environment. To address this gap, the Industry Council on ESD Target Levels introduced White Paper 3, which establishes a framework for reconciling the requirements of semiconductor providers and system OEMs [93], [94], [95]. A central pillar of this framework is the system-efficient ESD design (SEED) methodology, which uses quasi-static and transient modeling to co-optimize the protection provided by the IC and the onboard components. Future directions will need to focus on co-design methodologies that integrate IC, package, and PCB-level protection strategies to ensure reliable system performance under realistic ESD stress conditions.

D. EMERGING APPLICATIONS AND RELIABILITY REQUIREMENTS

Beyond traditional computing and consumer electronics, emerging applications such as 5G communication, automotive electronics, AI accelerators, and IoT devices impose new requirements on ESD protection design. These systems often demand ultralow power consumption, broadband high-frequency performance, and stringent reliability across harsh operating environments. For example, automotive electronics require robust tolerance to IEC-level surges over extended lifetimes. Furthermore, the rise of quantum computing introduces a new frontier for ESD protection; quantum processors and their control interfaces operate at cryogenic temperatures, where traditional semiconductor physics change, and the extremely sensitive qubits can be permanently decohered or damaged by even minute ESD transients. Designing ESD solutions for quantum applications requires a careful balance between providing a low-impedance discharge path and minimizing the thermal noise and parasitic loading that could interfere with quantum state manipulation. As a result, ESD protection must evolve from a purely device-level safeguard to an application-aware design discipline, where circuit robustness, high-frequency integrity, and reliability are co-optimized for the target application domain [96].

VIII. CONCLUSION

This article has presented an overview of on-chip ESD protection. The discussion began with the fundamentals of ESD phenomena and then introduced commonly adopted protection circuits. Diode-based protection, *RC*-triggered MOS clamps, and SCR devices were explained in terms of their conduction mechanisms and coordination in providing effective discharge paths. These representative examples illustrate the essential design principles that underpin robust ESD protection in CMOS technologies. In addition, their comparative advantages highlight the tradeoffs designers must consider, such as trigger efficiency, leakage control, area overhead, and latch-up immunity. A good ESD protection strategy must also account for the operating temperature range, as thermal variations significantly shift the triggering and holding voltages of protection devices. While elevated temperatures can degrade current-handling robustness due to increased phonon scattering, they simultaneously lower the threshold for latch-up activation, narrowing the safe design window. By understanding both the physical behavior of ESD transients and the circuit-level response of protection structures, engineers can develop solutions that are not only robust but also compatible with mainstream process technologies. The insights summarized here, therefore, provide a foundation for translating device-level mechanisms into practical circuit implementations that safeguard ICs across diverse applications.

Looking ahead, continued CMOS scaling, heterogeneous 3-D integration, and chiplet-based architectures will bring new challenges for ESD protection design. At the same time, increasingly stringent system-level standards require protection solutions that extend beyond the chip itself. Future progress will depend on the development of new device concepts, circuit techniques, and co-design methodologies that balance robustness, efficiency, and compatibility with advanced semiconductor technologies. To ensure long-term reliability in environments ranging from cryogenic quantum systems to high-heat automotive electronics, a holistic design approach that considers these thermal extremes is essential. By consolidating fundamental knowledge with practical circuit perspectives, the ESD community can continue to support reliable operation in next-generation electronic systems.

ACKNOWLEDGMENT

The authors would like to thank Dr. Yun-Shiang Shu from MediaTek Inc., for his valuable suggestions during the preparation of this review article.

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