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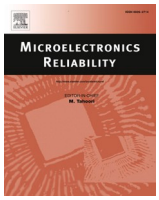

Research paper

RC-inverter-based power-rail ESD clamp circuit for monolithic GaN ICs☆

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ABSTRACT

This paper presents the design and verification of an *RC*-inverter power-rail electrostatic discharge (ESD) clamp circuit implemented in a 0.5-μm GaN-on-Si process. The proposed structure utilizes a GaN-compatible inverter composed of depletion-mode and enhancement-mode HEMTs to achieve reliable triggering behavior without transient leakage under normal power-on conditions. The SPICE simulation was conducted to verify the circuit operation under normal power-on events and ESD events. The circuit exhibits a low DC standby leakage current of 6.9 μA at a 6-V bias. The experimental results from transmission-line-pulse (TLP) measurement, very-fast TLP (VF-TLP) measurement, and human-body-model (HBM) tests confirm strong bidirectional ESD robustness. The measured TLP failure currents reach +4.8 A/ -5.8 A, while the corresponding HBM levels are +4500 V and − 5500 V. Additionally, the measured VF-TLP failure currents are +5.8 A and − 6.8 A. These results demonstrate that the proposed *RC*-inverter power-rail ESD clamp provides a robust and low-leakage solution for whole-chip ESD protection in GaN-based integrated circuits.

1. Introduction

Gallium nitride (GaN) has emerged as a promising wide-bandgap (WBG) semiconductor material owing to its outstanding physical and electrical properties, including a wide bandgap energy of 3.4 eV, a high critical electric field, and superior electron mobility. These intrinsic material advantages enable GaN-based devices to achieve higher breakdown voltage, faster switching speed, and lower conduction losses compared to conventional silicon (Si) devices. Consequently, GaN power and radio-frequency (RF) transistors have gained increasing attention for use in high-efficiency and high-density power conversion systems, electric vehicles (EVs), data centers, and low-earth-orbit satellite communication platforms.

In recent years, the development of GaN-based integrated circuits (ICs) has accelerated, extending the application of GaN from discrete devices to monolithically integrated systems. Various circuit-level demonstrations, including logic circuits [1,2] and gate-driver ICs [3–6], have shown the feasibility of integrating high-performance GaN transistors on a common substrate. However, as the integration level increases, the reliability and yield of GaN ICs during large-scale manufacturing become major concerns. Among these reliability issues, electrostatic discharge (ESD) has been identified as one of the most critical threats because ESD events can inject extremely high transient energy into the device, leading to catastrophic gate oxide breakdown, junction breakdown, or metallization melting.

To ensure product reliability, whole-chip ESD protection designs must be incorporated into GaN ICs. These protection networks are required to safely dissipate ESD energy while maintaining normal circuit operation and minimizing parasitic effects. Moreover, the ESD robustness specifications for automotive and high-power industrial systems are typically more stringent than those defined for consumer electronics, often requiring devices to withstand several kilovolts of Human-Body-Model (HBM) stress. Therefore, this study focuses on the design of a highly robust ESD protection circuit that can effectively protect GaN-based ICs.

Regarding whole-chip ESD protection, the power-rail ESD clamp circuit is an essential element to enhance ESD robustness [7]. The traditional power-rail ESD clamp circuit in the silicon process is *RC*-inverter-based, which can be referred to Fig. 1. The *RC* time constant is typically designed within 0.1 μs to 1 μs, allowing the clamp circuit to distinguish between normal power-on and ESD conditions. During normal power-on, the V_{CC} rise time is about 0.1 to 1 ms. The node V_{RC} can track the V_{CC} power. The PMOS (*Mp*) is always kept off. After the V_{CC} of the circuit system is powered to a DC steady state, the node V_{RC} will be pushed to the same voltage as V_{CC}. The PMOS (*Mp*) will be kept off, and the NMOS (*Mn*) will be turned on. The node V_G will be pulled to ground,

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