Area-Efficient ESD Clamp Circuit With a Capacitance-Boosting Technique to Minimize Standby Leakage Current

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***Abstract*—This paper presents a new RC-based power-rail electrostatic discharge (ESD) clamp circuit, which achieves ultra-low leakage current while maintaining low silicon utilization. A capacitance-boosting technique is used in conjunction with mathematical analysis of area utilization to determine the best set of parameters to achieve the smallest implementation area in silicon. The proposed power-rail ESD clamp circuit has been verified in a 65-nm general-purpose CMOS process, which achieves an ultra-low standby leakage current of 80 nA at 25 °C under 1-V bias, as well as ESD robustness of a 4-kV human body model and a 250-V machine model with a silicon area of only 45 μm $\times$ 17 μm.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection, power rail, leakage.**

I. Introduction

ELECTROSTATIC DISCHARGE (ESD) is a major reliability concern in IC industry [1]. ESD involves peak voltages of several hundred volts and peak currents of several amperes, which are discharged in few nanoseconds. Such discharges may cause serious damage to the internal structures of the IC. Therefore, special ESD protection devices and circuits are placed around the IO pads to protect the internal circuits against ESD damage. These ESD protection circuits are capable of detecting ESD and provide a safe discharge path to conduct the ESD current away from the internal circuits. Because ESD may happen between any two pins, every pin-to-pin combination of ESD stress must be protected [2].

ESD protection design becomes more challenging in the nanoscale CMOS processes. With continuous miniaturization of transistors, the MOS gate oxide has been scaled down to a few nanometers, and as consequence the gate breakdown voltage has been reduced to less than $\sim$6 volts, reducing drastically the ESD robustness and thus requiring stronger ESD protection. In addition, the thin gate oxide suffers from large tunneling current [3]–[5], thus having to take the gate leakage current into consideration on design phase [6], [7]. The gate leakage current impacts drastically in the power-rail ESD clamp circuit design, where a MOSFET is commonly used to implement the large capacitor required for ESD detection. Although the high-K materials and metal gate alleviate the gate leakage effect [8], [9], these materials have not been included in the 90-nm, 65-nm, and 40-nm CMOS processes.

Some previous works have addressed the leakage current issue on the power-rail ESD clamp circuits [10]–[14]. In [10], the leaky MOS capacitor was replaced by a MOM capacitor to reduce the leakage current at the expense of some area overhead. In [11], a capacitance coupling technique is used to reduce the area of the capacitor, but this work did not contemplate the gate current in modern CMOS processes. In [12], stacked diodes are used to reduce the voltage drop across the capacitor therefore reducing the gate leakage current. Previous work [13] is similar in concept to [12] with the difference that feedback is used to more effectively control the capacitor voltage drop and thus to further reduce the leakage current. In addition, some comparisons among the different methods to reduce the impact from gate-oxide leakage on the power-rail ESD clamp circuit were reported in [14].

II. Traditional Power-Rail ESD Clamp Circuit

The traditional power-rail ESD clamp circuit implemented with a large-sized MOSFET as the main ESD clamp was commonly used in previous CMOS technologies. Due to the large leakage current caused by thin gate oxide in the nanoscale CMOS, such realization with a large-sized MOSFET results impractical. So, the silicon controlled rectifier (SCR) was used as the main ESD clamp in the power-rail ESD clamp circuit. In addition, an SCR can sustain more ESD current with the same area than the MOSFET counterpart [15]. The traditional power-rail ESD protection circuit with SCR device as main ESD clamp is shown in Fig. 1(a). The cross-sectional view and the equivalent circuit of SCR device are shown in Fig. 1(b) and (c), respectively. The main disadvantage of SCR is the slower turn-on speed, which can be troublesome for some fast ESD transients, although some previous work had reported the SCR with improved turn-on speed by using the dummy-gate structure to block the shallow-trench-isolation (STI) formation inside the SCR device [16].

Manuscript received July 29, 2014; revised February 20, 2015; accepted February 23, 2015. Date of publication February 26, 2015; date of current version June 3, 2015. This work was supported in part by the Ministry of Science and Technology (MOST), Taiwan, under Contracts MOST 103-2221-E-009-197-MY2, MOST 103-2220-E-009-007, and MOST 103-2622-E-009-006.

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Digital Object Identifier 10.1109/TDMR.2015.2407572

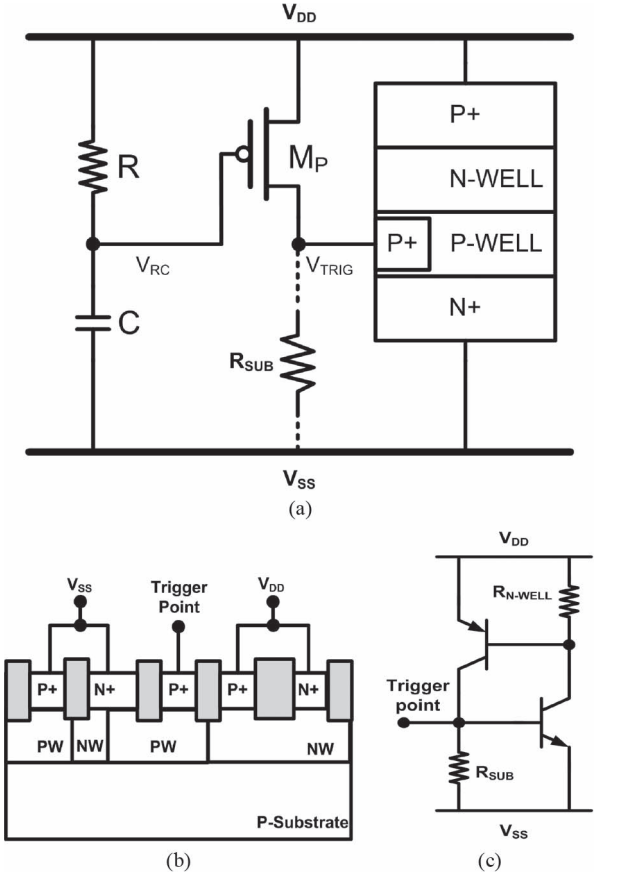

Fig. 1. (a) Traditional power-rail ESD clamp circuit using an SCR as ESD clamp. The SCR is the $\mathrm{P+/NW/PSUB/N+}$ parasitic device. $\mathrm{R_{SUB}}$ represents the SCR substrate resistance and it is used for simulation purpose. (b) The device cross-sectional view of SCR, and (c) the SCR equivalent circuit with the trigger point.

The operation of this circuit is as follows. Under an ESD-like waveform zapping at $\mathrm{V_{DD}}$ with $\mathrm{V_{SS}}$ grounded, the RC delay cannot follow up the fast rising edge of $\mathrm{V_{DD}}$, and therefore $\mathrm{V_{RC}}$ raises slower than $\mathrm{V_{DD}}$. The voltage drop in R turns $\mathrm{M_P}$ on and sends the trigger current to turn the SCR on. Under normal circuit operation, $\mathrm{V_{DD}}$ is stable at the operating voltage, thus C is charged up and $\mathrm{V_{RC}}$ should be equal to $\mathrm{V_{DD}}$. But in reality, it is slightly smaller due to the gate leakage of $\mathrm{M_P}$. If the voltage drop in R is relatively large, it could cause larger leakage current by slightly turning $\mathrm{M_P}$ on.

The traditional ESD clamp circuit has two main problems when implemented in nanoscale CMOS technologies, which are the excessive leakage current and the large implementation area. The problem lies mainly in the capacitor in the RC delay circuit for ESD detection. In order to reduce area, this capacitor was often implemented by MOS capacitor. But due to the gate leakage issue, the MOS capacitor would lead to too much large leakage current to cause circuit malfunction. Realizing the capacitor with other structures, such as junction capacitance or metal-metal capacitance (MIM or MOM), would somewhat lead to area overhead, because the capacitance-per-area ratio of these structures is much smaller than the capacitance-per-area ratio of MOS capacitor.

The area of the ESD detection circuit would be scaled up if not designed properly, so careful analysis has to be done. The parameters for the traditional RC delay are the resistor, the capacitance, and the time constant. These three parameters are related by the following equation

$$\tau = R \times C. \tag{1}$$

The time constant (τ) must be chosen as small as possible to minimize area, but also has to be large enough to detect the ESD transients. Typical Human-Body-Model (HBM) ESD event has a discharge transient with a rise time of $\sim$10 ns, so a time constant of 100 ns is an adequate choice.

To efficiently select the values for R and C, the area can be expressed as a function of these elements and then minimized.

$$A = k_C \times C + k_R \times R, \tag{2}$$

where A is the area, k_C is the capacitance-to-area constant of a given capacitor (in $\mathrm{m^2/F}$), and k_R is the resistance-to-area ratio of a given resistor (in $\mathrm{m^2/\Omega}$). These constants can be estimated from the device layouts with foundry's design rules. Replacing (1) into (2) and minimizing, the following values can be obtained

$$R = \sqrt{\frac{\tau k_C}{k_R}} \tag{3}$$

$$C = \sqrt{\frac{\tau k_R}{k_C}}. \tag{4}$$

For the CMOS process used in this work, k_C is approximately 0.25 $\mu\mathrm{m^2/fF}$ for the $\mathrm{P+/N}$-well junction. The resistor used is a poly resistor with silicide blocking and minimum length, which has the k_R of $181^{*}10^{-6}$ $\mu\mathrm{m^2/\Omega}$. Using (3) and (4) with a 100-ns time constant, the R and C values are with 370 $\mathrm{k\Omega}$ and 269 fF, respectively. Notice that if an arbitrary value was taken, the total area would be scaled up to 10-time larger than the value obtained. Therefore, the results obtained in (3) and (4) are very important.

III. Proposed Area-Efficient and Low-Leakage Power-Rail ESD Clamp Circuit

The main problem of the traditional RC delay arises from the lack of capacitor with high k_C but also low leakage current. The device with higher capacitance per area ratio is the thin-oxide MOS, but it has very large leakage current. The device with second biggest capacitance per area ratio in the given 65-nm CMOS process is the reverse-biased $\mathrm{P+/NW}$ junction, which capacitance per area ratio is only one fifth of that of the PMOS. Clearly, using the reverse-biased $\mathrm{P+/NW}$ junction as capacitor cannot yield an optimal design in silicon area consideration.

The proposed work uses a circuit technique known as capacitance boost or capacitance amplification [17]–[19], because it can effectively amplify the equivalent capacitance of a given device.

Fig. 2(a) shows an RC ESD detection circuit using the capacitance boost technique, with the current mirror composed

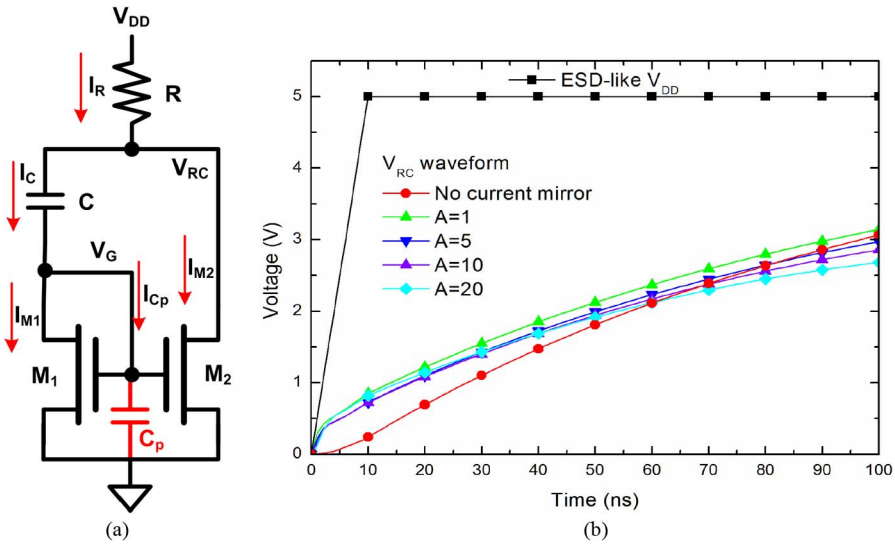

Fig. 2. (a) ESD detection circuit using the capacitance-boosting method, and (b) simulation results under a typical ESD-like waveform. Different current mirror configurations were simulated while still maintaining the same equivalent RC time constant. A is the size ratio between M_1 and M_2.

by M_1 and M_2. The analysis of the circuit is as follows. A signal applied at V_{DD} will cause a current to flow through the resistor. Some part of that current would flow through C and some part through M_2. The current flowing through C would then flow through M_1, but some part would be deflected by the parasitic capacitance of the transistor gates (C_p) at the node V_G. The total current flowing through M_1 is

$$I_{M1} = I_C - I_{Cp}. \tag{5}$$

Then,

$$\begin{aligned} I_{M1} =& C\frac{d}{dt}(V_{RC} - V_G) - C_p\frac{d}{dt}V_G \\ =& C\frac{d}{dt}V_{RC} - (C + C_p)\frac{d}{dt}V_G. \end{aligned} \tag{6}$$

The total current through R is the sum of the capacitor current plus the current through M_2, which is the equal to the current of M_1 amplified by the current mirror with a ratio of A

$$\begin{aligned} I_R =& C\frac{d}{dt}(V_{RC} - V_G) + A\left[C\frac{d}{dt}V_{RC} - (C + C_p)\frac{d}{dt}V_G\right] \\ =& (A+1)\times C\frac{d}{dt}V_{RC} - [(A+1)\times C + A\times C_p]\frac{d}{dt}V_G. \end{aligned} \tag{7}$$

The first term in (7) shows the amplification of C by a factor of $(\mathrm{A}+1)$, whereas the second term represents a deviation introduced by the non-ideal current mirror, and it mostly depends on the derivative of V_G, which in turns depends of I_{M1} following the MOS current equation. Equation (7) does not have a closed form solution, but it can be approximated for a specific application. Fig. 2(b) shows a simulation result for ESD-like waveforms using different current mirror configurations but still maintaining the same time constant (100 ns). For this, the capacitance value is reduced $\mathrm{A}+1$ times, whereas the M_1:M_2 ratio is A, and the resistor is left constant. The input

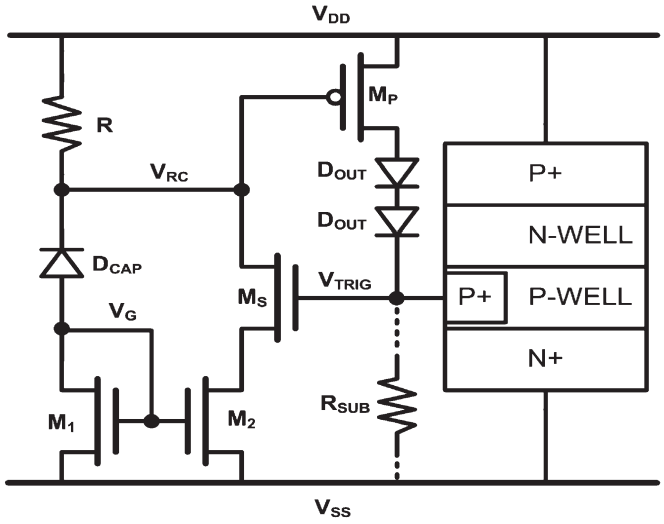

Fig. 3. Proposed power-rail ESD clamp circuit using the capacitance-boosting technique to reduce standby leakage current.

waveform is a 5-V pulse with rise time of 10 ns. A result for a traditional RC delay was also included for comparison. The current through the capacitor behaves almost linearly due to the large time constant. V_G is almost flat and then $(d/dt)V_G \approx 0$, thus the capacitance-boosting circuit behaves almost ideally, with the main difference being a small DC voltage added to the output which is caused by V_G. For practical purpose, this small difference lacks importance as V_{RC} is only used to control a PMOS transistor, and the voltage drop across R is high enough to turn M_P on for driving the required SCR trigger current. Obviously, careful analysis and design must be performed to ensure the circuit behaves as expected.

Area analysis on the circuit of Fig. 2(a) can be done following the same procedure as that for the traditional ESD detection circuit. The total area can be expressed as

$$Area = k_C \times C + k_R \times R + k_T \times (A+1). \tag{8}$$

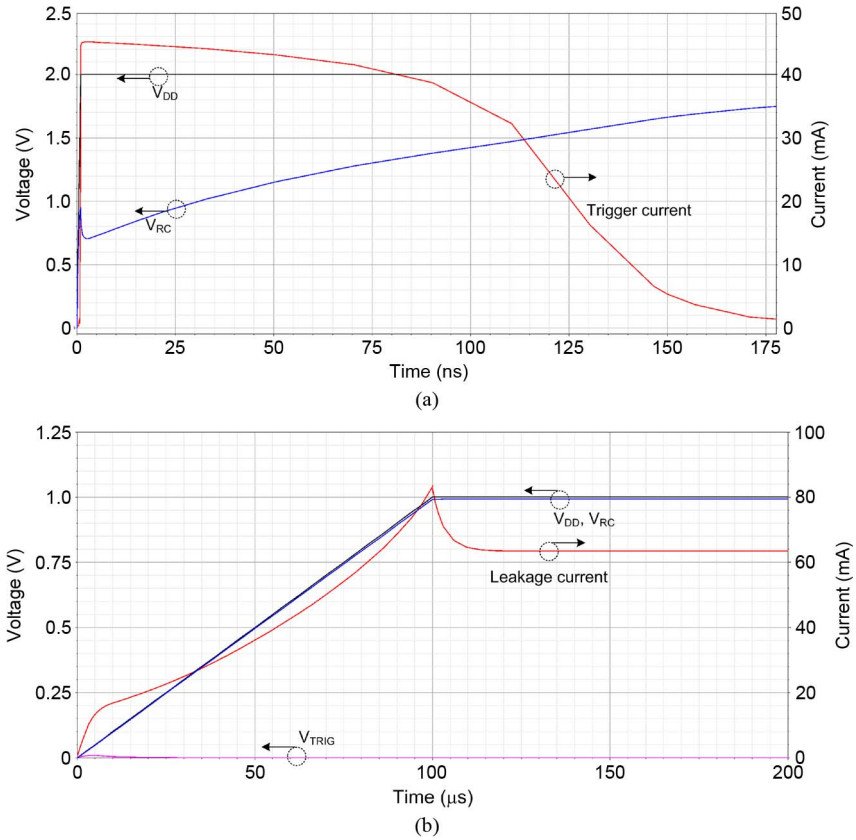

Fig. 4. Simulation results for the proposed power-rail ESD clamp circuit. (a) Simulated waveforms under ESD-like stress. The ESD-like stress is a 2-V pulse with a rise time of 1ns. (b) Simulation for normal power-on condition with 1V V_{DD} and a rise time of 100 μs.

k_C and k_R are as defined previously, k_T is the area ratio for the transistors and it has units of area, and A is the current mirror ratio. Because the current mirror amplifies the capacitance of C, the time constant is now defined as

$$\tau = R \times C \times (A + 1). \tag{9}$$

Using (8) and (9) and minimizing, the minimum area set of parameters can be found as

$$R = \sqrt[3]{\frac{k_T k_C \tau}{k_R^2}} \tag{10}$$

$$C = \sqrt[3]{\frac{k_T k_R \tau}{k_C^2}} \tag{11}$$

$$A = \sqrt[3]{\frac{k_R k_C \tau}{k_T^2}} - 1. \tag{12}$$

This set of parameters (R, C, and A) can achieve the best area-efficient RC ESD detection circuit. There is still one problem with the circuit of Fig. 2(a). Under normal circuit operation, V_{DD} is at the stable operating voltage, thus there is no current flow through the capacitor, and as a result V_G is floating. Because V_G controls M_2, the floating voltage would be sensitive to noise and causes some unexpected leakage current. In addition, any possible leakage through the capacitor would still be amplified by the current mirror as it can also be operated in sub-threshold regime. Therefore, a transistor is added in series with M_2 which acts as a switch, disconnecting M_2 during normal circuit operation and thus preventing the leakage current. In addition, this switch does not really depend on the size of M_2, it should only be large enough to prevent M_2 going into its triode region during the peak current at the beginning of the ESD. Therefore, the previously calculated area equations are still valid for the proposed circuit.

The proposed power-rail ESD clamp circuit with the area-efficient and low-leakage design is shown in Fig. 3. Transistors M_1 and M_2 form the current mirror, M_S controls the leakage current by disconnecting the current mirror under normal circuit operation, and M_P is the transistor to trigger the SCR. In addition, two forward-connected diodes (D_{OUT}) between M_P drain and V_{TRIG} are added. Previous work has shown that the output diode can effectively reduce the leakage current and increase M_P gate oxide reliability without impact in the ESD performance [20]. The selection of R and C are using the same devices as those in the traditional design. k_T is chosen as the area of M_1, which is W/L = 1 μm/60 nm. The resulting parameters are R = 78.7 kΩ, C = 55fF, and A = 22. M_P is W/L = 100 μm/60 nm, M_2 is W/L = 22 μm/60 nm, and M_S is W/L = 5 μm/60 nm. The size of each D_{OUT} is 45 μm $\times$ 1.3 μm. Simulation results under ESD-like and power-on waveforms are shown in Fig. 4. Initially when V_{DD} is rising, there is a transient period in which the feedback loop is not set because the transistors are not yet turned on. After the transient, M_P is turned on to drive the trigger current to

TABLE I
DEVICE DIMENSIONS

	TRAD (Fig. 1)	CM (Fig. 3)
D_{CAP}	20μm x 4μm	16μm x 1μm
R	370kΩ	78.7kΩ
M_1	---	1μm/60nm
M_2	---	22μm/60nm
M_S	---	5μm/60nm
M_P	100μm/60nm	100μm/60nm
D_{OUT}	---	45μm x 1.3μm
SCR	45μm x 6μm	45μm x 6μm

SCR, and the voltage drop across the SCR substrate resistance keeps M_S to be turned on. Due to the non-ideal behavior of the capacitance-boosting circuit, the trigger current drops faster than that in the traditional design, although the results are still acceptable. Under normal circuit operation, V_{RC} is kept at V_{DD} by the resistor R. M_P is turned off and V_{TRIG} is biased at V_{SS} by the substrate resistance, thus keeping M_S to be turned off. Simulation results show a leakage current of only ~60 nA under a 1V-bias at 25 °C.

IV. Circuits Layout and Test Chip

The circuits described in Figs. 1 and 3 are fabricated in a 65-nm general purpose CMOS process. M_P is designed with a dimension of $W/L = 100\ \mu m/60$ nm, and 2 output diodes are used to further reduce the leakage current, with a dimension of 45 μm × 1.3 μm. The SCR used in this work is the same for all the test circuits, with a dimension of 45 μm × 6 μm. A modified SCR with the dummy gates [16] was also used in the proposed power-rail ESD clamp circuit. Both SCR have the same anode to cathode spacing. A summary of the device dimensions in the fabricated power-rail ESD clamp circuits is listed in Table I.

The total silicon area of the traditional power-rail ESD clamp circuit is 45 μm × 18 μm. As a contrast, the same circuit previously realized by using a PMOS as capacitor and without considering the area analysis [13] has the total silicon area of 45 μm × 45 μm, which is 2.5 times bigger. The total silicon area of the proposed power-rail ESD clamp circuit is only 45 μm × 17 μm, including the output diodes.

V. Measurement Results

A. Leakage Current

Leakage current is measured on die by ultra-low leakage probes at controlled temperature, under 1-V bias. The circuit of Fig. 1 is labeled as TRAD and the circuit of Fig. 3 is labeled as CM. Measurement results are shown in Fig. 5. The traditional power-rail ESD clamp circuit shows a low leakage current at low temperature (313 nA at 25 °C), because it is implemented by a reverse biased junction (diode) as capacitor instead of a PMOS (which would have a leakage current in the order of microamperes). At high temperature, the junction leakage of the diode (D_{CAP}) increases notably and causes a voltage drop in the resistor R, which slightly turns M_P on to cause extra

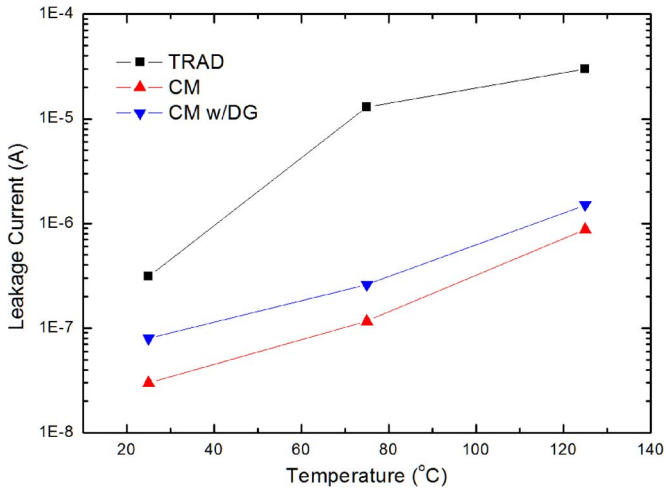

Fig. 5. Measurements of the standby leakage current under 1–V bias at different temperatures. DG stands for the dummy gates used in the SCR. The circuit of Fig. 1 is labeled as TRAD and the circuit of Fig. 3 is labeled as CM.

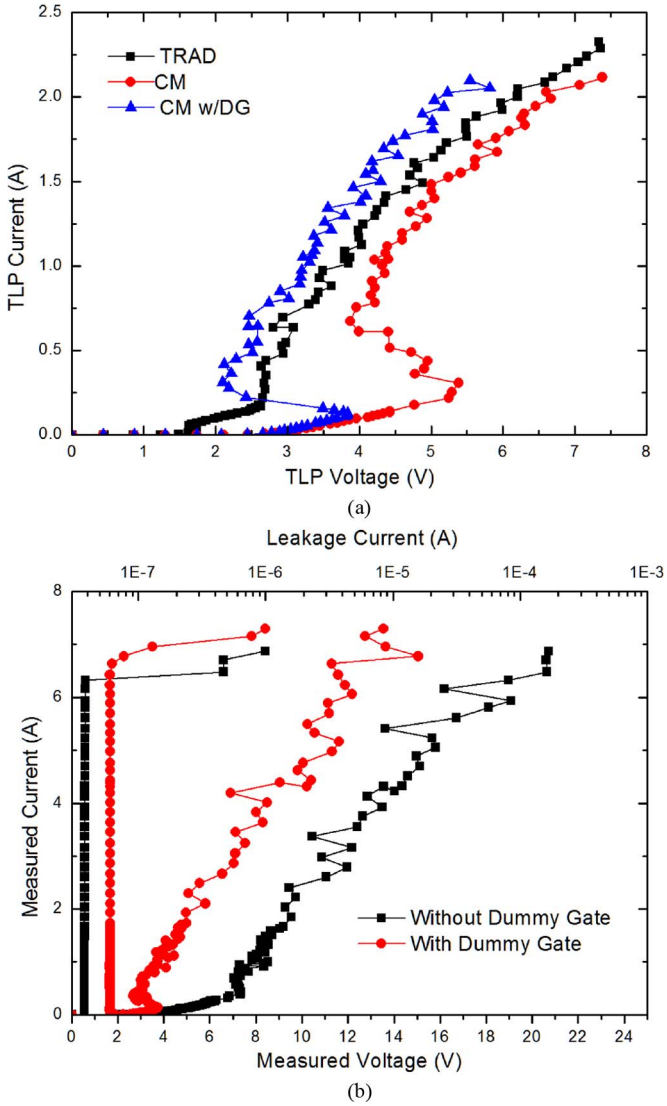

Fig. 6. (a) The TLP-measured I–V curves of the fabricated ESD clamp circuits, and (b) vf-TLP measured I–V curves for the proposed design with and without dummy gates.

TABLE II
RESULTS COMPARISON

Circuits	Leakage current (@1V bias)		ESD Level		Area	CMOS Process
	25ºC	125ºC	HBM	MM		
Ref. 10	358nA	1.91μA	4kV	350V	N/A	65-nm
Ref. 13	165nA	1.11μA	3kV	250V	45μm x 45μm	65-nm
Ref. 18	220nA	1.42μA	3.5kV	250V	50μm x 35μm	65-nm
TRAD (Fig. 1)	313nA	30μA	4kV	250V	45μm x 18μm	65-nm
This Work (Fig. 3)	**80nA**	**1.05μA**	**4kV**	**250V**	**45μm x 17μm**	**65-nm**

leakage current. The leakage current of the traditional power-rail ESD clamp circuit at 125 °C is 30 μA.

The proposed power-rail ESD clamp circuit measures 30 nA and 874 nA at 25 °C and 125 °C, respectively. The circuit using the SCR with dummy gates shows a larger leakage current as a result of the gate leakage in the dummy gates (80 nA at 25 °C and 1.05 μA at 125 °C). This extra leakage current could be further reduced if the thick gate oxide were used instead of thin gate oxide to block the STI in the SCR device.

B. TLP

TLP measurement results among the fabricated power-rail ESD clamp circuits are shown in Fig. 6(a). The traditional power-rail ESD clamp circuit does not show snapback effect, and has a holding voltage of ∼2.5 V. The proposed design presents a snapback voltage at ∼5.5 V, which is lower than the gate oxide breakdown voltage (∼6 V). When using the SCR with dummy gates, the snapback occurs at ∼4 V and the holding voltage is ∼2 V. Clearly, the dummy gates used to block the STI formation in the SCR device improve the TLP results, at the expense of little extra leakage current. The second breakdown current (I_{t2}) is ∼2.25 A for all the circuits due to the same device dimensions of the SCR used in the circuits.

A very fast TLP (vf-TLP) test was also performed with rise time of 200 ps and a pulse with of 5 ns. The vf-TLP measured I–V curves on the proposed power-rail ESD clamp circuits which were realized with/without the dummy gate on the SCR device are shown in Fig. 6(b). The proposed circuit without the dummy gates shows an apparent higher holding voltage and a slower turn-on speed. The vf-TLP test shows that the dummy gate can effectively increase the SCR turn-on speed.

C. ESD Robustness

The Human Body Model (HBM) and Machine Model (MM) ESD testers are used to verify the ESD robustness of the fabricated ESD clamp circuits. The devices are stressed with a selected ESD voltage and then the I–V curve of the device is measured and compared to the original I–V curve. A 30% deviation from the original I–V curve is considered as failure. The process is repeated with increasing stress ESD voltage until the device fails.

All the fabricated ESD clamp circuits passed the ESD stresses of HBM of 4 kV and MM of 250 V, which is consistent with the TLP-measured results. Moreover, it is expected that all the circuits should have the same ESD robustness as the only change is in the ESD detection part, whereas the trigger transistor and SCR remain the same.

A comparison among the power-rail ESD clamp circuits realized in this work and some previous works is listed in Table II.

VI. CONCLUSION

This work has demonstrated that mathematical analysis of the ESD detection circuit is very important for area-efficient design on the power-rail ESD clamp circuit. By using the area analysis and the capacitance-boosting technique to reduce the silicon area, a new power-rail ESD clamp circuit was proposed and successfully verified to achieve both of ultra-low standby leakage current and good enough ESD robustness.

ACKNOWLEDGMENT

The authors would like to thank TSMC University Shuttle Program for chip fabrication, and the TLP equipment supported from Hanwa Electronic Ind. Co., Ltd., Japan.

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