ESD Protection Design With Low-Capacitance Consideration for High-Speed/High-Frequency I/O Interfaces in Integrated Circuits

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Abstract: Electrostatic discharge (ESD) protection has been a very important reliability issue in microelectronics, especially for integrated circuits (ICs). ESD protection design for giga-Hz high-speed input/output (I/O) circuits has been one of the key challenges to implement high-speed interface circuits in CMOS technology. Conventional on-chip ESD protection circuits at the I/O pads often cause unacceptable performance degradation to high-speed I/O circuits. Therefore, ESD protection circuits must be designed with minimum negative impact to the high-speed interface circuits and to sustain high enough ESD robustness. In this paper, ESD protection design considerations for high-speed I/O circuits are addressed, and the patents related to on-chip ESD protection designs for high-speed I/O circuits are presented and discussed.

Keywords: Electrostatic discharge (ESD), input/output (I/O) interface, low capacitance (low-C), power-rail ESD clamp circuit, LC resonator, LC-tank, impedance cancellation, impedance isolation, impedance matching, distributed ESD protection scheme, substrate-triggering technique, silicon-controlled rectifier (SCR), waffle structure.

1. INTRODUCTION

With the advantages of high integration and low cost for mass production, integrated circuits (ICs) with high-speed input/output (I/O) operating in giga-Hz (GHz) frequency bands have been designed and fabricated in complementary metal-oxide-silicon (CMOS) technology. Electrostatic discharge (ESD), which can cause serious damage to IC products, must be taken into consideration during the design phase of ICs [1]-[4], including the high-speed I/O circuits. The effects of ESD induced damage in the high-speed I/O circuits had been studied, which had demonstrated that the termination resistance in the high-speed I/O circuit was changed after ESD stresses [5]. The impedance mismatch after ESD stresses causes significant waveform distortion on the I/O signals, which seriously degrades the performance of high-speed I/O circuits. Therefore, on-chip ESD protection circuits must be provided for all I/O pads in ICs. However, ESD protection circuits inevitably introduce some negative impacts to circuit performance due to the parasitic capacitance. As the operating frequency of high-speed I/O circuits increases, performance degradation due to ESD protection circuits will become more serious. On the other hand, the trigger voltage and holding voltage of ESD protection device must be designed lower than the gate-oxide breakdown voltage of metal-oxide-silicon field-effect transistor (MOSFET) to prevent the high-speed I/O circuits from damage during ESD stresses. Moreover, the turn-on resistance of ESD protection device should be minimized in order to reduce the joule heat generated in the ESD protection device during ESD stresses. As semiconductor process technology is scaled down to nanoscale, the gate-oxide breakdown voltage of MOSFET is also decreased. Typically, the gate-oxide breakdown voltage under 100-ns transmission line pulsing (TLP) stress is decreased to only ~5 V in a 90-nm CMOS technology with gate-oxide thickness of ~15 Å. However, the ESD voltages in our environment could be as high as thousands of volts. Thus, ESD protection design in nanoscale CMOS technologies has met with more challenging. To simultaneously optimize the circuit performance and ESD robustness, the high-speed I/O circuit and ESD protection circuit should be co-designed in the design phase of IC products.

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This paper presents an overview on the ESD protection designs for high-speed I/O circuits, which have been granted with U.S. patents. The design considerations on ESD protection circuits for high-speed I/O applications are discussed in Section 2. The granted U.S. patents about ESD protection designs by circuit solutions, layout solutions, and process solutions are presented and discussed in Sections 3, 4, and 5, respectively. Finally, the current and future developments, and conclusion are provided in Sections 6 and 7, respectively.

2. DESIGN CONSIDERATIONS ON ESD PROTECTION CIRCUITS FOR HIGH-SPEED I/O APPLICATIONS

2.1. Parasitic Effects of ESD Protection Devices

In order to provide enough immunity against ESD stresses, ESD protection circuits must be provided to all I/O pads in ICs, as shown in Fig. (**1**). However, the parasitic capacitance in the ESD protection circuit degrades the circuit performance of high-speed I/O. A typical request on the maximum loading capacitance of ESD protection device for a 2-GHz high-frequency input pin was specified as only ~200 fF [6]. Recently, the negative impacts of ESD protection devices to high-speed circuit performance had been investigated [7], [8], which had demonstrated that the performance of high-speed circuits is significantly degraded by the parasitic capacitance of ESD protection devices. The impact will become

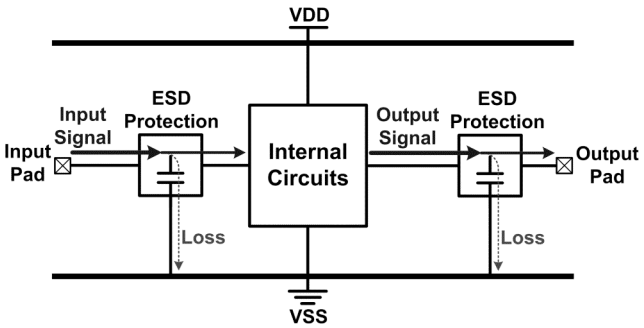

Fig. (1). The schematic to show the input pad and output pad with ESD protections in integrated circuits.

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more serious as the operating frequency of high-speed I/O circuits increases. Thus, the parasitic capacitance of ESD protection device must be minimized. Generally, ESD protection circuits cause performance degradation on high-speed I/O circuits with three undesired effects, which are the parasitic capacitive load, RC delay, and signal loss.

Parasitic capacitance is one of the most important design considerations for ICs operating in giga-Hz frequency bands. Conventional ESD protection devices with large device dimensions have the parasitic capacitance which is too large to be tolerated for giga-Hz high-speed I/O circuits. The parasitic capacitance of the ESD protection device lowers the operating speed of the high-speed I/O circuits, because it takes more time to charge or discharge the input or output nodes to the predefined level. Moreover, the parasitic capacitance of ESD protection devices causes signal loss from the pad to ground. Consequently, the signal swings of the high-speed I/O circuits are decreased.

Besides signal loss, another impact caused by the ESD protection circuit is RC delay. With the ESD protection circuit added to the input and output pads, the parasitic capacitance and parasitic resistance from the ESD protection device and the interconnects introduce RC delay to the input and output signals. Therefore, the rising and falling time of the signals at the I/O pads with ESD protection would be longer than those of the I/O pads without ESD protection. As a result, the eye closure is reduced and the intersymbol interference (ISI) is deteriorated [9].

For the analog circuits operating in giga-Hz frequency bands, which are often called as radio-frequency (RF) circuits, ESD protection circuits cause RF performance degradation on three aspects, which are noise figure, power gain, and input matching.

Noise figure is one of the most important merits for RF receivers. Since the RF receiver is a cascade of several stages, the overall noise figure of the RF receiver can be obtained in terms of the noise figure and power gain of each stage in the receiver. For example, if there are *m* stages cascaded in the RF receiver, the total noise figure of the RF receiver can be expressed as [10]

$$NF_{total} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \cdots + \frac{NF_m - 1}{A_{p1} \cdots A_{p(m-1)}} \qquad (1)$$

where NF_i and A_{pi} are the noise figure and the power gain of the *i*-th stage, respectively. According to (**1**), the noise figure contributed by the first stage is the dominant factor to the total noise figure of the RF receiver (NF_{total}). With the ESD protection circuit added at the input pad to protect the RF receiver IC against ESD damage, the ESD protection circuit becomes the first stage in the RF receiver IC. For simplicity, only the first two stages, which are the ESD protection circuit and the low-noise amplifier (LNA), are taken into consideration, as shown in Fig. (**2**). The overall noise figure (NF_{LNA_ESD}) of the LNA with ESD protection circuit is

$$NF_{LNA\_ESD} = NF_{ESD} + \frac{NF_{LNA} - 1}{L^{-1}} = L + (NF_{LNA} - 1)L = L \cdot NF_{LNA} \qquad (2)$$

where *L* is the power loss of the ESD protection circuit, and NF_{LNA} and NF_{ESD} denote the noise figures of the LNA and ESD protection circuit, respectively. Since the ESD protection circuit is a passive reciprocal network, NF_{ESD} is equal to *L*. This implies if the ESD protection circuit has 1-dB power loss, the noise figure of the LNA with ESD protection will directly increase 1 dB as well. Thus, the power loss of the ESD protection circuit must be minimized, because it has a significant increase on the total noise figure of the RF receiver. Moreover, the signal loss due to the ESD protection

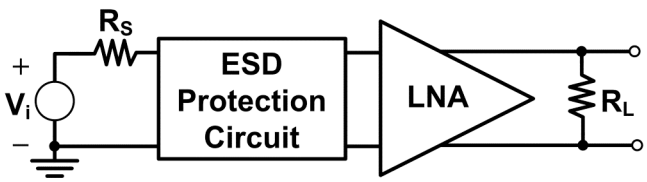


Fig. (2). The block diagram of the low-noise amplifier (LNA) with ESD protection circuit.

circuit would also cause power gain degradation in RF circuits. Another negative impact caused by the ESD protection circuit is the input impedance mis-matching, which is particularly critical for narrow band RF circuits. With the ESD protection circuit added at the input node, the original input matching condition is changed by the parasitic capacitance from the ESD protection circuit. As a result, the center frequency of the narrow band RF circuit is shifted due to impedance mismatching.

2.2. Trigger and Holding Voltages of ESD Protection Devices

To provide effective ESD protection, the voltage across the ESD protection device during ESD stresses should be carefully designed. First, the trigger voltage and holding voltage of the ESD protection device must be lower than the gate-oxide breakdown voltage of MOSFETs to prevent the internal circuit from being damaged before the ESD protection device is turned on during ESD stresses. Second, the trigger voltage and holding voltage of the ESD protection device must be higher than the power-supply voltage of the IC to prevent the ESD protection devices from being mis-triggered under normal circuit operating conditions. As semiconductor process technology is continually scaled down, the power-supply voltage is decreased, but also the gate oxide becomes much thinner. Overall, the ESD design window, defined as the difference between the gate-oxide breakdown voltage of the MOSFET and the power-supply voltage of the IC, becomes narrower in nanoscale CMOS technologies. Furthermore, ESD protection circuits need to be quickly turned on during ESD stresses in order to provide efficient discharge paths in time. Thus, ESD protection design in nanoscale CMOS technologies has suffered from more challenging.

3. ESD PROTECTION DESIGNS BY CIRCUIT SOLUTIONS

To mitigate the performance degradation due to ESD protection circuits, circuit design techniques had been used to reduce the parasitic capacitance from the ESD protection device. With the extra circuit design, the parasitic capacitance of the ESD protection device can be significantly reduced or even cancelled. Furthermore, no process modification is needed by using the circuit design techniques to reduce the parasitic capacitance. However, the silicon area may be increased due to the additional components of extra circuit design.

3.1 Conventional ESD Protection Circuits

Fig. (**3**) shows the typical on-chip ESD protection scheme in which two ESD diodes at I/O pad are co-designed with the power-rail ESD clamp circuit to prevent internal circuits from ESD damage [11, 12]. The pin combinations in ESD test are shown in Fig. (**4**), where include the ESD events of human body model [13] and machine model [14]. ESD stresses may have positive or negative voltages on an I/O pin with respect to the grounded VDD or VSS pin. For comprehensive ESD verification, the pin-to-pin ESD stress and VDD-to-VSS ESD stress had also been specified to verify the whole-chip ESD robustness. When the ESD diodes D_P and D_N are under forward-biased condition, they can provide discharge paths from I/O pad to VDD and from VSS to I/O pad,

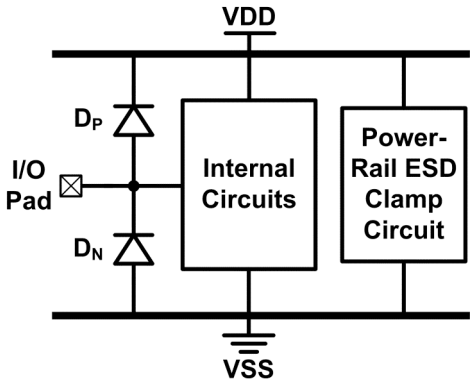


Fig. (3). The typical on-chip ESD protection scheme with ESD diodes and the power-rail ESD clamp circuit.

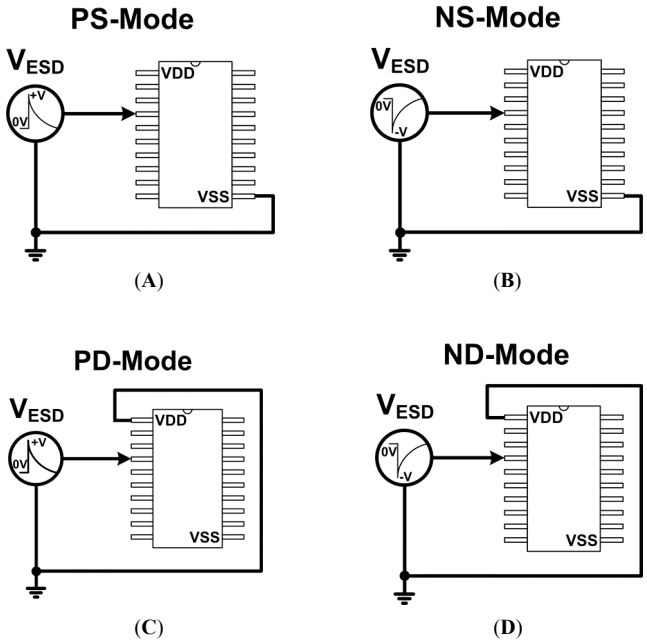


Fig. (4). The pin combinations of an IC in ESD test under the human-body-model (HBM) and machine-model (MM) (**A**) positive-to-VSS (PS) mode, (**B**) negative-to-VDD (ND) mode, (**C**) positive-to-VDD (PD) mode, and (**D**) negative-to-VDD (ND) mode ESD stresses.

respectively. The device dimensions of ESD diodes need to be reduced in order to mitigate the performance degradation due to the parasitic capacitance. During the positive-to-VDD (PD) mode and negative-to-VSS (NS) mode ESD stresses, ESD current is discharged through the forward-biased diodes D_P and D_N, respectively. To avoid the ESD diodes from being operated under breakdown condition during the positive-to-VSS (PS) mode and negative-to-VDD (ND) mode ESD stresses, which results in a substantially lower ESD robustness, the power-rail ESD clamp circuit is added between VDD and VSS to provide discharge paths between the power rails [12]. Thus, ESD current is discharged from the I/O pad through the forward-biased diode D_P to VDD, and discharged to the grounded VSS pin through the turn-on efficient power-rail ESD clamp circuit during PS-mode ESD stresses. Similarly, ESD current is discharged from the VDD pin through the turn-on efficient power-rail ESD clamp circuit and the forward-biased diode D_N to the I/O pad during ND-mode ESD stresses. Since the power-rail ESD clamp circuit is not directly connected to the I/O pad, its parasitic capacitance does not have any impact to the high-speed I/O signals. By adding the power-rail ESD clamp circuit, the ESD diodes are operated in the forward-biased condition under all ESD test modes. Thus, high enough ESD robustness can be achieved by using ESD diodes of small device dimensions to reduce the parasitic capacitance at the I/O pad.

3.2. Stacked ESD Diodes

In order to reduce the performance degradation caused by the parasitic capacitances from the ESD diodes at I/O pad, the device dimensions of ESD diodes are reduced to reduce the parasitic capacitance, while ESD robustness can be still kept by using the turn-on efficient power-rail ESD clamp circuit. However, the minimal device dimensions of ESD diodes can not be shrunk unlimitedly because ESD robustness needs to be maintained. In order to further reduce the parasitic capacitance from ESD diodes without sacrificing ESD robustness, the ESD diodes in stacked configuration had been proposed in silicon-on-insulator (SOI) processes [15, 16]. The ESD diodes formed by P-well/N-well junction in SOI processes are shown in Fig. (**5A**), Fig. (**5B**), and Fig. (**5C**), respectively. As shown in Fig. (**5A**) to Fig. (**5C**), there is a buried-oxide layer between the well regions and P-substrate, so the SOI diodes are able to be connected in stacked configuration, as

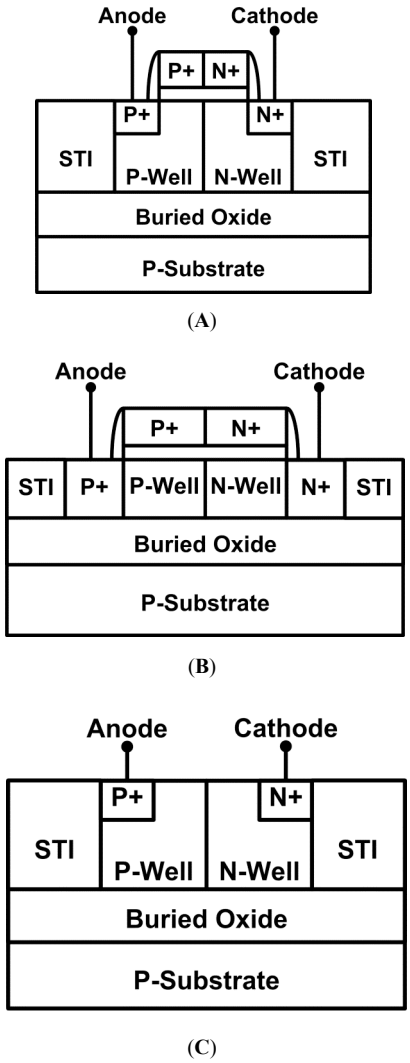


Fig. (5). The cross-sectional views of (**A**) the SOI gated diode, (**B**) the modified SOI gated diode, and (**C**) the SOI non-gated diode.

shown in Fig. (**6**). Similarly, using stacked diodes to reduce the parasitic capacitance had also been proposed in bulk CMOS processes [17, 18]. Since the total capacitance of ESD diodes in stack configuration can be significantly reduced, this technique can be used to reduce parasitic capacitance at the I/O pad with ESD protection devices. Besides reducing parasitic capacitance, the leakage current of ESD diodes under normal circuit operating conditions can be reduced by using the stacked configuration. Although stacked ESD diodes can reduce the parasitic capacitance and leakage current, the turn-on resistance and the voltage across the ESD protection devices during ESD stresses are increased by using stacked ESD diodes, which is adverse to ESD protection. In Fig. (**6**), the resistor R is added to limit ESD current flowing through the internal circuits. A gate-grounded NMOS (GGNMOS) M_n is applied to further limit the overstress voltage to the internal circuits. During PS-mode ESD stresses, M_n is operated in the snapback region to discharge ESD current. During NS-mode ESD stresses, an ESD path is formed by the bulk-to-drain junction diode in M_n.

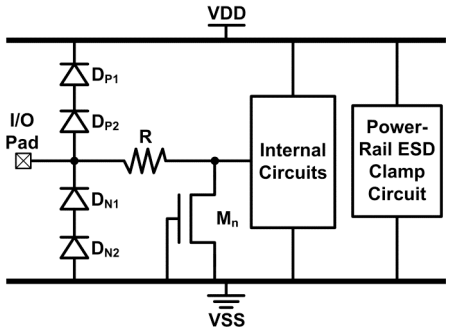


Fig. (6). The on-chip ESD protection circuit with stacked ESD diodes and power-rail ESD clamp circuit.

3.3. Impedance Cancellation

Besides stacked ESD protection devices, several ESD protection designs with inductor to reduce the parasitic capacitance of ESD protection devices had been proposed. Fig. (**7**) shows a parallel LC resonator and the simulated S_{21}-parameter under different frequencies. In a parallel LC resonator composed of the inductance *L* and capacitance *C*, the resonant frequency (ω_0) is

$$\omega_0 = \frac{1}{\sqrt{LC}} \cdot \qquad (3)$$

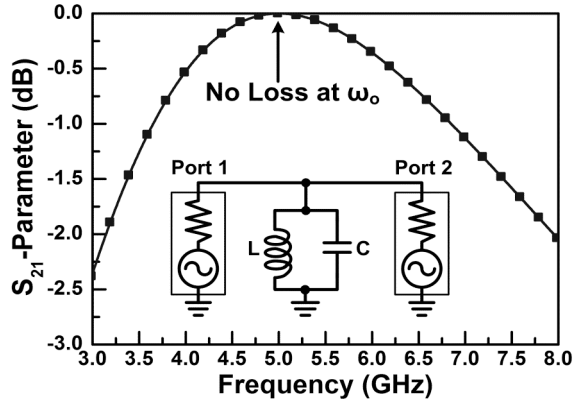


Fig. (7). The simulated S_{21}-parameter of the parallel LC resonator under different frequencies.

At the resonant frequency of the parallel LC resonator, the signal loss is ideally zero, so it was used for ESD protection design. Based on this concept, the ESD protection circuit with a parallel inductor had been proposed, as shown in Fig. (**8**) [19-23]. The inductance of L_1 was designed to resonate with the parasitic capacitance of the ESD protection device at the operating frequency of the high-speed or high-frequency I/O circuit. With the parallel LC network resonating at the operating frequency, the shunt impedance of L_1 and the ESD protection device becomes very large, which suppresses the signal loss. Therefore, the ESD protection design using impedance-cancellation technique can mitigate the impacts on circuit performance for circuit operation in a narrow frequency band. The inductor L_1 can be realized by the on-chip spiral inductor or by utilizing the bondwire in the package [19-22]. Furthermore, the inductor L_1 not only resonates with the parasitic capacitance of the ESD protection device, but also serves as an ESD protection device by itself. In this configuration, the DC biases must be equal on both ends of the inductor L_1. Otherwise, there will be steady leakage current flowing through the inductor L_1 under normal circuit operating conditions.

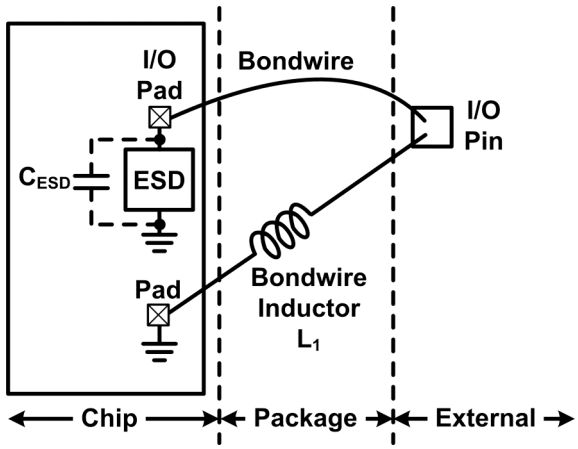


Fig. (8). The ESD protection circuit utilizing impedance-cancellation technique.

Another ESD protection design using a parallel inductor to cancel the parasitic capacitance of the ESD diode was also reported [24]. As shown in Fig. (**9**), since VDD is an equivalent AC ground node, the inductor L_P is connected between the I/O pad and VDD to form a parallel LC resonator with the ESD diode between the I/O pad and VSS. The inductor and the parasitic capacitance of the ESD diode are designed to resonate at the operating frequency of the

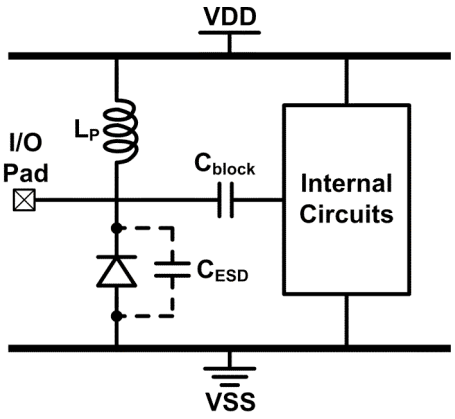


Fig. (9). The ESD protection circuit using the parallel LC network.

high-speed or high-frequency I/O circuit to minimize performance degradation caused by the ESD protection device. With an inductor directly connected between the I/O pad and VDD, the ESD diode is reverse biased with the largest possible DC voltage under normal circuit operating conditions to minimize the parasitic capacitance of the ESD diode. In this design, a DC blocking capacitor C_{block} is required to provide a separated DC bias for the internal circuits. The inductor L_P also serves as an ESD protection device to provide discharge path between I/O pad and VDD.

3.4. Impedance Isolation

Another ESD protection design for high-speed or high-frequency I/O circuits utilizing the impedance isolation technique had been proposed [25-29]. As shown in Fig. (**10**), an LC-tank, which consists of the inductor L_P and the capacitor C_1, is placed between the I/O pad and VDD. Another LC-tank consisting of the inductor L_N and the capacitor C_2 is placed between the I/O pad and VSS. The ESD diodes D_P and D_N are used to block the steady leakage current path from VDD to VSS under normal circuit operating conditions. At the resonant frequency of the LC-tank, there is an ideally infinite impedance from the signal path to the ESD diode. Consequently, the parasitic capacitances of the ESD diodes are isolated, and the impacts of the ESD diodes on high-speed circuit performance can be significantly reduced. During ESD stresses, ESD current is discharged through the inductors and the ESD diodes. With the power-rail ESD clamp circuit providing a discharge path between VDD and VSS, the ESD diodes are operated in the forward-biased condition to achieve high ESD robustness under all ESD test modes. Furthermore, the capacitors C_1 and C_2 can be directly realized with ESD diodes to provide efficient ESD paths, apart from the inductors.

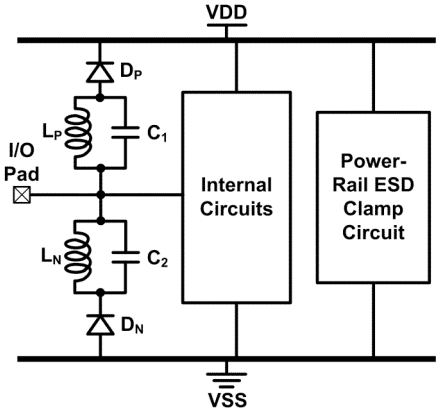


Fig. (10). The ESD protection circuit with LC-tanks.

Besides only one LC-tank, the modified design with stacked LC-tanks connected between the signal path and the ESD diode had also been proposed, as shown in Fig. (**11**) [25-28]. In Fig. (**11**), two or more LC-tanks are stacked to provide better impedance isolation at resonance, which can further mitigate the parasitic effects from the ESD diodes.

3.5. Series LC Resonator

In addition to the parallel LC resonator, the series LC resonator can also be used for broadband ESD protection design for high-speed or high-frequency I/O circuits. The simulated S_{21}-parameter of the series LC resonator under different frequencies is shown in Fig. (**12**). The resonant frequency (ω_0) is

$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad (4)$$

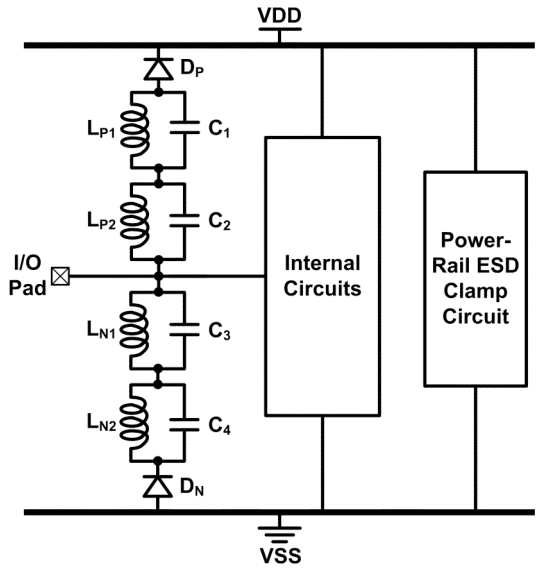


Fig. (11). The modified ESD protection circuit with stacked LC-tanks.

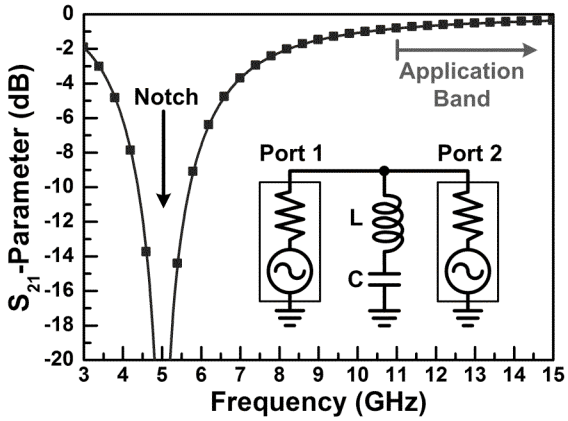


Fig. (12). The simulated S_{21}-parameter of the series LC resonator under different frequencies.

where *L* and *C* are the inductance and the capacitance in the series LC resonator. At the resonant frequency, there is a notch where the signal loss is very large. However, at frequencies above the resonant frequency, the impedance of the series LC resonator becomes inductive, so the magnitude of impedance increases (which means the signal loss is reduced) with frequency until the self-resonant frequency of the inductor is reached. Thus, ESD protection for broadband high-speed or high-frequency I/O circuits can be achieved by designing application band of the series LC resonator to cover the frequency band of the high-speed or high-frequency signals. Fig. (**13**) shows the ESD protection design proposed in [19-22], which utilizes the series LC resonator. The inductance of L_1 and the parasitic capacitance of the ESD protection device (C_{ESD}) are designed to resonate at the image frequency, which provides a very low impedance at the image frequency. Thus, the image signal can be filtered out by the notch filter formed by the inductor L_1 and the ESD protection device. The inductor L_1 can be realized either by the on-chip spiral inductor or by the bondwire.

Another design utilizing the series LC resonator is shown in Fig. (**14**) [30-32]. In Fig. (**14**), two series LC resonators are placed between the I/O pad and VSS, and between the I/O pad and VDD, respectively. In this design, ESD paths from the I/O pad to both

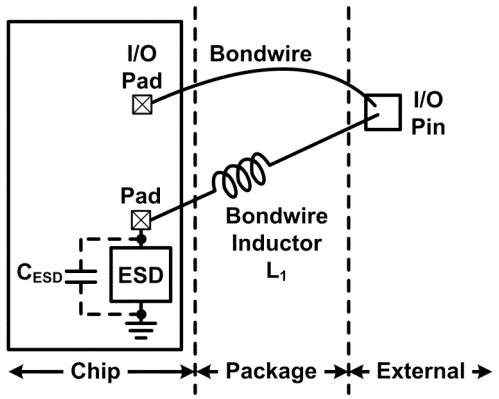


Fig. (13). The ESD protection circuit with the series LC resonator.

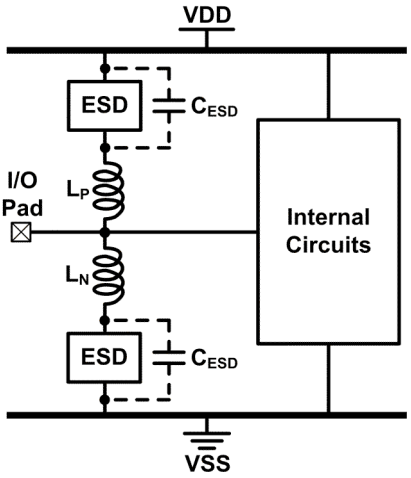


Fig. (14). The ESD protection circuit with two series LC resonators.

VDD and VSS are provided by the ESD protection devices. The modified design, which uses only one inductor connected in series with the two ESD protection devices between the inductor and VDD, and the ESD protection device between the inductor and VSS, is shown in Fig. (**15**) [30-32]. In Fig. (**15**), the capacitance in the series LC resonator is the sum of the parasitic capacitances of the two ESD protection devices. Therefore, the inductance used in Fig. (**15**) is smaller than that used in Fig. (**14**) under the same resonant frequency.

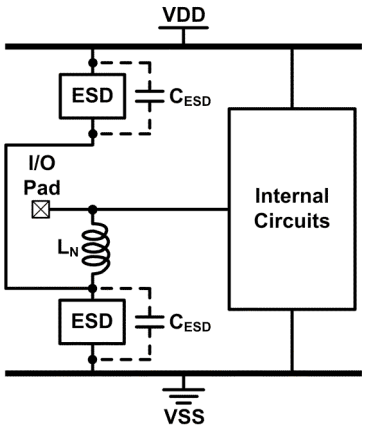


Fig. (15). The modified ESD protection circuit with only one inductor to realize the series LC resonator from the I/O pad to both VDD and VSS.

3.6. Impedance Matching

Conventionally, ESD protection devices were realized with small device dimensions to minimize the parasitic effects. However, ESD robustness would be sacrificed because the ESD protection capability declines with smaller device dimensions. To solve this dilemma, ESD protection devices are treated as a part of the impedance matching network. Thus, the ESD protection device does not need to be realized with minimal device dimensions. The technique of matching the parasitic capacitance of ESD protection device had been proposed [33-36].

In the ESD protection circuit shown in Fig. (**16**), ESD current is discharged from the I/O pad through the ESD protection devices to VDD and VSS. The combined impedance of the shunt and series impedance is designed to provide impedance matching between the high-speed or high-frequency signal and the internal circuits with ESD protection [33, 34]. Various circuit components can be used to realize the shunt and series impedance. The ESD protection design using inductance to match the parasitic capacitances of ESD protection devices is shown in Fig. (**17**) [35]. In Fig. (**17**), the ESD protection devices are placed next to the I/O pad, providing ESD protection for the IC. The transmission line (T-Line) connects the

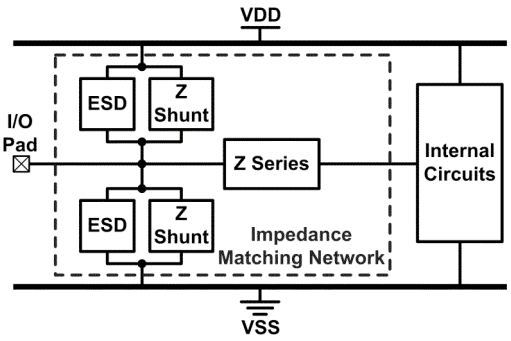


Fig. (16). The ESD protection design with the shunt and series components to achieve input impedance matching.

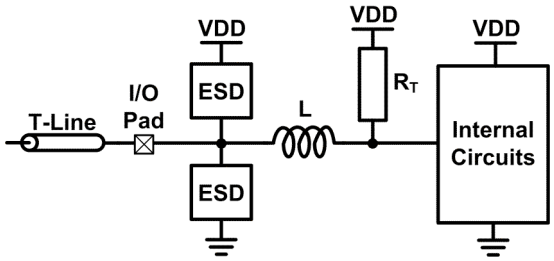


Fig. (17). The ESD protection design using the series inductor to match the parasitic capacitances.

IC and the external components. The inductive component L, which can be an inductor or a transmission line, is connected in series with the signal line, and matches the parasitic capacitances of the ESD protection devices, internal circuit, bond pad, and termination element (R_T). The small-signal circuit model is shown in Fig. (**18**), where the inductive component L separates the two parasitic capacitances C_1 and C_2. C_1 and C_2 are

$$C_1 = C_{\text{int}} + C_{RT} \qquad (5)$$

$$C_2 = C_{Pad} + C_{ESD} \qquad (6)$$

where C_{int}, C_{RT}, C_{Pad}, and C_{ESD} denote the parasitic capacitance at the input node of the internal circuit, the parasitic capacitances of

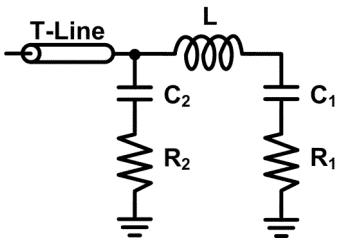


Fig. (18). The small-signal circuit model of the high-speed I/O circuit shown in Fig. (**17**).

the termination element, bond pad, and ESD protection devices, respectively. The inductance of L is designed to neutralize the reactance of the sum of C_1 and C_2 at the circuit operating frequency. Namely, the design goal is

$$X_{C1} + X_{C2} + X_L = 0 \qquad (7)$$

where X_{C1}, X_{C2}, and X_L are the reactances of C_1, C_2, and L, respectively. Once (**7**) holds, the overall input impedance matching of the high-speed or high-frequency I/O circuit with ESD protection is achieved.

Another ESD protection design with impedance matching is shown in Fig. (**19**) [36]. The capacitors C_1 and C_2 provide impedance matching with the balun, which converts the signals between single-ended and differential modes. The ESD protection devices include diodes D_1 to D_4 and inductor L_1. Under ESD stresses, the voltage corresponding to the ESD event is divided between the capacitors C_1, C_2, and C_3. The voltage across C_2 is transposed from the first winding to the second winding of the balun, and is clamped to VDD by the diodes D_3 and D_4. Besides, the diode D_1 and the inductor L_1 provide the ESD path from the I/O pad to VDD and VSS, respectively.

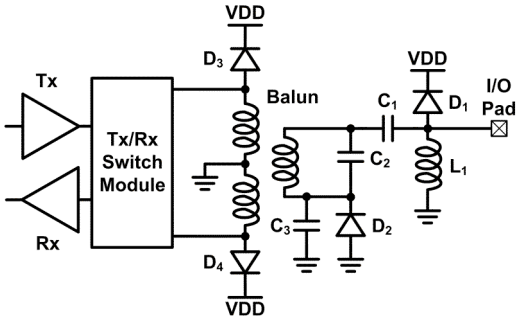


Fig. (19). The ESD protection design with a balun and the impedance matching network.

3.7. Distributed ESD Protection Scheme

In order to achieve impedance matching for broadband high-speed or high-frequency signals, the equal-size distributed ESD (ES-DESD) protection scheme had been proposed, as shown in Fig. (**20**) [37, 38]. The ESD protection devices are divided into several sections with the same device dimensions and are impedance matched by the transmission lines (T-lines) or inductors. The number of ESD protection devices can be varied to optimize the high-speed circuit performance. Each ESD protection device is connected to VDD or VSS, which is an equivalent AC ground node. The distributed ESD protection devices are impedance matched by the transmission lines under normal circuit operating conditions. With the ESD protection devices divided into small sections and

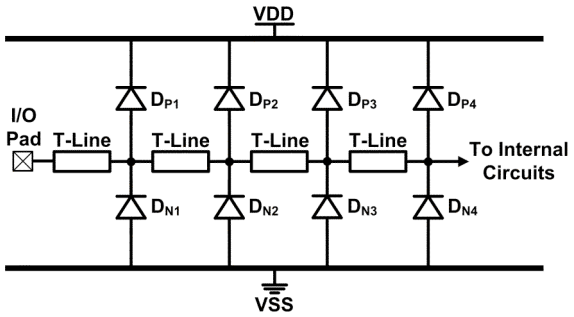


Fig. (20). The equal-size distributed ESD (ES-DESD) protection scheme.

matched by the transmission lines, such a distributed ESD protection scheme can achieve both broadband impedance matching and high ESD robustness.

To further improve ESD robustness, the modified design of decreasing-size distributed ESD (DS-DESD) protection scheme had been proposed, as shown in Fig. (**21**) [39]. The DS-DESD protection scheme allocates the ESD protection devices with decreasing sizes from the I/O pad to the internal circuit. Under the same total parasitic capacitance of the ESD protection devices, the DS-DESD protection scheme had been proven to have higher ESD robustness than that of the ES-DESD protection scheme, because the first section of the ESD protection devices in the DS-DESD protection scheme is larger than that in the ES-DESD protection scheme. With larger ESD protection devices close to the I/O pad, ESD robustness is improved. Moreover, it had been verified that good broadband impedance matching is still maintained in the distributed amplifier with the DS-DESD protection scheme [40].

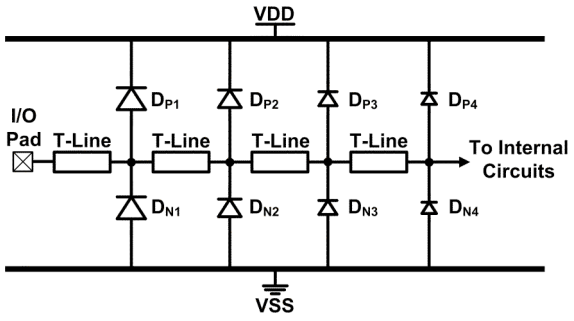


Fig. (21). The decreasing-size distributed ESD (DS-DESD) protection scheme.

Another distributed ESD protection design is the π-model distributed ESD (π-DESD) protection scheme, as shown in Fig. (**22**) [41]. Composed of one pair of ESD diodes close to the input pad, the other pair close to the internal circuits, and a transmission line matching these parasitic capacitances, the π-DESD protection scheme can also achieve both good broadband impedance matching and high ESD robustness. The first pair of the ESD diodes (D_{P1} and D_{N1}) in the π-DESD protection scheme is directly connected to the I/O pad, but the first pair of ESD protection diodes in the ES-DESD protection scheme is connected to the I/O pad through a transmission line. Therefore, the π-DESD protection scheme can sustain higher ESD robustness than that of the ES-DESD protection scheme.

3.8. Biasing Technique

In the conventional output buffers, the GGNMOS and gate-VDD PMOS (GDPMOS) are used to provide ESD protection, as

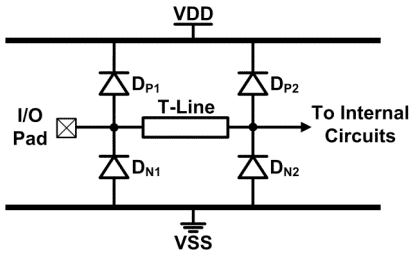


Fig. (22). The π-model distributed ESD (π-DESD) protection scheme.

shown in Fig. (**23**). The ESD protection design with an increased reverse-biased voltage across the PN junction in the ESD protection device to reduce the parasitic capacitance had been proposed, as shown in Fig. (**24**) [42]. In Fig. (**24**), the PMOS M_{P2} is used instead of the GGNMOS M_{N1} in Fig. (**23**). The four diodes D_{SP1}, D_{DP1}, D_{SP2}, and D_{DP2} denote the parasitic source-to-well and drain-to-well junction diodes in M_{P1} and M_{P2}, respectively. Since the source and gate terminals of M_{P1} and M_{P2} are at equal potentials, M_{P1} and M_{P2} are kept off under normal circuit operating conditions. During PD-mode ESD stresses, M_{P1} is turned on to discharge ESD current, and the parasitic diodes D_{DP1} and D_{SP2} are forward biased to provide ESD path from the I/O pad to VDD. During NS-mode ESD stresses, M_{P2} is turned on to discharge ESD current because the drain and source terminals of M_{P2} are exchanged, as compared with those under normal circuit operating conditions. Thus, ESD current is discharged from VSS to the I/O pad through M_{P2}. As compared with the GGNMOS, the parasitic PN-junction diodes of M_{P2} are reversed biased with larger voltages, which results in smaller parasitic junction capacitance. This is because the cathodes of the parasitic PN-junction diodes are biased to the highest potential in the circuit under normal circuit operating conditions.

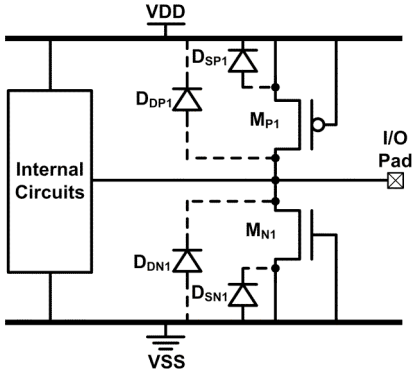


Fig. (23). The traditional ESD protection circuit with gate-grounded NMOS (GGNMOS) and gate-VDD PMOS (GDPMOS).

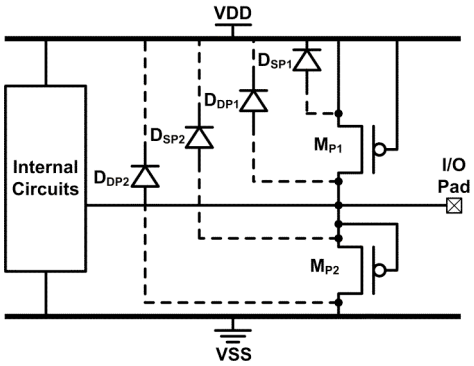


Fig. (24). The ESD protection circuit with increased reverse-bias voltage to reduce the parasitic junction capacitance.

If the voltage across a capacitor can be kept at zero, the effective capacitive loading effect can be ideally eliminated. An ESD protection design utilizing the feedback technique to reduce the parasitic capacitance had been proposed [43]. As shown in Fig. (**25**), an amplifier in unity-gain configuration is used. During PD-mode ESD stresses, the base-emitter junction diode of bipolar junction transistor (BJT) Q_1 is forward biased, so ESD current is discharged from I/O pad through Q_1 and D_1 to VDD. During NS-mode ESD stresses, ESD current is discharged from VSS through D_2 and Q_2 to I/O pad because the base-emitter junction diode of Q_2 is forward biased. Since the amplifier provides unity-gain feedback across the I/O pad and the bases of Q_1 and Q_2, ideally a zero voltage is kept across the base-emitter junction diodes of Q_1 and Q_2. Thus, the effective parasitic capacitances of the base-emitter junction diodes of Q_1 and Q_2 are ideally eliminated if the amplifier has a large enough gain.

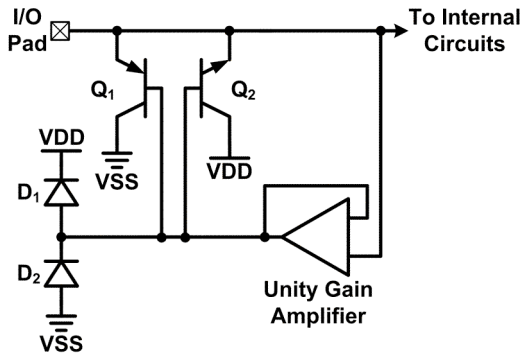


Fig. (25). The ESD protection circuit utilizing the unity-gain amplifier to reduce the parasitic capacitance.

3.9. Substrate-Triggering Technique

In Conventional ESD protection designs, the parasitic BJTs in MOSFET and silicon-controlled rectifier (SCR) are turned on when the avalanche breakdown occurs in the PN junction if no extra trigger circuit is added. Such a slow turn-on speed and high trigger voltage may not be able to protect the internal circuit against ESD stresses in time. To solve the problem, the substrate-triggering technique had been proposed to turn on the parasitic BJTs in the ESD protection devices efficiently. The substrate-triggering current is injected into the base of the parasitic BJT in the ESD protection device, which is the substrate or well region in an integrated circuit. Fig. (**26**) shows an ESD protection design utilizing the substrate-triggering technique [44, 45]. During PS-mode ESD stresses, a large current proportional to the transient voltage change flows through the MOS capacitor M_2, which can be expressed as

$$I_{M2} = C_{M2}\frac{dv}{dt} \qquad (8)$$

where I_{M2} is the current flow through MOS capacitor M_2, and C_{M2} is the capacitance of MOS capacitor M_2. The current I_{M2} boosts the gate potential of M_6, and turns on M_6. With the drain current of M_6 flowing into the bulk of M_1, the voltage across R_{well} rises. When the voltage across R_{well} exceeds the cut-in voltage of the bulk-to-source junction diode (which is the base-emitter junction diode of the parasitic BJT), the parasitic BJT in the multi-finger MOSFET M_1 is uniformly turned on and discharges ESD current. M_4 and M_5 are used to prevent M_6 from being turned on under normal circuit operating conditions. R_3 and M_7 form the secondary ESD protection circuit, which protects the internal circuit from ESD damage. In order to eliminate non-linear capacitive load on the I/O pad, which is a function of the signal voltage, the diode D_1 with a positive

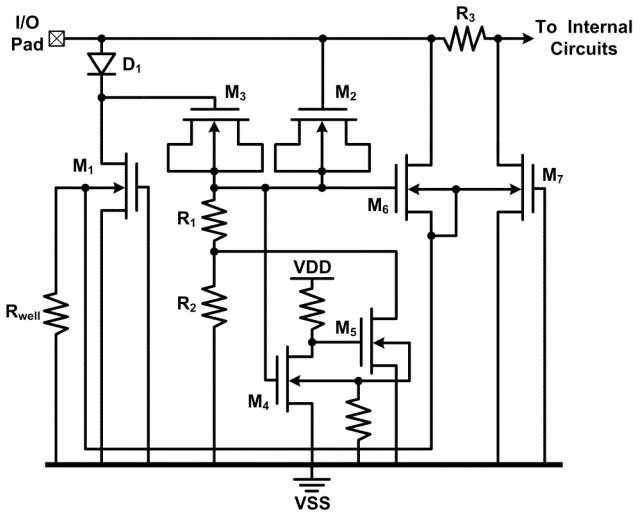


Fig. (26). The ESD protection design with the substrate-triggering circuit to turn on the ESD protection device.

coefficient, and MOSFETs M_6 and M_7 with negative voltage coefficients, can be co-designed to obtain a constant capacitive load at the I/O pad. In this design, the parasitic junction capacitance of M_1 is isolated by D_1, so the noise from substrate is significantly reduced. Moreover, adding D_1 also reduces capacitive load at the I/O pad because the parasitic capacitances of D_1 and M_1 are in series configuration.

Apart from substrate-triggered MOSFET, the whole-chip ESD protection circuit with substrate-triggered SCRs had been proposed, as shown in Fig. (**27**) [17]. The SCRs and ESD diodes are kept off under normal circuit operating conditions. Because the ESD diodes between the I/O pad and the power-rails are in series configuration, the parasitic capacitance is reduced. The stacked diodes D_{P1} and D_{P2} provide ESD protection during PD-mode ESD stresses. On the other hand, the stacked diodes D_{N1} and D_{N2} provide ESD protection during NS-mode ESD stresses. Fig. (**28**) shows the equivalent circuit of Fig. (**27**), in which the SCR is replaced by a PNP and a NPN BJT. During PS-mode ESD stresses, D_{P2}, D_{1b}, the base-emitter junction diode of the NPN BJT in SCR_1, and D_{1a} are forward biased, injecting trigger current into the NPN BJT in SCR_1. Consequently, SCR_1 is turned on, and ESD current is discharged through two current paths. The first ESD path during PS-mode ESD stresses is through D_{P2}, D_{1b}, the base-emitter junction diode of the NPN BJT in SCR_1 and D_{1a}. The second ESD path is through D_{P2}, D_{P1}, SCR_1, D_{1a}. Similarly, the base-emitter junction diode of the

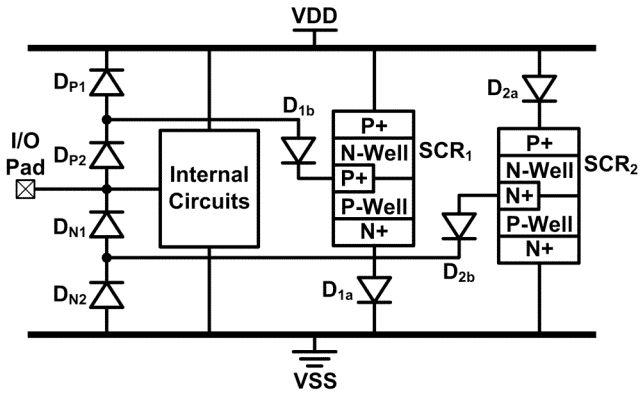


Fig. (27). The whole-chip ESD protection scheme with the substrate-triggered SCR devices and series diodes.

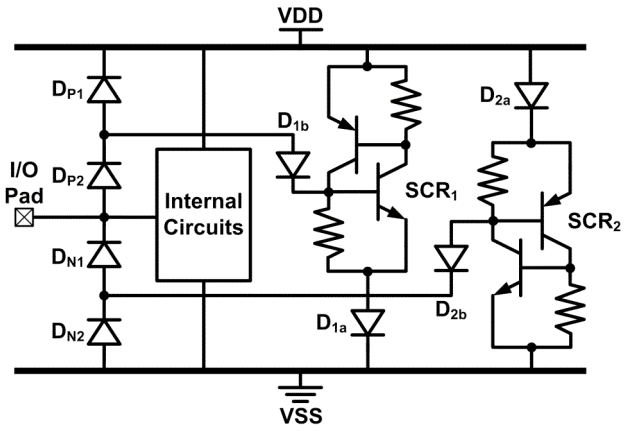


Fig. (28). The equivalent circuit of the whole-chip ESD protection scheme shown in Fig. (**27**).

PNP BJT in SCR_2 (D_{2a}), D_{2b}, and D_{N1} are forward biased during ND-mode ESD stresses, injecting trigger current into the PNP BJT in SCR_2. With the turned-on SCR_2, two discharge paths are formed during ND-mode ESD stresses. The first ESD path is through D_{2a}, the base-emitter junction diode of PNP BJT in SCR_2, D_{2b}, and D_{N1}. The second ESD path is through D_{2a}, SCR_2, D_{N2}, and D_{N1}. When the IC is under VDD-to-VSS ESD stresses, eight forward-biased diodes form the discharge path from VDD to VSS, which includes D_{2a}, the base-emitter junction diode of the PNP BJT in SCR_2, D_{2b}, D_{N1}, D_{P2}, D_{1b}, the base-emitter junction diode of the NPN BJT in SCR_1, and D_{1a}. Moreover, the series diodes D_{N2}, D_{N1}, D_{P2}, and D_{P1} form an ESD path from VSS to VDD.

4. ESD PROTECTION DESIGNS BY LAYOUT SOLUTIONS

Besides circuit solutions, layout solutions can be utilized to reduce the parasitic capacitance from the ESD protection device. By utilizing layout solutions, some silicon area can be shared to lower the fabrication cost. Furthermore, no process modification is needed and the ESD protection scheme does not need to be changed by using layout solutions.

4.1. Low-Capacitance Layout Structure for MOSFET

The layout structure for MOSFET with low parasitic capacitance had been proposed [46]. The layout top view is shown in Fig. (**29**). The P-well region is defined between the two dotted rectangles in Fig. (**29**). Fig. (**30**) shows the cross-sectional view of the low-capacitance MOSFET. The dotted line in Fig. (**30**) denotes

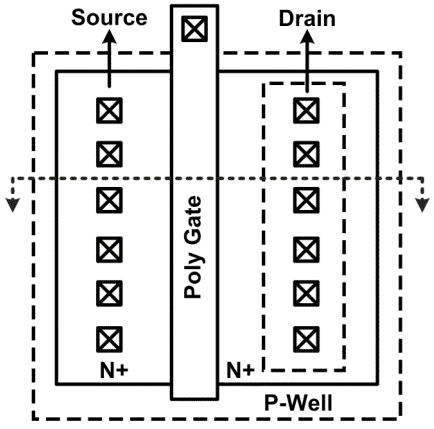


Fig. (29). The layout top view of the low-capacitance MOSFET proposed in [46].

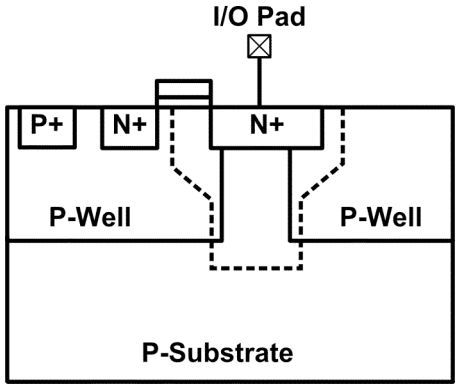


Fig. (30). The cross-sectional view of the low-capacitance MOSFET shown in Fig. (**29**).

the depletion region edge of the PN junction under the drain region. The P-well is designed not to lie below most of the drain area. Since the P-well does not exist under the drain region of the NMOS transistor, the space charge region between the N+ diffusion and the P-substrate is larger than that of the N+/P-well junction. Thus, the parasitic capacitance is reduced by eliminating the P-well from existing under the drain region. During ESD stresses, the snapback breakdown occurs in the NMOSFET, which turns on the parasitic NPN BJT in the NMOS transistor to provide ESD protection. Because of the relatively low doping level in the PN junction, the breakdown voltage of the drain-to-substrate junction is higher than that of the drain-to-well junction, resulting in degraded ESD robustness. Thus, a tradeoff exists between the parasitic capacitance and ESD robustness in this design.

4.2. Low-Capacitance Layout Structure for SCR

SCR had been demonstrated to be suitable for ESD protection design for high-frequency applications, because it has both high ESD robustness and low parasitic capacitance under a small layout area [47]. Layout structures which can reduce the parasitic capacitance of SCR had been investigated [48-51]. The layout top view and the cross-sectional view of low-capacitance SCR proposed in [48-50] are shown in Fig. (**31**) and Fig. (**32**), respectively. The SCR structure shown in Fig. (**32**) is similar to that of the low-voltage triggering SCR (LVTSCR) [52, 53]. With a low trigger

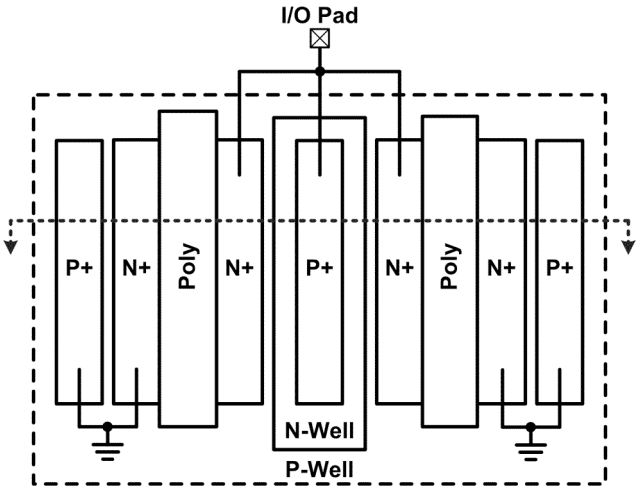


Fig. (31). The layout top view of the low-capacitance SCR proposed in [48-50].

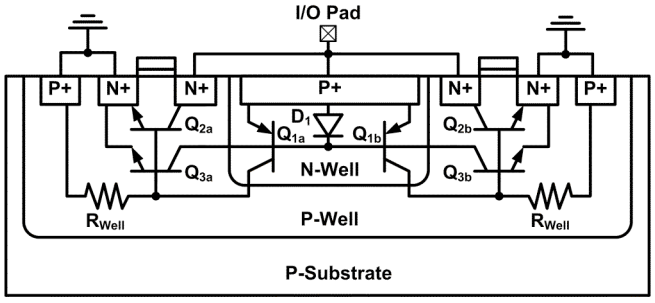


Fig. (32). The cross-sectional view of the low-capacitance SCR shown in Fig. (**31**).

voltage, the LVTSCR can provide effective ESD protection for the input stage of ICs without a secondary ESD protection circuit. Therefore, the total layout area of the ESD protection circuits with LVTSCR can be significantly saved. During PS-mode ESD stresses, the snapback breakdown occurs in the NMOS, which turns on the parasitic NPN BJT Q_{2a} (formed by the N+ diffusion, P-well, and N+ diffusion) in the NMOS. As the voltage across the P-well resistance (R_{well}) exceeds the cut-in voltage of the base-emitter junction diode in the parasitic NPN BJT Q_{3a}, which is formed by the N-well, P-well, and N+ diffusion, Q_{3a} turns on. Consequently, The SCR composed of Q_{1a} and Q_{3a} is turned on and then provides the first discharge path for ESD current. The second ESD path is provided by the other SCR composed of Q_{1b} and Q_{3b}. The ESD protection capability is doubled by splitting the current paths. The parasitic capacitance of the SCR primarily comes from the N-well/P-well junction and from the N+ diffusion (drain of the NMOS) to P-well junction. In order to reduce the parasitic capacitance, the shallow-trench isolation (STI) is utilized in the modified design [51]. As shown in Fig. (**33**), the inserted STI reduces the drain-to-well sidewall area and the N-well-to-P-well boundary area, which leads to a reduced parasitic capacitance. Because the SCR device can sustain large ESD current under a small layout area, smaller SCR dimensions can achieve the same ESD robustness as that can be achieved by larger MOSFETs. Therefore, SCR is a promising device to achieve high ESD robustness and low parasitic capacitance simultaneously.

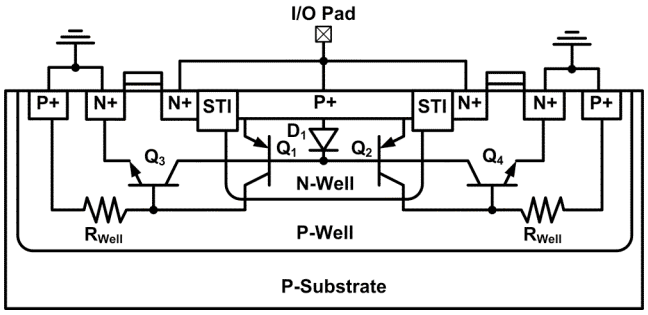


Fig. (33). The cross-sectional view of the modified low-capacitance SCR with shallow-trench isolation (STI).

Another ESD protection design utilizing the parasitic SCR is shown in Fig. (**34**) [54]. The cascoded MOSFETs M_1 and M_2 are used for mixed-voltage I/O applications, which can receive 2×VDD input signal by using only 1×VDD devices without the gate oxide-reliability issue. The diode D_1 is used to provide ESD path from the I/O pad to VDD. The cross-sectional view of the ESD protection circuit is shown in Fig. (**35**), where the MOSFETs M_1 and M_2 are

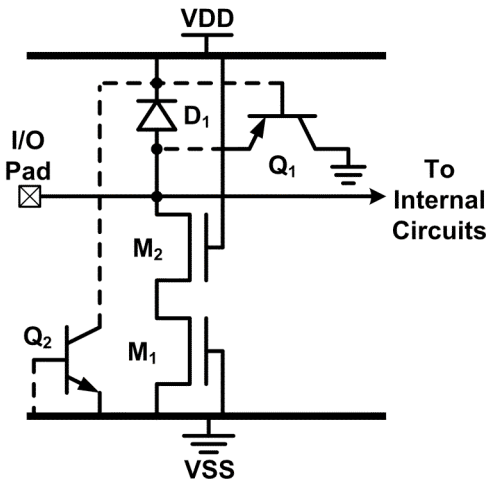


Fig. (34). The ESD protection circuit with a parasitic SCR proposed in [54].

realized with multi-finger structure. As shown in Fig. (**35**), the P+ diffusion, N-well, and P-substrate form the vertical PNP BJT Q_1, and the N-well, P-substrate, and N+ diffusion form the lateral NPN BJT Q_2. In such a layout structure, the P+ diffusion, N-well, P-substrate, and N+ diffusion form the parasitic SCR to provide ESD path between the I/O pad and VSS. Since the base terminal of Q_1 is biased to VDD, which is the highest potential in the IC, the base-emitter junction capacitance of Q_1 is reduced. Moreover, the emitter, base, and collector of Q_2 are connected to VDD or VSS, which is the equivalent AC ground node, so the parasitic capacitance of Q_2 does not have any impact to the high-speed I/O signals.

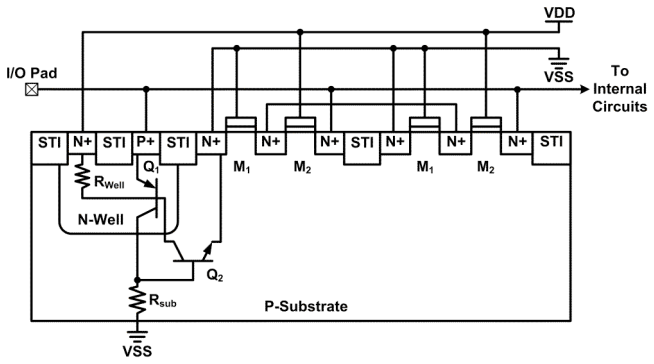
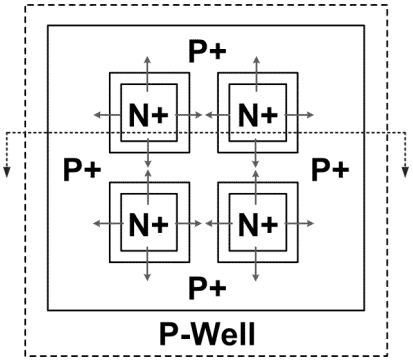


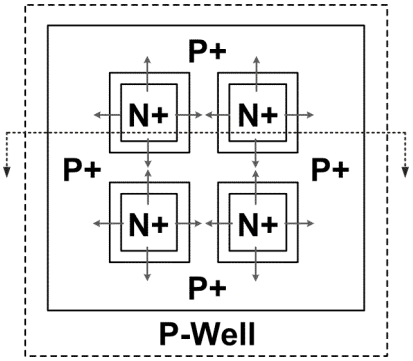
Fig. (35). The cross-sectional view of the ESD protection circuit shown in Fig. (**34**).

4.3. Waffle Layout Structure

To save the silicon area and reduce the parasitic capacitance, the MOSFETs realized with the waffle structure had been studied [55, 56]. Similarly, some ESD protection devices had been realized with the waffle structure to optimize ESD robustness. The ESD diode with the maximum ratio of perimeter to area is preferred, because it has the maximum ratio of ESD robustness to parasitic capacitance. The ESD diode realized with the waffle structure had been proposed [57, 58]. To maximize the ratio of perimeter to area, small square diffusions are used. The layout top views and cross-sectional views of the P+/N-well and N+/P-well waffle diodes are shown in Fig. (**36**) and Fig. (**37**), respectively. For the P+/N-well diode, the P+ diffusion is implemented in the N-well region and surrounded by the N+ diffusion. Thus, ESD current can be discharged through four directions of the P+ diffusion. To scale the

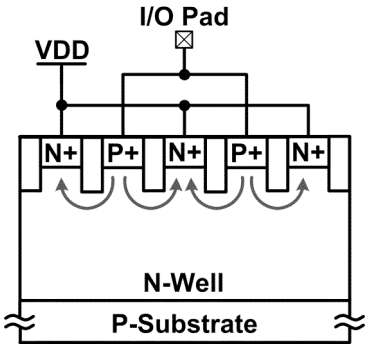


(**A**)

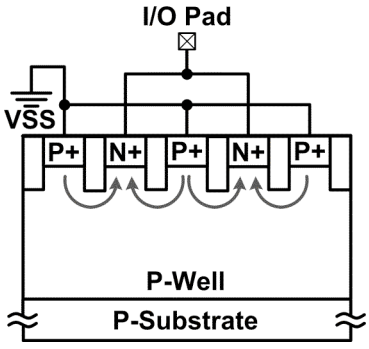


(**B**)

Fig. (36). The layout top views of the (**A**) P+/N-well and (**B**) N+/P-well waffle diodes.



(**A**)



(**B**)

Fig. (37). The cross-sectional views of the (**A**) P+/N-well and (**B**) N+/P-well waffle diodes.

high-current capability, multiple P+ diffusions are connected in parallel to form the waffle diode structure. As shown in Fig. (**37**), the ESD paths is increased in the waffle diode. Under the same ESD robustness, the waffle diode has the reduced parasitic capacitance than that of the traditional ESD diode.

4.4. ESD Protection Circuit under Bond Pad

For the sake of reducing the chip area, ESD protection circuits can be placed under the bond pad, as shown in Fig. (**38**) [59]. The contacts in Fig. (**38**) connect the diffusion regions to the bond pad. Fig. (**39**) shows the schematic circuit diagram, which can be used to illustrate the operation mechanism of the ESD protection circuit under the bond pad. The parasitic diodes D_1 and D_2 provide ESD protection during PD-mode and NS-mode ESD stresses, respectively. During PS-mode ESD stresses, the BJTs Q_3 and Q_4 can be turned on when breakdown occurs in the reverse-biased base-collector junction. After either Q_3 or Q_4 is turned on, the SCR formed by Q_3 and Q_4 is turned on to discharge ESD current. Similarly, the SCR composed of Q_1 and Q_2 is turned on during ND-mode ESD stresses to provide ESD protection. With the ESD protection circuit under the bond pad, the parasitic capacitances of the bond pad and ESD protection circuit are series connected from the I/O pad to substrate, resulting in a reduced parasitic capacitance. Thus, the total parasitic capacitance of the bond pad and ESD protection circuit is reduced, as compared with the ESD protection circuit placed beside the bond pad.

Another ESD protection circuit under the bond pad had been proposed, with its layout top view shown in Fig. (**40**) [60]. Fig. (**41**) shows the schematic circuit diagram. The diode D_1 is formed by the P-well/N-well junction. The PNP BJT Q_1 is formed by the P+ diffusion, N-well and P-well, and the NPN BJT Q_2 is formed by the

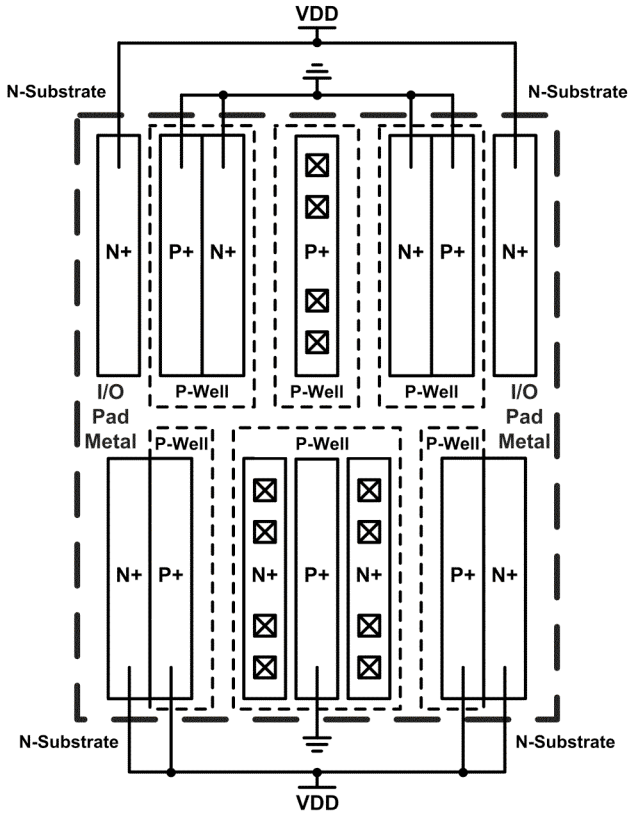


Fig. (38). The layout top view of the ESD protection circuit under the bond pad proposed in [59].

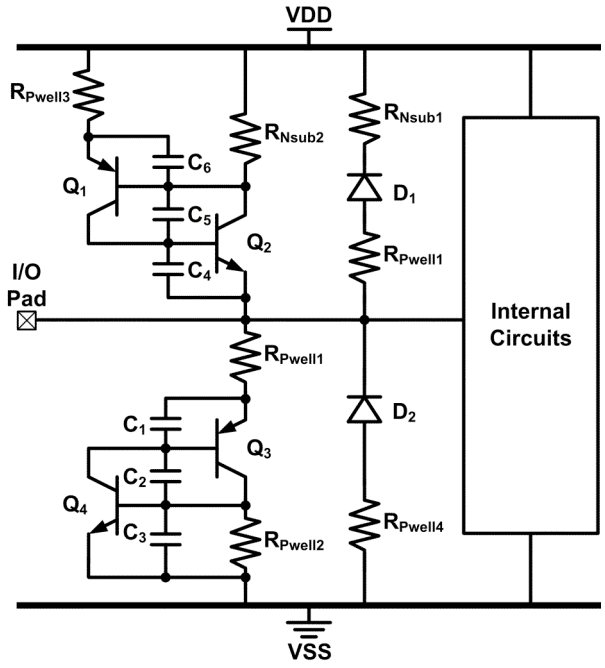


Fig. (39). The schematic circuit diagram of the ESD protection circuit shown in Fig. (**38**).

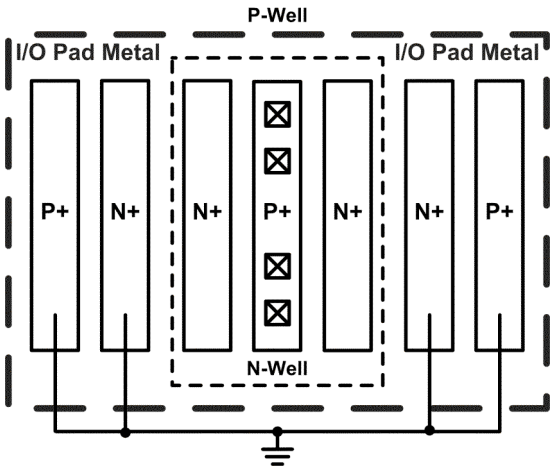


Fig. (40). The layout top view of the ESD protection circuit under the bond pad proposed in [60].

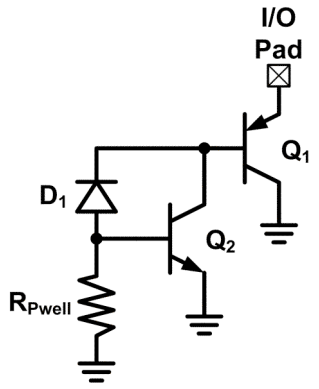


Fig. (41). The schematic circuit diagram of the ESD protection circuit shown in Fig. (**40**).

N-well, P-well, and N+ diffusion. Q_1 and Q_2 form a SCR from the I/O pad to VSS. During PS-mode ESD stresses, the junction breakdown in D_1 occurs, which turns on the SCR to discharge ESD current. In the ESD protection circuit, the parasitic capacitance is reduced, because the capacitance connected to the I/O pad is only the P+/N-well junction capacitance, which is the base-emitter junction capacitance of Q_1. Moreover, the parasitic capacitance from the I/O pad to the grounded P-well region is reduced because the ESD protection circuit is placed under the bond pad.

5. ESD PROTECTION DESIGNS BY PROCESS SOLUTIONS

The third approach to reduce the parasitic capacitance from the ESD protection device is to modify the fabrication process. Besides standard CMOS processes, ESD protection devices fabricated in some modified processes had been reported to reduce the parasitic capacitance. However, chip fabrication cost will be increased because of process modification.

5.1. Symmetrical SCR Structure

Fig. (**42**) shows the cross-sectional view of the ESD protection design in the process with the N+ buried layer and P- layer [61]. The ESD protection design has two symmetrical SCR devices. With the high-concentration N+ buried layer, the clamp voltage of the ESD protection device is reduced, which leads to more efficient ESD protection. Moreover, the deep-trench isolation separates the symmetrical SCR structure from the internal circuit, which is beneficial for latchup prevention. In the ESD protection circuit, the anode and cathode sides are junction-isolated, which reduces the parasitic capacitance. The overall reduction in parasitic capacitance is due to its smaller junction area and the series connected parasitic capacitances of the two P-well/N+ buried layer junctions. Fig. (**43**) shows the schematic circuit diagram of this ESD protection circuit, in which the anode is connect to the I/O pad, and the cathode is connected to VSS. The P-well_1, N+ buried layer, P-well_2, and N+ diffusion form the first SCR from anode to cathode. The P-well_2, N+ buried layer, P-well_1, and N+ diffusion form the second SCR from cathode to anode. The N+ diffusion which is connected to anode, P-well_1, and N+ buried layer form the NPN BJT Q_4. The N+ diffusion which is connected to cathode, P-well_2, and N+ buried layer form the NPN BJT Q_2. The N+ buried layer and N-well form the base of the BJT Q_1, and the P-well_1 and P-well_2 form the emitter and collector of the BJT Q_1, respectively. The first vertical BJT Q_5 is formed by the P- layer, N+ buried layer, and P-well_1. The second vertical BJT Q_3 is formed by the P- layer, N+ buried layer, and P-well_2. During PS-mode ESD stresses, The avalanche breakdown occurs at the N+ buried layer/ P-well_2 junction in Q_1, increasing current through Q_1. As current flows through the parasitic resistance in P-well_2 (R_{Pwell_2}), the voltage

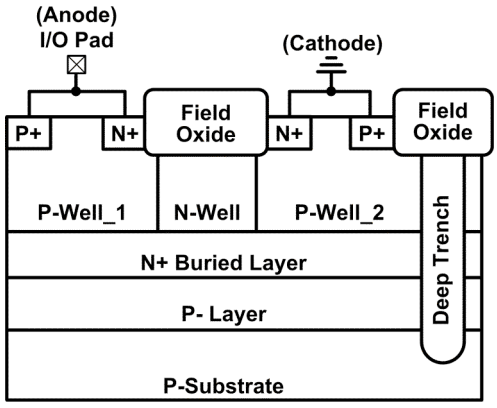


Fig. (42). The cross-sectional view of the ESD protection circuit with the symmetrical SCR structure.

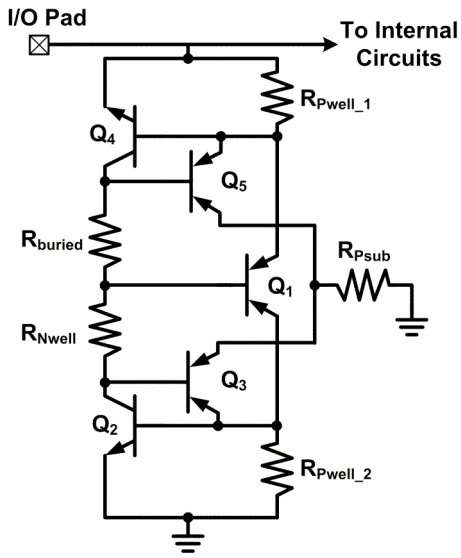


Fig. (43). The schematic circuit diagram of the ESD protection circuit shown in Fig. (**42**).

across the base-emitter junction of Q_2 increases. When the voltage across the base-emitter junction of Q_2 exceeds the cut-in voltage, Q_2 turns on, and the SCR composed of Q_1 and Q_2 is turned on to discharge ESD current. Similarly, the SCR composed of Q_1 and Q_4 is turned on to discharge ESD current during NS-mode ESD stresses.

5.2. Low-Capacitance MOSFET

In section 4.1, it has been mentioned that the parasitic capacitance can be reduced by lowering the concentration of the PN junction. The similar idea using an extra mask to lower the concentration at the drain-to-well junction had been proposed [62]. The cross-sectional view of the low-capacitance PMOS transistor is shown in Fig. (**44**). The drain and source regions are surrounded by the lightly-doped P-type (P-) regions. The N- region under the drain is counter-doped with P-type material to reduce the effective N-type concentration. Since the depletion region of the P+/N- junction is larger than that of the P+/N-well junction, the parasitic capacitance is reduced. The PMOS transistor is turned on to discharge ESD current under PD mode ESD stresses.

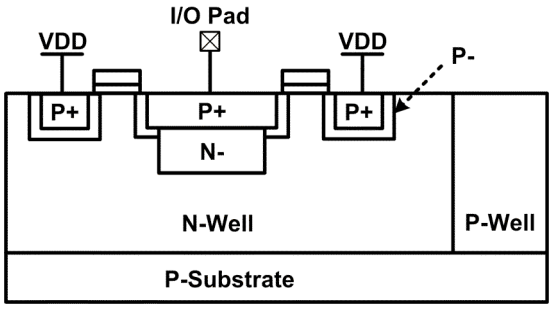


Fig. (44). The cross-sectional view of the PMOS with low parasitic capacitance proposed in [62].

6. CURRENT & FUTURE DEVELOPMENTS

As the operating frequencies of the high-speed or high-frequency I/O circuits enter the giga-Hz frequency bands, the specification on the maximum loading capacitance is decreased.

Therefore, the traditional ESD protection design flow, which directly attaches the ESD protection circuit to the I/O pads after finishing the design of the internal circuit, is not feasible anymore. This is because the giga-Hz high-speed or high-frequency I/O circuit is very sensitive to the capacitive loading effect from the ESD protection circuit. A negligible parasitic effect in the conventional IC may be the critical element which deteriorates the circuit performance of the high-speed or high-frequency I/O circuit. The solutions to ESD protection design for high-speed or high-frequency I/O circuits have been overviewed in the previous sections.

The comparison among various ESD protection designs for high-speed or high-frequency I/O circuits has been summarized in Table (**1**). The evaluated parameters are explained as following.

- Design complexity:
  - "low": The stand-alone ESD protection device is the ESD protection circuit without extra auxiliary component.
  - "moderate": The stand-alone ESD protection device is the ESD protection circuit without extra auxiliary component, but the layout of the ESD protection device needs careful consideration.
  - "high": Besides the ESD protection device, extra auxiliary components are needed, and the auxiliary components should be carefully designed.
- Parasitic capacitance:
  - "small": The parasitic capacitance of the ESD protection circuit at the I/O pad can be very small with proper design.
  - "moderate": The parasitic capacitance of the ESD protection circuit at the I/O pad is moderate for high-speed or high-frequency I/O applications.
  - "large": The parasitic capacitance of the ESD protection circuit at the I/O pad is large for high-speed or high-frequency I/O applications.
- ESD robustness:
  - "poor": ESD robustness of the ESD protection circuit is poor.
  - "moderate": ESD robustness of the ESD protection circuit is moderate.
  - "good": ESD robustness of the ESD protection circuit is good.
  - "adjustable": For some ESD protection designs by circuit solutions, ESD robustness can be adjusted by using different ESD protection devices.
- Area efficiency:
  - "poor": The area efficiency of the ESD protection circuit is poor.
  - "moderate": The area efficiency of the ESD protection circuit is moderate.
  - "good": The area efficiency of the ESD protection circuit is good.

According to Table (**1**), most ESD protection designs utilize circuit solutions to mitigate the impacts caused by the ESD protection circuit. By utilizing the circuit solutions, the ESD protection device can be realized with large device dimensions, because the parasitic capacitance from the ESD protection device can be compensated or cancelled. However, circuit solutions often use additional components. As a result, the chip area is increased, which in turn increases the fabrication cost. Moreover, characteristics of the ESD protection device and the additional components need to be carefully investigated to minimize the undesired effects.

Among the ESD protection devices, SCR is a promising device because it has both high ESD robustness and low parasitic capacitance under a small layout area. Besides, the holding voltage and turn-on resistance of SCR are quite low. As the power-supply voltage of ICs decreases, the latchup issue is avoided. These factors reveal the advantages of SCR devices. With suitable trigger circuit to enhance the turn-on speed and to reduce the trigger voltage, SCR

Table 1. Comparison Among the ESD Protection Designs for High-Speed or High-Frequency I/O Circuits

ESD Protection Designs for High-Speed or High-Frequency I/O Circuits		Design Complexity	Parasitic Capacitance	ESD Robustness	Area Efficiency
Circuit Solutions	Stacked ESD Diodes [15-19]	low	moderate	moderate	good
	Impedance Cancellation [19-24]	high	small	adjustable	poor
	Impedance Isolation [25-29]	high	small	adjustable	poor
	Series LC Resonator [19-22], [30-32]	high	small	adjustable	poor
	Impedance Matching [33-36]	high	small	adjustable	poor
	Distributed ESD Protection Scheme [37-41]	high	small	moderate	poor
	Biasing Technique [42, 43]	low	large	poor	moderate
	Substrate-Triggering Technique [16], [44, 45]	high	moderate	moderate	good
Layout Solutions	Low-Capacitance Layout Structure for MOSFET [46]	moderate	large	poor	moderate
	Low-Capacitance Layout Structure for SCR [48-51]	moderate	moderate	good	good
	Waffle Layout Structure [57, 58]	moderate	moderate	moderate	good
	ESD Protection Circuit under Bond Pad [59, 60]	moderate	moderate	moderate	good
Process Solutions	Symmetrical SCR [61]	low	small	good	good
	Low-Capacitance MOSFET [62]	low	large	poor	moderate

could be the most promising component for high-speed or high-frequency I/O ESD protection in the future.

7. CONCLUSION

A comprehensive overview on the recent patents in the field of ESD protection design for high-speed or high-frequency I/O circuits has been presented. The requirements on ESD protection design for high-speed/high-frequency I/O circuits include low parasitic capacitance, low loss, and high ESD robustness. To optimize both high-speed circuit performance and high enough ESD robustness simultaneously, the undesired parasitic effects from ESD protection devices must be minimized or cancelled. Furthermore, the ESD protection circuits and high-speed I/O circuits should be co-designed to achieve both good circuit performance and high ESD robustness. As the operating frequencies of ICs are further increased, on-chip ESD protection design for high-speed/high-frequency I/O applications will continuously be an important design task.

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