PAPER MOS-Bounded Diodes for On-Chip ESD Protection in Deep Submicron CMOS Process

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SUMMARY New diode structures without the field-oxide boundary across the p/n junction for ESD protection are proposed. A NMOS (PMOS) is especially inserted into the diode structure to form the NMOS-bounded (PMOS-bounded) diode, which is used to block the field oxide isolation across the p/n junction in the diode structure. The proposed N(P)MOS-bounded diodes can provide more efficient ESD protection to the internal circuits, as compared to the other diode structures. The N(P)MOS-bounded diodes can be used in the I/O ESD protection circuits, power-rail ESD clamp circuits, and the ESD conduction cells between the separated power lines. From the experimental results, the human-body-model ESD level of ESD protection circuit with the proposed N(P)MOS-bounded diodes is greater than 8 kV in a 0.35- μ m CMOS process.

key words: electrostatic discharge (ESD), diode, poly-bounded diode, MOS-bounded diode, ESD protection

1. Introduction

To scale down device dimension, the shallower junction depth, much thinner gate oxide, salicided (self-aligned silicide) process, and LDD (lightly-doped drain) structure had been widely used in deep submicron CMOS technology. But, those advanced process technologies result in the CMOS integrated circuits more susceptible to electrostatic discharge (ESD) damage [1]–[3]. To sustain a reasonable ESD stress (typically, $\pm 2 \text{ kV}$ in the human-body-model ESD event [4]) for safe mass production, on-chip ESD protection circuits have to be added into the IC products. The typical ESD protection circuit with double diodes for a pad is shown in Fig. 1 [5]. To avoid unexpected ESD damage in the internal circuits of CMOS ICs, the power-rail ESD clamp circuit must be placed between the VDD and VSS power lines [6]. The ESD current at the input pad under the positive-to-VSS (PS-mode) ESD stress condition can be discharged through the forward-biased P-type diode (Dp) and the VDD-to-VSS ESD clamp circuit to ground. However, if the turn-on resistance of the power-rail ESD clamp circuit is too high or the device dimension of P-type diode is drawn too small, the overshooting voltage on the input pad could be so high to cause the reverse-biased junction breakdown on the N-type diode (Dn). Therefore, the diodes under both

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VDD Dp Dp Internal Circuits VSS

Fig. 1 The typical ESD protection design with double diodes for an input pad.



Fig. 2 The pull-down weakest point at the boundary between the fieldoxide shallow-trench isolation (STI) and the diffusion edge of the diode structure [7].

forward-biased and reverse-biased stress conditions are important concerns of providing efficient ESD protection to the internal circuits.

When the diodes are stressed by the ESD pulse under the reverse-biased stress conditions, which are the positiveto-VSS (PS-mode) ESD stress for N-type diode and the negative-to-VDD (ND-mode) ESD stress for P-type diode, the diffusion boundary to the field-oxide isolation is easily damaged by ESD to cause a very low ESD robustness [7]. The weakest point at the boundary between the field-oxide shallow-trench isolation (STI) and the diffusion edge of the diode structure is illustrated in Fig. 2, where the field-oxide region near to the P+ diffusion has a pull-down structure. When the p/n junction is reverse biased during ESD stress, the breakdown point is located at the boundary between the P+ diffusion and field-oxide region. Due to the limited area of the boundary for heat dissipation, this pull-down structure on the field-oxide boundary often causes the P+ diffusion having a lower ESD robustness on its diffusion edge. If the CMOS process has the silicided diffusion, the silicided layer covered on the P+ diffusion causes a bend-down

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corner at the boundary between the P+ diffusion and fieldoxide region [7], [8]. This bend-down corner further causes the diode being more easily damaged by ESD. Thus, the ESD protection circuits formed by double diodes often have lower ESD robustness in the reverse-biased ESD-stress conditions (PS-mode and ND-mode ESD stresses), even if the diodes have been drawn with larger silicon area.

In this paper, new diode structures, called as NMOSbounded diode and PMOS-bounded diode, are proposed to significantly improve ESD robustness of CMOS ICs in deep-submicron CMOS processes [9], [10]. With the new proposed diode structures, the on-chip ESD protection circuits for input, output, and power pads have been designed and practically verified in a 0.35- μ m CMOS process.

2. Diode Structures

2.1 Normal Diodes

The cross-sectional view of the normal N-type diode realized in a deep submicron CMOS process is shown in Fig. 3. For the normal N-type diode, N+ diffusion (as the cathode) is placed in a P-well in P-substrate to form the p/n junction of the diode. The anode of such an N-type diode is connected out by the P+ diffusion in the P-well (or p-substrate). Between the P+ and N+ diffusions, there is the field-oxide region to isolate these two diffusions. For the normal P-type diode, P+ diffusion (as the anode) is placed in an N-well to form the p/n junction of the diode. The cathode of such a P-type diode is connected out by the N+ diffusion in the Nwell. Between the P+ and N+ diffusions, there is the fieldoxide region to isolate these two diffusions.

2.2 Poly-Bounded Diodes

To overcome the weakest ESD-damaged location at the p/n junction diffusion to the field-oxide boundary, the modified diode structures with dummy gate [7], [11], [12], called as the poly-bounded N-type (P-type) diodes, had been reported. The cross-sectional view of the poly-bounded Ntype diode realized in a deep submicron CMOS process is shown in Fig. 4. As comparing to Fig. 3, the field-oxide isolation regions between the P+ and N+ diffusions are removed away from the N+ diffusion of the normal N-type diode and replaced by the dummy poly gates. The dummy poly gates are located half on the P-well region and half



Fig. 3 The device cross-sectional view of the normal N-type diode in CMOS process.

on the field-oxide region. Therefore, there is no field-oxide boundary to the N+ diffusion edge of the poly-bounded Ntype diode. Without the field-oxide boundary at the p/n junction of the diode, the pull-down and bend-down corner in Fig. 2 that causes low ESD robustness can be overcome.

2.3 NMOS-Bounded and PMOS-Bounded Diodes

The layout top views and the device cross-sectional views







Fig. 5 The layout top views and the device cross-sectional views of (a) the NMOS-bounded diode, and (b) the PMOS-bounded diode, in CMOS process.

of the new proposed NMOS-bounded diode and PMOSbounded diode are shown in Figs. 5(a) and 5(b), respectively, where the corresponding symbols are also shown in Figs. 5(a) and 5(b). These symbols will be used to draw the on-chip ESD protection circuits in Sect. 4. The N(P)MOSbounded diode has an N(P)MOS structure inserted in the diode structure. The NMOS-bounded diode in Fig. 5(a) has a cathode of N+ diffusion, which does not directly touch the P+ diffusion in the diode structure. The diode anode of P+ diffusion directly touches another N+ diffusion in the NMOS-bounded diode, but this N+ diffusion is floating in the device structure. The anode of the PMOS-bounded diode in Fig. 5(b) is the P+ diffusion in the center region of device structure, which does not directly touch the N+ diffusion. The cathode of PMOS-bounded diode is the N+ diffusion, which directly touches another P+ diffusion in the diode structure, but this P+ diffusion is floating in the device structure. Therefore, silicide-blocking mask is used to block the silicided layer covered on the anode P+ diffusion/floating N+ diffusion (cathode N+ diffusion/floating P+ diffusion) of the N(P)MOS-bounded diode in the silicided or salicided CMOS processes. In this N(P)MOSbounded diode, the poly gate is fully covered by the N+(P+)implantation, therefore the gate function can be successfully formed on the NMOS (PMOS) channel. The poly gate in the layout top view has a close-loop ring to block the fieldoxide boundary from the cathode N+ diffusion (anode P+ diffusion) of the N(P)MOS-bounded diode structure.

3. Experimental Results

The new proposed N(P)MOS-bounded diodes, the traditional normal diodes, and the poly-bounded diodes had been fabricated in a 0.35-µm CMOS process without silicided diffusion. In this study, the gate length of N(P)MOS-Bounded Diodes is $0.35 \,\mu m$ and the gate oxide thickness is 70 Å. The dc I-V characteristics of the diodes are measured by HP4155. To investigate the turn-on behavior of the diodes during high ESD current stress, transmission line pulse (TLP) generator with the pulse width of 100 ns is used to measure the second breakdown current (It2) [13]. The ESD protection circuits with diodes under four different stress modes which include PS-mode (positive-to-VSS), ND-mode (negative-to-VDD), NS-mode (negative-to-VSS), and PD-mode (positive-to-VDD) are measured by the Zap-Master ESD tester to verify their ESD robustness. The failure criterion is defined at the leakage current greater than $1\,\mu\text{A}$ under 3.3-V reverse bias.

3.1 DC I-V Characteristics

The leakage current under normal circuit operating condition is a concern for ESD protection devices connected to an I/O pin. The leakage currents of N-type diodes and P-type diodes under reverse-biased condition are shown in Figs. 6(a) and 6(b), respectively. The poly gate of N(P)MOS-bounded diode is connected to P+ anode (N+



Fig. 6 Comparison of the leakage currents of (a) the N-type diodes, and (b) the P-type diodes, under reverse-biased condition.

cathode) during the dc measurement. In Fig. 6(a), the maximum leakage currents of the NMOS-bounded diode, normal N-type diode, and poly-bounded N-type diode with a junction perimeter of 800 μ m under 3.3-V reverse bias are 50 pA, 37 pA, and 13 pA, respectively. The maximum leakage currents of the PMOS-bounded diode, normal P-type diode, and poly-bounded P-type diode with a junction perimeter of 800 μ m under 3.3-V reverse bias at the N+ cathode are all smaller than 10 pA, as shown in Fig. 6(b). In addition, the dc I-V characteristics among those diodes are not significantly different. Therefore, those diodes in CMOS IC under the normal operating condition have the same turn-off behavior with very low leakage current.

3.2 TLP I-V Characteristics

The TLP-measured I-V characteristics of N-type diodes under reverse-biased and forward-biased ESD stress conditions are shown in Figs. 7(a) and 7(b), respectively. The poly gate is connected to P+ anode for NMOS-bounded diode during the pulse of TLP.

In Fig. 7(a), the It2 level of the NMOS-bounded diode is 5.92 A, which is much higher than that of the normal diode of 1.39 A, and the poly-bounded diode of 1.12 A, where the total junction perimeters of the diodes are $800 \,\mu\text{m}$. The turn-on resistance of the NMOS-bounded diode is initially the same as that of the normal and poly-bounded Ntype diodes at the low voltage condition. When the voltage



Fig.7 The TLP-measured I-V characteristics of N-type diodes (a) under PS-mode stress condition and (b) under NS-mode stress condition.

is more increased, the turn-on resistance of NMOS-bounded diode is reduced significantly, as shown in Fig. 7(a). The ESD current flows through the diode path of the NMOSbounded diode, when the diode is stressed with low-voltage level ESD stress. But, under the high-voltage ESD stress condition, the parasitic lateral n-p-n bipolar transistor in the NMOS-bounded diode structure is turned on to discharge ESD current. The gate-grounded NMOS device often suffers the non-uniform turn-on issue caused by the snapback effect of the parasitic lateral bipolar transistor, especially when the device is drawn with a large device width [14]. Because the ESD current flows through the diode path of the NMOS-bounded diode under low-voltage level ESD stress, the non-uniform turn-on issue of the parasitic lateral bipolar transistor in NMOS-bounded diode can be avoided. In addition, the small turn-on resistance and low holding voltage of parasitic lateral n-p-n bipolar transistor enable the NMOSbounded diode to sustain much higher ESD level. Therefore, the better ESD protection capability can be achieved by the NMOS-bounded diode than that of the normal and polybounded N-type diodes under reverse-biased ESD stress condition.

In Fig. 7(b), the It2 levels of three kinds of diodes under forward-biased ESD stress condition are nearly 5 A with the total diode junction perimeter of $400 \,\mu$ m. The turn-on resistance of the NMOS-bounded diode has no significant difference as compared to that of other diode structures un-



Fig.8 The clamped voltage waveforms by different N-type diodes under PS-mode stress with a 50-V TLP pulse.

der forward-biased ESD stress. High ESD robustness can be achieved by the N-type diodes under forward-biased condition.

3.3 Turn-On Verification

A voltage pulse generated from the TLP system with a pulse height of 50 V and a rise time of ~10 ns is used to simulate the rising edge of ESD pulse. Such a voltage pulse is applied to the N-type diodes under reverse-biased condition to verify the turn-on behavior of the diodes in time domain. The voltage waveforms clamped by different N-type diodes under the stress of a 50-V TLP pulse are shown in Fig. 8, where the clamped voltage level of the diodes has the sequence of: poly-bounded diode (22 V) > normal diode (18.5 V) > NMOS-bounded diode (14 V). The NMOS-bounded diode has the lowest clamped voltage of 14 V. The measured result is consistent with the TLP-measured I-V characteristics shown in Fig. 7(a). Therefore, the NMOS-bounded diode with a lower clamped voltage can provide more efficient ESD protection to the internal circuits.

3.4 ESD Robustness

The It2 level and human body model (HBM) ESD level of N-type diodes with different total diode junction perimeters under PS-mode ESD stress condition are shown in Figs. 9(a) and 9(b), respectively. In Fig. 9(a), the NMOS-bounded diode has much higher It2 level than that of the normal diode or the poly-bounded diode. The It2 level of NMOSbounded diode is almost linearly increased while the total diode junction perimeter increases. The It2 level of NMOS-bounded diode is increased from 1.79 A to 5.92 A when the total diode junction perimeter is increased from $200\,\mu\text{m}$ to $800\,\mu\text{m}$, whereas that of the normal diode or the poly-bounded diode with total diode junction perimeter of $800\,\mu\text{m}$ is only around 1.4 A. In Fig. 9(b), the HBM ESD test results are consistent with the TLP-measured It2 in Fig. 9(a). The NMOS-bounded diode has much higher HBM ESD level than that of the normal diode or the poly-



Fig.9 The (a) It2 level, and (b) HBM ESD level, of N-type diodes with different total diode junction perimeters under PS-mode ESD stress condition.

bounded diode. The HBM ESD level of NMOS-bounded diode with a total diode junction perimeter of $600 \,\mu\text{m}$ is larger than 8 kV, whereas that of the normal diode or the poly-bounded diode with total diode junction perimeter of $800 \,\mu\text{m}$ are only around 2.7 kV.

The It2 level and HBM ESD level of P-type diodes with different total diode junction perimeters under ND-mode ESD stress condition are shown in Figs. 10(a) and 10(b), respectively. In Fig. 10(a), the It2 level of PMOS-bounded diode is increased from 1.13 A to 4.05 A, which is much higher than that of normal diode from 0.4 A to 1.59 A, and that of poly-bounded diode from 0.28 A to 1.15 A, when the total diode junction perimeter is increased from $200\,\mu m$ to $800\,\mu\text{m}$. The It2 level of PMOS-bounded diode is almost linearly increased while the total diode junction perimeter increases. In Fig. 10(b), the HBM ESD test results are consistent with the TLP-measured It2 in Fig. 10(a). The HBM ESD level of PMOS-bounded diode is increased from 2.3 kV to be greater than 8 kV when the total diode junction perimeter is increased from $200\,\mu m$ to $800\,\mu m$. However, the HBM ESD levels of the normal diode and poly-bounded diode with total diode junction perimeter of 800 μ m are only around 3 kV and 2 kV, respectively.

From the experimental results shown in Fig. 9 and Fig. 10, the NMOS-bounded diode and PMOS-bounded diode have much higher ESD levels than those of the nor-



Fig. 10 The (a) It2 level, and (b) HBM ESD level, of P-type diodes with different total diode junction perimeters under ND-mode ESD stress condition.

mal diodes and poly-bounded diodes under reverse-biased condition.

The HBM ESD level of diodes with different total diode junction perimeters under NS-mode ESD stress condition for N-type diode and PD-mode ESD stress condition for P-type diode are shown in Figs. 11(a) and 11(b), respectively. In Fig. 11(a), the HBM ESD level of NMOS-bounded diode has no significant difference to that of normal diode and poly-bounded diode under NS-mode ESD stress. The HBM ESD level of those diodes with the total diode junction perimeter of $400\,\mu\text{m}$ are nearly 8 kV or even higher than 8 kV. In Fig. 11(b), the HBM ESD level of PMOSbounded diode has no significant difference to that of the normal diode or the poly-bounded diode under PD-mode ESD stress. The HBM ESD level of those diodes with the total diode junction perimeter of $400\,\mu$ m are nearly 8 kV or even higher than 8 kV. From the experimental results shown in Fig. 11, the HBM ESD test results are consistent with the TLP-measured It2 shown in Fig. 7(b). Those diodes can sustain much higher HBM ESD levels due to the diodes are stressed under the forward-biased condition.

From the measured results, the MOS-bounded diodes have much higher ESD robustness than that of other diodes under both forward-biased and reverse-biased stress conditions. Therefore, the MOS-bounded diodes can provide



Fig. 11 The HBM ESD levels of diodes with different total diode junction perimeters under (a) NS-mode ESD stress condition for N-type diodes, and (b) PD-mode ESD stress condition for P-type diodes.

more effective ESD protection to the internal circuits in the ESD protection scheme shown in Fig. 1.

4. Applications for On-Chip ESD Protection

With the new proposed NMOS-bounded or PMOS-bounded diodes, some new on-chip ESD protection circuits have been designed to achieve higher ESD robustness and better protection capability for protecting the internal circuits [10].

4.1 ESD Protection Circuits for I/O Pad

The ESD protection circuits with the NMOS-bounded and PMOS-bounded diodes for the input or output pads are shown in Figs. 12(a) and 12(b), respectively. In Fig. 12(a), the poly gate of the N(P)MOS-bounded diode is connected to VSS(VDD) through a resistor. The PMOS and NMOS in the diode structures are kept off when the IC is in the normal operation condition with the VDD and VSS biases. In Fig. 12(b), the gate-coupled technique [15] is applied to control the gate of the NMOS-bounded and PMOS-bounded diodes. In the normal operation condition, the PMOS and NMOS in the diode structures are kept off due to the resistor connection of their gates. But, in the PS (ND)-mode ESD stress, the positive (negative) ESD voltage on the pad is coupled to the gate of N(P)MOS-bounded diode through the ca-



Fig. 12 The ESD protection circuits with the NMOS-bounded and PMOS-bounded diodes for the input or output pads, where (a) poly gate of the N(P)MOS-bounded diode is connected to VSS (VDD) through a resistor, and (b) the gate-coupled technique is applied.

pacitor Cn (Cp). With a positive (negative) gate bias at the gate Gn (Gp), the N(P)MOS-bounded diode can be turned on more quickly to discharge ESD current. Therefore, it can provide better and effective ESD protection function to the internal circuits.

4.2 Power-Rail ESD Clamp Circuits

The ESD clamp circuit between the VDD and VSS power rails is added into the chip to avoid ESD damages located in the internal circuits [6]. The power-rail ESD clamp circuits realized with the NMOS-bounded diode and PMOSbounded diode are shown in Figs. 13(a) and 13(b), respectively. In Figs. 13(a) and 13(b), the gate of NMOS-bounded or PMOS-bounded diode is controlled by the RC-based ESD detection circuit, where the RC has a time constant of ~ 1 μ s [6]. In the normal operation condition, the gate of N(P)MOS-bounded diode is biased at the voltage level of VSS(VDD), therefore the N(P)MOS in the N(P)MOSbounded diode structure is kept off. During the VDD-to-VSS ESD stress condition, the RC delay of $\sim 1 \,\mu s$ causes the voltage on the capacitor C still staying at a low voltage level (\sim VSS). In Fig. 13(a), the inverter is powered up by the ESD energy to charge the gate Gn of NMOS in the NMOS-bounded diode to a high voltage level. Therefore, the NMOS-bounded diode can be quickly turned on to discharge ESD current from VDD to VSS. In Fig. 13(b), with a low voltage level on the gate Gp of PMOS in the PMOSbounded diode due to the RC delay, the PMOS-bounded diode can be turned on to discharge ESD current from VDD to VSS. By using the RC delay circuit technique, the gates of NMOS-bounded/PMOS-bounded diodes can be suitably biased to quickly discharge ESD current. Therefore, this design can provide more effective ESD protection to the internal circuits of CMOS ICs.

4.3 ESD Conduction Cell between Separated Power Lines

For a complex VLSI, the power lines for different circuit groups are often separated to block the noise between differ-



Fig. 13 The power-rail ESD protection circuits realized by (a) the NMOS-bounded diode, and (b) the PMOS-bounded diode, with RC-based ESD detection circuit.



Fig. 14 The ESD protection networks realized with NMOS-bounded and PMOS-bounded diodes between the separated power rails. The stacked NMOS-bounded and PMOS-bounded diodes in back-to-back configuration are used to connect the different power lines.

ent circuit groups. But, an IC with the separated power lines often has some unexpected ESD damages located on the interface circuits between the circuit groups [16]. To avoid the ESD damage on the interface or internal circuits, the ESDconduction cell is added between the separated power lines [17]. The NMOS-bounded and PMOS-bounded diodes in stacked configuration can be placed between the separated power rails to provide the ESD current discharging paths. In Fig. 14, the stacked PMOS-bounded (NMOS-bounded) diodes in back-to-back configuration are used to connect VDD1 (VSS1) and VDD2 (VSS2) power lines to provide ESD current discharging paths. The PMOS-bounded diodes forward-stacked (backward-stacked) from VDD1 to VDD2 have gates controlled by RC-based ESD detection circuit of circuit_1 (circuit_2) to quickly discharge ESD current. In addition, the gate of each NMOS-bounded diode is connected to its cathode of each NMOS-bounded diode. The power-rail ESD clamp circuits in Fig. 14 can be realized by those circuits shown in Fig. 13. By using these ESD protection networks, the interface circuits and internal circuits of CMOS IC can be fully protected against ESD damage.

5. Conclusion

DC characteristics, TLP characteristics, turn-on verification, and ESD robustness of N(P)MOS-bounded diodes for ESD

protection in a 0.35- μ m CMOS process have been investigated and compared to that of normal N(P)-type diode and poly-bounded N(P)-type diode. With the new proposed MOS-bounded diode structure, the parasitic lateral bipolar transistor in the MOS-bounded diode has shown with a small turn-on resistance and a low holding voltage to sustain much higher ESD level. The proposed N(P)MOS-bounded diodes can sustain the HBM ESD stress of > 8 kV with the total diode junction perimeter of 800 μ m in a 0.35- μ m CMOS process in all modes of ESD stresses. The experimental results have confirmed that the new proposed diode structures with higher HBM ESD robustness are more suitable for on-chip ESD protection design than the other diode structures in deep-submicron CMOS processes.

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