Investigation of Human-Body-Model and Machine-Model ESD Robustness on Stacked Low-Voltage Field-Oxide Devices for High-Voltage Applications

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***Abstract*— Electrostatic discharge (ESD) robustness of low-voltage (LV) field-oxide devices in stacked configuration for high-voltage (HV) applications was investigated in a 0.5-μm HV silicon on insulator (SOI) process. Stacked LV field-oxide devices with different stacking numbers have been verified in a silicon chip to exhibit both a high ESD robustness and latch-up immunity for HV applications. The effect of turn-on resistance in the stacked ESD protection device on ESD current waveform under human body model (HBM) and machine model (MM) ESD tests was studied. The resistance of stacked device has a significant impact on the ESD peak current and damping waveform, especially in MM ESD test. The MM ESD level can be increased by the numbers of LV field-oxide devices in stacked configuration, but the HBM ESD level is still kept the same. The mechanism to cause such a result has been theoretically analyzed in detail in this paper.**

***Index Terms*— Damping effect, electrostatic discharge (ESD) protection, high-voltage (HV) ICs, human body model (HBM), machine model (MM).**

I. Introduction

IN HIGH-VOLTAGE (HV) applications, the power management ICs and automotive ICs play a major role, which were often realized with the laterally diffused-MOS (LDMOS) devices. The HV ICs implemented in the SOI process have got more advantages to manage HV blocks, to reduce parasitic bipolar effect, and to increase circuit speed. To get sufficient electrostatic discharge (ESD) robustness for the HV ICs, the HV devices at the I/O pins were often drawn with a large device dimension to meet the ESD specifications. In the literature [1]–[6], ESD protection in SOI process was reported with MOS and SCR combining together into the device structure, which allowed SCR being triggered on to reach a high ESD robustness. However, the holding voltage (V_h) of SCR was much lower than the circuit operation voltage level. If such ESD protection device was triggered on by the unexpected noises or the electrical transient pulses in some system-level reliability tests [7]–[10], it would cause serious latch-up-like failure in the HV applications.

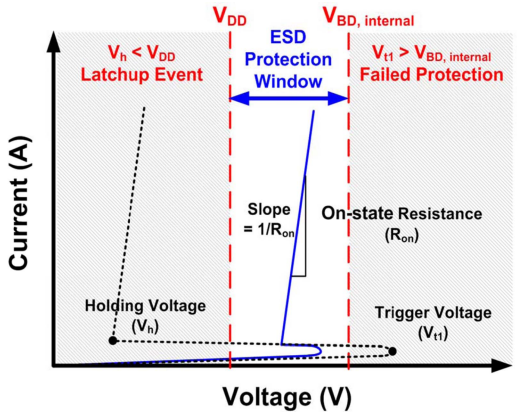

Fig. 1. I–V characteristics of ESD protection device to meet ESD protection window.

The typical I–V characteristics of ESD protection devices are shown in Fig. 1. The snapback behavior of the SCR embedded with HV LDnMOS together did not fulfill ESD design window for HV applications, due to its low holding voltage. Compared with HV devices, the low-voltage (LV) devices were relatively good at ESD robustness, and the stacked configuration is a way to achieve a high holding voltage for latch-up-free design [11]–[13].

In this paper, the stacked LV p-type field-oxide devices (LVPFOD) with different stacking numbers for HV applications were investigated in a 0.5-μm SOI process. This 0.5-μm SOI process was developed for the applications of 120, 150, and 200 V. Different HV devices for ESD protection were also accomplished as reference. Experimental results measured by the dc I–V curve tracer, transmission-line-pulsing (TLP) system, and ESD tester have confirmed that the proposed ESD solution with the stacked LVPFOD can achieve both the high ESD robustness and latch-up-free immunity for HV applications.

II. Typical HV Devices and the Proposed Solution With Stacked LVPFOD

A. Typical HV Devices

The device cross-sectional view and the corresponding layout top view of the HV LDnMOSs are shown in Fig. 2(a) and (b), respectively. The device dimension of

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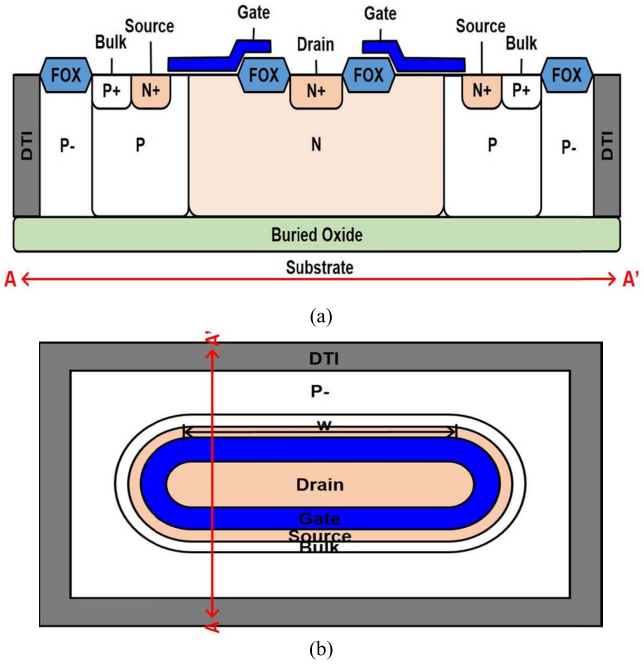


Fig. 2. (a) Device cross-sectional view and (b) layout top view, of HV LDnMOS in a 0.5-μm SOI process.

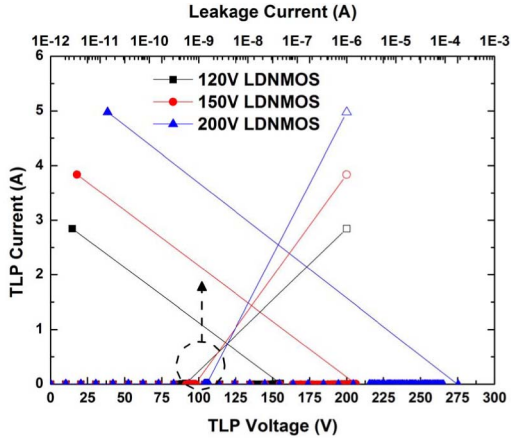


Fig. 3. TLP I–V characteristics of the 120, 150, and 200 V HV LDnMOS fabricated in a 0.5-μm SOI process.

LDnMOS was drawn with $W/L = 200/0.9$ μm in the testchip to investigate its ESD robustness, which has been fabricated in a 0.5-μm SOI process. For different HV applications, the clearances from the drain to the poly gate of LDnMOS are specified differently in the design rules of the given 0.5-μm SOI process.

The TLP-measured I–V characteristics of the 120, 150, and 200 V LDnMOS with gate-grounded connection are shown in Fig. 3. The drain breakdown voltages (at $I = 1$ μA) of those HV LDnMOSs are 146.5, 192.8, and 271 V, respectively. The trigger voltages (V_{t1}) are 155.3, 206.3, and 275.5 V, respectively. But, such HV devices got very low human body model (HBM) ESD robustness (<500 V), which were almost burned out immediately after drain breakdown. Such HV LDnMOSs can neither provide self-protection, nor to protect the internal circuits or devices in the HV ICs.

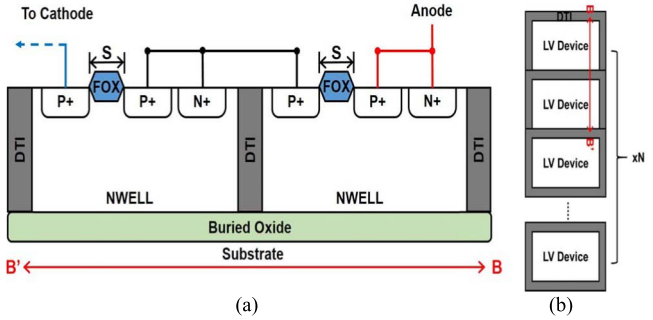


Fig. 4. (a) Device cross-sectional view and (b) layout top view, of the proposed ESD protection solution realized with the stacked LVPFOD in a 0.5-μm SOI process.

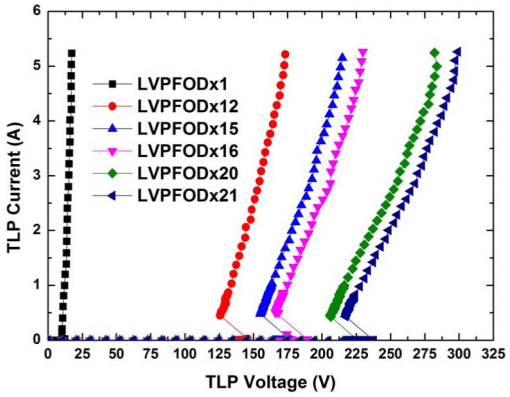
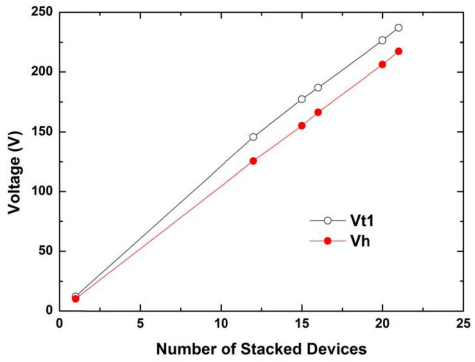


Fig. 5. TLP-measured I–V characteristics of the stacked LVPFOD with different stacking numbers of 1, 12, 15, 16, 20, and 21, fabricated in a 0.5-μm SOI process.

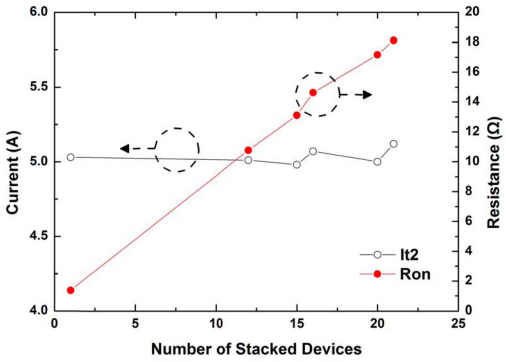
B. Stacked LVPFOD Devices

The device cross-sectional view and layout top view of the stacked LVPFOD in a 0.5-μm HV SOI process are shown in Fig. 4(a) and (b), respectively. The dimension of each LVPFOD in the stacked configuration was drawn with a total width of 1600 μm and S of 0.9 μm, which was fully isolated to each other by the deep trench isolation and buried oxide. Every LVPFOD was connected through metal layers to make the stacked configuration with different stacking numbers. The drain breakdown voltage (defined at 1 μA) of a single LVPFOD is 11 V, measured from the silicon chip. So, it is easy to estimate the stacking number of LVPFOD to meet different application voltages of the HV ICs.

The TLP-measured I–V characteristics of the stacked LVPFOD with different stacking numbers (1, 12, 15, 16, 20, and 21) are shown in Fig. 5. The pulsewidth of TLP used in this measurement is 100 ns. The trigger voltage (V_{t1}) of stacked LVPFOD can be smaller than the breakdown voltage of HV LDMOS to get an effective ESD protection. The holding voltage (V_h) of stacked LVPFOD can be greater than the maximum operation voltage (V_{cc}) to avoid latch-up-like issue. The trend of V_{t1} and V_h on different stacking numbers is shown in Fig. 6(a). They can be linearly increased by the numbers of LVPFOD in the stacked configuration. The ON-state resistance (R_{ON}) of stacked LVPFOD is also linearly increased by the numbers of stacked LVPFOD. The second breakdown current (I_{t2}) of stacked LVPFOD with different stacking numbers can be kept at ~5 A, which does not



(a)



(b)

Fig. 6. Dependence of TLP-measured (a) trigger voltage (V_{t1}) and holding voltage (V_h) and (b) second breakdown current (I_{t2}) and ON-state resistance (R_{ON}), on the number of stacked LVPFOD devices.

decrease under different stacking numbers. The trend of R_{ON} and I_{t2} on the different stacking numbers is shown in Fig. 6(b). Such measured results have confirmed that the ESD current can uniformly flow through every LVPFOD in the stacked configuration.

The detailed I–V characteristics of stacked LVPFOD with different stacking numbers are listed in Table I. In the literature, the silicon data reported in this paper showed the first solution in SOI process that can provide over 8-kV HBM ESD level in a HV SOI process with latch-up-free immunity. By adjusting the stacking numbers, the proposed ESD protection solution can be easily adjusted for different HV applications.

With TLP-measured I_{t2} of ~5 A, the stacked LVPFOD also exhibited excellent ESD robustness of up to 8 kV in HBM ESD test. Moreover, the stacked LVPFOD under machine model (MM) ESD test can pass at least 450 V, which can be linearly increased by the numbers of LVPFOD in the stacked configuration. The trend of MM ESD level on the stacked LVPFOD with different stacking numbers is shown in Fig. 7. The further study to understand the dependence of HBM and MM ESD levels on the stacked LVPFOD with different stacking numbers is presented in Section III.

III. HBM AND MM EFFECT OF STACKED LVPFOD

As shown in Table I, all the HBM ESD levels of stacked LVPFOD with different stacking numbers are kept the same,

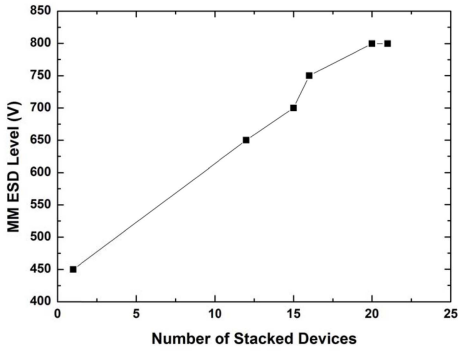


Fig. 7. Dependence of MM ESD level on the number of stacked LVPFOD devices.

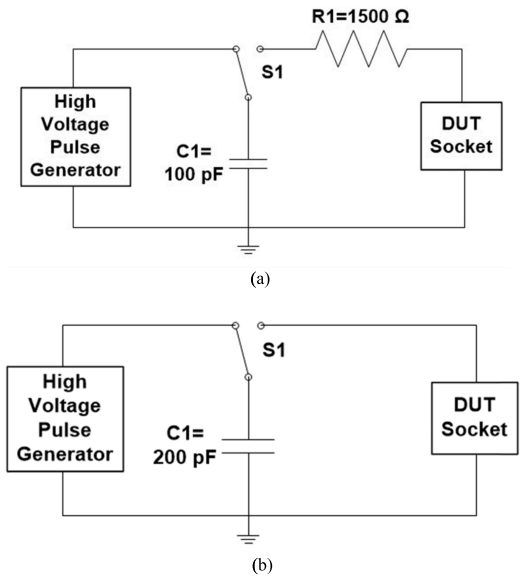


Fig. 8. Equivalent circuits of (a) HBM [14] and (b) MM [15], ESD tests.

but the MM ESD level increases with the numbers of stacked LVPFOD. Based on JEDEC standards [14], [15], the equivalent circuits of HBM and MM ESD tests are shown in Fig. 8(a) and (b), respectively. In HBM, there is a resistance of 1500 ohm in series into the ESD current discharging path to the device under test (DUT). In MM, ideally, there is no resistance in series into the ESD current discharging path to the DUT. The measurement setup to capture the transient current waveforms under HBM and MM ESD tests is shown in Fig. 9. The transient current can be captured by the current prober (CT1), and through the attenuator the waveform can be observed and recorded in the oscilloscope. The ESD zapping voltages on the stacked LVPFOD for transient ESD current measurement were selected as 8 kV for HBM and 300 V for MM, respectively. From Table I, the stacked LVPFOD can sustain such ESD stresses without damage.

The ESD current waveforms on the stacked LVPFOD with different stacking numbers under 8-kV HBM ESD test are shown in Fig. 10(a). A zoomed-in figure to show the peak current is also inserted in Fig. 10(a). Because the ON-state resistance of stacked LVPFOD is much smaller (comparing with the series resistance of 1.5 kΩ), as shown in Table I,

TABLE I

SUMMARY OF TLP *I–V* CHARACTERISTICS AND ESD ROBUSTNESS ON STACKED LVPFOD WITH DIFFERENT STACKING NUMBERS

Staked Number of LVPFOD	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V) (I@1μA)	R_{on} (Ω)	HBM (kV)*	MM (V)*
1	12.20	10.14	5.03	11.0	1.39	>8	450
12	145.69	125.55	5.01	132.5	10.77	>8	650
15	177.36	155.13	4.98	165.1	13.11	>8	700
16	186.93	166.30	5.07	176.3	14.63	>8	750
20	226.67	206.49	5.00	221.5	17.17	>8	800
21	237.04	217.48	5.12	233.5	18.13	>8	800

(*) ESD failure criteria : BV (I @1μA) shift >20%.

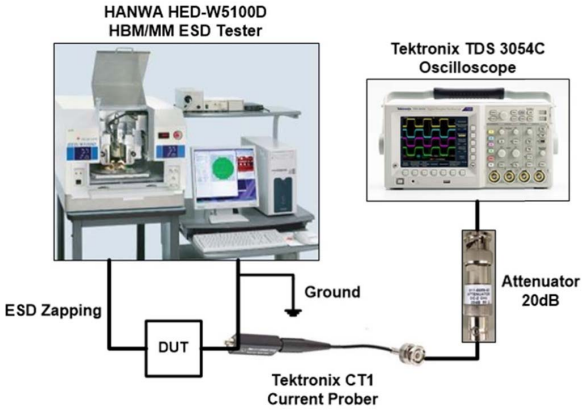


Fig. 9. Measurement setup for capturing the ESD current waveforms under HBM and MM ESD test.

the ESD current under HBM ESD test is mainly dominated by the series resistance of 1.5 kΩ. So, the current waveforms in Fig. 10(a) almost have the similar peak currents, rise times, and pulse decay times.

The ESD current waveforms on the stacked LVPFOD with different stacking numbers under 300 V MM ESD test are shown in Fig. 10(b). The current waveform of MM ESD test is dominated by device resistance itself, because there is no resistance in series in MM ESD test. As shown in Fig. 10(b), the measured current waveforms under MM ESD test have the decreased peak currents, slower rise times, and smaller pulsewidth of the first current pulse, when the stacking numbers of stacked LVPFOD are increased. With the decreased peak currents, the MM ESD levels on the stacked LVPFOD can be increased by the stacking numbers of stacked LVPFOD. The dependences of HBM and MM ESD peak currents on the stacked LVPFOD with different stacking numbers are compared in Fig. 11.

The dependences of rise time and first pulsewidth on the stacked LVPFOD with different stacking numbers under 300 V MM ESD test are shown in Fig. 12. The measured MM current waveforms verified that the rise time and first pulsewidth are decreased by the numbers of stacked LVPFOD. Under the same MM ESD voltage of 300 V, when the device ON-state resistance is larger, the peak current becomes smaller, as well as the rise time and first pulsewidth are also decreased.

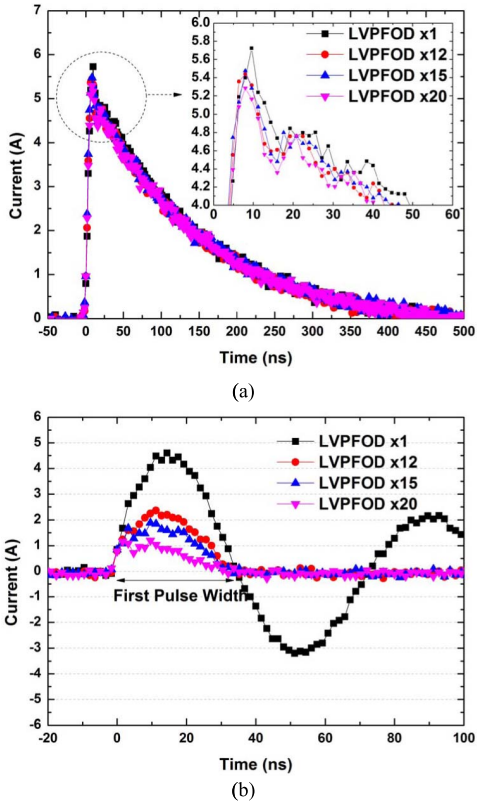


Fig. 10. Measured transient current waveforms through the stacked LVPFOD with different stacking numbers under (a) 8-kV HBM and (b) 300 V MM, ESD tests.

IV. DAMPING EFFECT IN ESD TEST

As shown in Fig. 10(b), there are underdamping and overdamping waveforms in the measured MM ESD currents, when the stacking numbers in the stacked LVPFOD are different. The equipment *RLC* series circuit of MM ESD test, including the parasitic inductance (L) along the connection line and the ON-state resistance (R) of DUT, is shown in Fig. 13. From the circuit theory [16], there are three different waveforms depending on the value of the damping factor (ξ), which are underdamping ($\xi < 1$), overdamping ($\xi > 1$), and critically damped ($\xi = 1$). The underdamping waveform has a decaying oscillation at the frequency of ω_d. The overdamping waveform has a decay of the transient waveform without oscillation. The equations

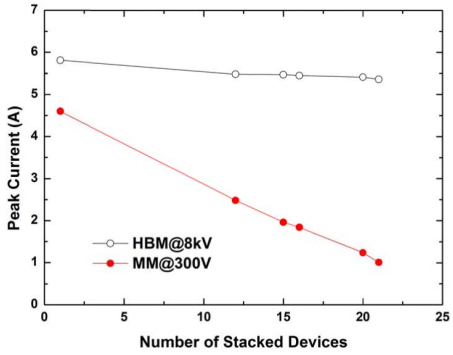


Fig. 11. Dependences of HBM and MM ESD peak currents on the number of stacked LVPFOD devices.

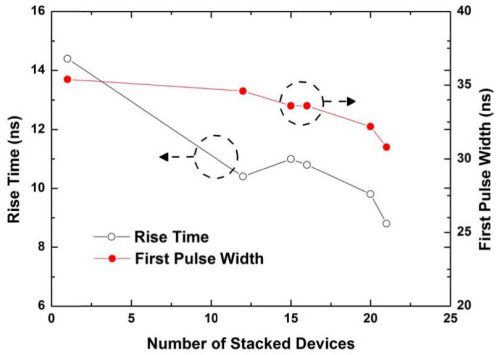


Fig. 12. Dependences of rise time and first pulse width on the number of stacked LVPFOD devices under 300 V MM ESD test.

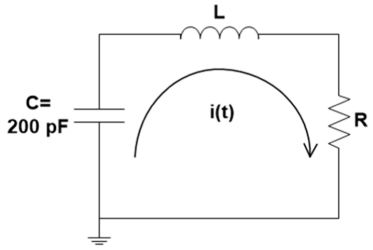


Fig. 13. Equipment *RLC* series circuit of MM ESD test, including the parasitic inductance (L) along the connection line and the ON-state resistance (R) of DUT.

of damping factor (ξ) and frequency ω_d are derived in the following.

In the condition with a single LVPFOD that has an underdamping current waveform, the capacitance (C) is 200 pF and $R_{\rm ON}$ is 1.39 Ω. Also known that the initial voltage of capacitance is 300 V, and peak current is 4.60 A. The differential equation of *RLC* series circuit of MM ESD test can be found in the constitutive equation (1). First of all, for the case where the waveform is underdamping, differentiating and dividing by inductance (L) leads to the second-order differential equation (2). Then, the differential equation has the characteristic (3) of underdamping waveform. The corresponding parameters α, ω_0, and ω_d are shown in (4)–(6). The coefficients C_1 and C_2 are determined by the boundary conditions of the specific problem being analyzed. Therefore, the underdamping waveform of MM ESD test can be theoretically calculated

$$Ri + L\frac{di(t)}{dt} + \frac{1}{C}\int_{-\infty}^{\tau=t} i(\tau)d\tau = 0 \tag{1}$$

$$\frac{d^2i(t)}{dt^2} + \frac{R}{L}\frac{di(t)}{dt} + \frac{1}{LC}i(t) = 0 \tag{2}$$

$$i(t) = C_1 e^{-\alpha t}\cos(\omega_d t) + C_2 e^{-\alpha t}\sin(\omega_d t) \tag{3}$$

$$\alpha = \frac{R}{2L} \tag{4}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{5}$$

$$\omega_d = \sqrt{\omega_0^2 - \alpha^2} \tag{6}$$

$$\xi = \frac{\alpha}{\omega_0} = \frac{R}{2}\sqrt{\frac{C}{L}}. \tag{7}$$

Finally, the parasitic inductance in the *RLC* series circuit of MM ESD test can be calculated from the measured peak current value. From the measured data, the parasitic series inductance in the MM ESD test is extracted as 0.41 nH. According to the damping factor in (7), if the MM current waveform is overdamping ($\xi > 1$), the device resistance should be more than 2.88 Ω. From the TLP-measured $R_{\rm ON}$ listed in Table I, only the single LVPFOD has its resistance (1.39 Ω) smaller than 2.88 Ω, therefore the measured ESD current with underdamping waveform only appeared on the single LVPFOD (marked as LVPFOD x1) in Fig. 10(b). When the stacking number is increased, the ON-state resistance is also increased to be more than 2.88 Ω, so the measured ESD currents in Fig. 10(b) of the stacked LVPFOD appeared with the overdamping waveforms. From this theoretical analysis, the root cause to make the stacked LVPFOD having higher MM ESD level when the stacking number is increased can be clearly understood.

As seen in Fig. 10(a), there are all overdamping waveforms in the HBM ESD currents whenever the LVPFOD with different stacking numbers. By the same analysis method used in MM, the parameters of *RLC* series circuit for HBM ESD test can be known. According to the extracted inductance (0.41 nH) along the connection line of the ESD tester under MM ESD test, the HBM ESD test is also performed by the same ESD tester with the same connection line, so the parasitic inductance under HBM ESD test can also be approximated as ∼0.41 nH. The capacitance of HBM is specified as 100 pF. Based on the damping factor in (7), if the HBM current waveform is overdamping, the total series resistance along the ESD current path should be more than 4.07 Ω. In the condition with a single LVPFOD, $R_{\rm ON}$ of DUT (single LVPFOD) is only 1.39 Ω, but the HBM discharge resistance of 1.5 kΩ adds into the series *RLC* circuit. With the total resistance (1.5 kΩ + $R_{\rm ON}$) much larger than 4.07 Ω, it is clear to know why the definition current waveform of HBM in the JEDEC standard [14] is always an overdamping waveform. With the dominated series resistance of 1.5 kΩ, the HBM ESD peak current waveforms in Fig. 10(a) have almost the same overdamping waveforms. Therefore, the LVPFOD with different stacking numbers can have the same HBM ESD robustness, as the similar peak currents shown

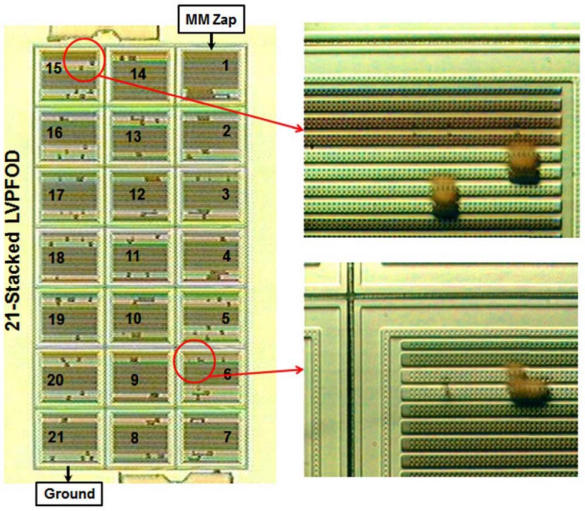


Fig. 14. Picture to show the failure locations among the 21-stacked LVPFOD devices after the MM ESD stress of 850 V.

in Fig. 11 among the stacked LVPFOD under 8-kV ESD zapping.

V. Failure Analysis

As shown in Table I, all of the stacked LVPFOD devices with different stacked numbers can sustain HBM ESD stress of over 8 kV (the maximum HBM ESD voltage provided by the ESD tester). However, the failure voltage levels of the stacked LVPFOD devices under MM ESD test are below the maximum MM ESD voltage that can be provided by the ESD tester. So, the failure analysis is applied on the ESD-zapping sample with 21-stacked LVPFOD devices after MM ESD stress. The picture with the failure locations among the 21-stacked LVPFOD devices after the MM ESD stress of 850 V is shown in Fig. 14, where the connection sequence of each LVPFOD is shown with the number (1∼21) on it. The ESD-induced failure sites are happened and located on every LVPFOD device in the stacked configuration. Some potions are enlarged and shown at the right-hand side of Fig. 14. This picture confirmed that the MM ESD current is really discharging through every LVPFOD device in the stacked configuration.

VI. Conclusion

An effective ESD protection solution realized with LVPFOD in stacked configuration for 120, 150, and 200 V HV applications has been successfully verified in a 0.5-μm SOI process. The proposed ESD protection solution can get high ESD robustness with latch-up-free immunity. In addition, the root cause, for why the MM ESD level can be increased by the stacking numbers of stacked LVPFOD but all the HBM ESD level are still kept the same, has been theoretically analyzed in this paper.

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