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Active Electrostatic Discharge (ESD) Device for On-Chip ESD Protection in Sub-Quarter-Micron Complementary Metal-Oxide Semiconductor (CMOS) Process

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A novel electrostatic discharge (ESD) protection device with a threshold voltage of ~0 V for complementary metal-oxide semiconductor (CMOS) integrated circuits in sub-quarter-micron CMOS technology is proposed. Quite different to the traditional ESD protection devices, such an active ESD device is originally standing in its turn-on state when the IC is zapped under ESD events. Therefore, such an active ESD device has the fastest turn-on speed and the lowest turn-on voltage to effectively protect the internal circuits with a much thinner gate oxide in future sub-0.1 μm CMOS technology. The proposed active ESD device is fully process-compatible to the general sub-quarter-micron CMOS process.
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KEYWORDS: electrostatic discharge (ESD), threshold voltage, active ESD device, leakage current

Electrostatic discharge (ESD) damage has become the main reliability issue for complementary metal-oxide semiconductor (CMOS) IC products fabricated in the sub-quarter-micron CMOS processes. In the past, the on-chip ESD protection devices in CMOS ICs were realized by the N/P-channel metal-oxide semiconductors NMOS/PMOS, field-oxide device (FOD), diode, parasitic bipolar junction transistor (BJT), or even the silicon-controlled rectifier (SCR) devices. Such traditional ESD protection devices are initially kept off in CMOS ICs. Under ESD zapping condition, the overstress ESD voltage causes the junction breakdown to trigger on such traditional ESD protection devices, and then the ESD current is discharged through them. Among these traditional ESD protection devices, they have relatively higher breakdown voltage or higher turn-on voltage. To effectively protect the thinner gate oxide in deep-submicron CMOS processes, the gate-coupled[1–3] or the substrate-triggered[4–7] circuit techniques had been used to reduce the turn-on voltage or to enhance the turn-on speed of the traditional ESD protection devices.

In this paper, the active ESD device is proposed to effectively protect CMOS IC products in the sub-quarter-micron CMOS process. Such active ESD device has the fastest turn-on speed and the lowest turn-on voltage due to the ~0 V or even negative threshold voltage. When the IC is floating without any power bias, such active ESD device is initially in the turn-on state to discharge any ESD-stress current. When the IC is under normal circuit operating condition, such active ESD device can be turned off by a negative gate voltage.

As the device scaling down, the twin-well technology is necessary to balance the device characteristics of NMOS and PMOS devices. The normal NMOS and PMOS devices in the sub-quarter-micron process should be formed in the P-well and N-well, respectively. The active ESD device proposed in this paper is built neither in the P-well nor in the N-well, but it is directly in the p-substrate. The detail device structure with different doping profiles of the normal NMOS device and the proposed active ESD device in a standard twin-well CMOS process are shown and compared in Figs. 1(a) and 1(b). The main difference between these two devices is that the active ESD device only has a p-type pocket implant in the source/drain region to prevent the short channel effect and a n-type lightly-doped drain (LDD) implant to reduce the hot carrier effect. The active ESD device is directly formed in the p-substrate without the P-well region, which can be realized in general sub-quarter-micron CMOS processes by using layout design to generate the correct masking layer. Due to the lightly p-type doses, this active ESD device has very low threshold voltage (~0 V) and high electron mobility in channel region. Therefore, it will have the lowest trigger voltage and the highest turn-on speed to discharge the fast transient ESD current.

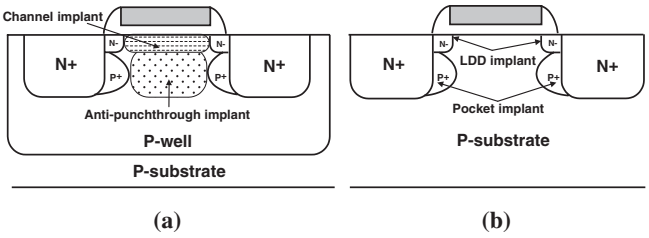

Fig. 1. The device structures of (a) the normal NMOS device, and (b) the proposed active ESD device, in a twin-well p-substrate CMOS technology.

The I_{ds}-V_{gs} characteristics of the active ESD device and the normal NMOS fabricated in a 0.25-μm shallow trench isolation (STI) CMOS process are measured by HP4155 under V_{ds} of 0.1 V and shown in Fig. 2. Both of the active ESD device and the normal NMOS are drawn with the same channel width of 360 μm in the same layout style, but the channel length is modified to investigate its performance for ESD protection. The threshold voltage is extracted by the standard maximum Gm method. The threshold voltage of the active ESD device (~0.3 V) is much lower than that of normal NMOS (~0.7 V). Under 0-V gate bias, the active ESD device (the normal NMOS) with W/L of 360 μm/0.5 μm has a current level about ~0.01 mA (~0.3 nA). With

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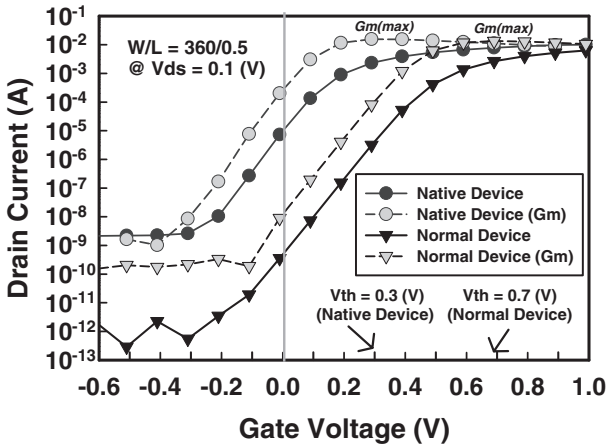

Fig. 2. The measured DC *I-V* curves and the Gm curves of the fabricated active ESD device and the normal NMOS. The threshold voltage (V_{th}) is extracted by the maximum Gm method.

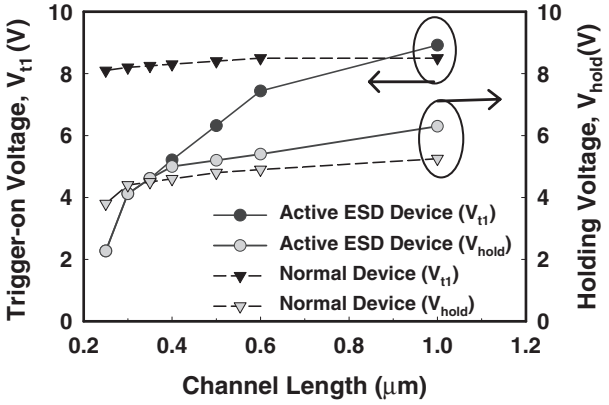

Fig. 3. The dependences of the trigger-on voltage (V_{t1}) and the snapback holding voltage (V_{hold}) of the active ESD device and the normal NMOS on the channel length.

more negative gate bias (–0.5 V), the leakage current of the active ESD device can be reduced to ~ 2 nA. Therefore, the active ESD devices are initially standing in the turn-on state when the gate voltage is greater than zero or even floating.

The snapback *I-V* characteristics of the fabricated active ESD devices and the normal NMOS under different channel lengths are measured by curve tracer (Tek370). The dependence of the trigger-on voltage (V_{t1}) and the snapback holding voltage (V_{hold}) of the active ESD device and the normal NMOS on the channel length are compared in Fig. 3. The trigger-on voltage of the normal NMOS device depends on the breakdown of p-n junction. So, the trigger-on voltage of the normal NMOS device is almost constant. On the other hand, the trigger-on voltage of the active ESD device decreases when its channel length is shrunk. The reason is that the active ESD device has a serious drain-induced barrier lowering (DIBL) effect (one of the short channel effect) in surface channel due to low p-type channel dose. With a shorter channel length, the DIBL effect becomes more serious to cause a lower trigger-on voltage. When the channel length of the active ESD device is below 0.4 μm, its holding voltage is equal to its trigger-on voltage due to punchthrough mechanism.

The TLP-measured second breakdown current (I_{t2}) of the

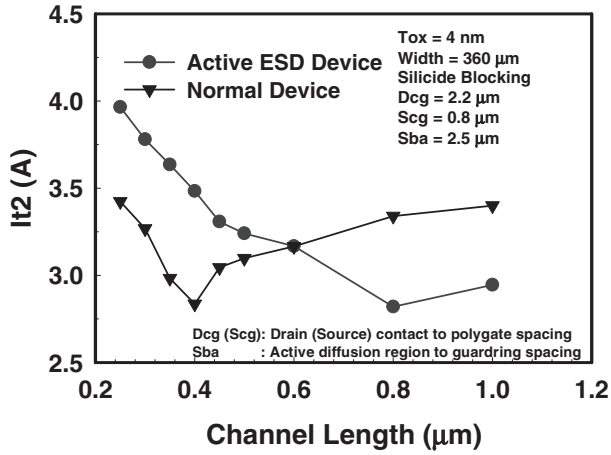

Fig. 4. The dependences of the transmission-line-pulse (TLP)-measured second breakdown current (I_{t2}) of the active ESD device and the normal NMOS on different channel lengths.

active ESD devices and the normal NMOS with different channel lengths are shown in Fig. 4. The I_{t2} value of active ESD device is linearly increased as the channel length is shrunk. This is because the surface punchthrough mechanism creates more current path to discharge ESD current. The I_{t2} value of active ESD devices is lower than that of normal NMOS devices in long channel region, but is higher than that of the normal NMOS devices in short channel region. A device with a higher I_{t2} can sustain a higher ESD stress. Therefore, ESD robustness of the active ESD devices can be superior to that of the normal NMOS devices with a shorter channel length.

With the superiority of the low threshold voltage and high ESD robustness, the active ESD device can be used stand alone as the ESD clamp device for on-chip ESD protection. It can be further used as a control device to quickly trigger on other ESD clamp devices to discharge ESD current. In this study, one ESD clamp cell (inserted in Fig. 5) is realized by a FOD, which is triggered by the active ESD device. The FOD is triggered on by the active ESD device through its substrate. The TLP-measured current-voltage (*I-V*) curves of the combined ESD clamp cell and the stand-alone FOD

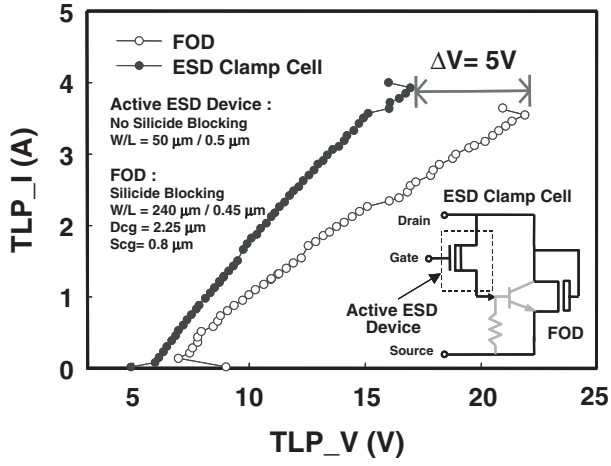

Fig. 5. The TLP-measured *I-V* curves of the combined ESD clamp cell (inserted in this figure) and the stand-alone field-oxide device (FOD).

device are compared in Fig. 5. The FOD is drawn with W/L of 240 μm/0.45 μm, and the active ESD device inserted in this FOD is drawn with W/L of only 50 μm/0.5 μm. The triggered-on voltage (V_{t1}) of the combined ESD clamp cell is about 5.8 V, which is lower than that (9.0 V) of the stand-alone FOD in the same CMOS process. The secondary breakdown current (I_{t2}) value (3.9 A) of the combined ESD clamp cell is slightly greater than that (3.54 A) of the stand-alone FOD. But, the secondary breakdown voltage (V_{t2}) (16.9 V) of the combined ESD clamp cell has a 5 V reduction from that (21.9 V) of the stand-alone FOD. With a much lower V_{t2}, it can provide better ESD protection for the internal circuits with thinner gate oxide in future sub-0.1 μm CMOS process.

The active ESD device for ESD protection has been successfully verified in 0.25-μm STI twin-well p-substrate CMOS process. With the superiors of fastest turn-on speed and lowest trigger-on voltage under ESD stress condition, the active ESD device is excellent to be the express ESD clamp device for effective ESD protection in the future sub-0.1 μm CMOS process. Under normal circuit operating condition, the leakage current of the active ESD devices can be turned off by a negative gate bias which can be generated by an on-chip charge pumping circuit. The proposed active ESD device is fully process-compatible to the general sub-quarter-micron CMOS process.

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1) C. Duvvury and C. Diaz: *Proc. IEEE Int. Reliability Physics Symp. (IRPS), San Diego, California, 1992* (IEEE, New York, 1992) p. 141.
2) M. D. Ker, C. Y. Wu, T. Cheng and H. H. Chang: IEEE Trans. VLSI Syst. **4** (1996) 307.
3) J. Chen, A. Amerasekera and C. Duvvury: IEEE Trans. Electron Devices **45** (1998) 2448.
4) M. D. Ker, T. Y. Chen and C. Y. Wu: *Proc. IEEE Int. ASIC Conf. & Exhibit, Portland, Oregon, 1997* (IEEE, New York, 1997) p. 287.
5) M. D. Ker, T. Y. Chen, C. Y. Wu, H. Tang, K. C. Su and S. W. Sun: *Proc. IEEE Int. Symp. Circuits & Systems, Monterey, California, 1998* (IEEE, New York, 1998) p. 212.
6) C. Duvvury, S. Ramaswamy, A. Amerasekera, R. Cline, B. Andresen and V. Gupta: *Proc. 22th Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symp., Anaheim, California, 2000* (ESD Association, New York, 2000) p. 7.
7) M. D. Ker, T. Y. Chen and C. Y. Wu: *Proc. IEEE Int. Symp. Circuits & Systems, Sydney, Australia, 2001* (IEEE, New York, 2001) p. 754.