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ESD robustness of thin-film devices with different layout structures in LTPS technology

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Abstract

The electrostatic discharge (ESD) robustness of different thin-film devices, including three diodes and two thin-film transistors (TFTs) in low-temperature polysilicon (LTPS) technology, is investigated. By using the transmission line pulse generator (TLPG), the high-current characteristics and the secondary breakdown current (It2) of these thin-film devices are observed. The experimental results with different parameters and layout structures of these LTPS thin-film devices have been evaluated for optimizing ESD protection design for liquid crystal display (LCD) panel.

1. Introduction

Low-temperature polysilicon (LTPS) thin-film transistors (TFTs) have been widely used in active matrix liquid crystal display (AMLCD) because their electron mobility can be 100 times faster than that of the conventional amorphous silicon (α-Si:H) TFTs [1]. Many small-size to mid-size AMLCDs fabricated by LTPS technology have been used in mobile phone, digital camera, notebook, and so on. The state-of-the-art design efforts focus on realization of system-on-panel (SOP) application [2,3] to integrate more control and driver circuits on the glass substrate.

The electrostatic discharge (ESD) is one of the major reliability concerns in integrated circuits (ICs) [4], and it is also the most critical issue on the flat display panel to reduce the production yield [5]. When the large glass panel is delivered or assembled in the factory, the insulator material or the process machines could accumulate considerable static charges by triboelectric and field-induced charging. Since the fabricated material used for thin-film devices has a low thermal conductivity, the heat generated by ESD current cannot be efficiently dissipated in contract to the CMOS devices in deep substrate with a low thermal resistance. At the secondary breakdown point, the stressed device reaches a critical temperature by ESD to initiate thermal runaway [6]. With joule heating consideration [7], the ESD reliability of LTPS thin-film devices becomes more serious when the design rules are shrunk to make more devices and circuits integrated on LCD panel.

Compared to silicon-based CMOS technology, a few papers were studied on thin-film devices under ESD-stress condition [8–13]. Under the system level ESD test [14], the ESD reliability of panel was tested by an ESD gun with a voltage level of several kV [8]. At the device level, α-Si TFTs under machine-model (MM) ESD test [15] and under transmission line pulsing (TLP) test [16] were studied [8–11]. The transmission line pulsing (TLP) system with a 100-ns current pulse was used to investigate ESD degradation on LTPS TFTs [12,13]. The device dimension of TFTs studied in [8–13] was so small that they could not sustain high ESD current and failed as long as they were turned on. Therefore, only the failure result on TFTs after different over-voltage stress conditions is demonstrated. No high-current characteristic of TFT under ESD-stress condition was presented in those published papers.

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In this work, three diodes and two TFTs with different structures and geometry layout parameters fabricated in LTPS technology are tested to evaluate their ESD robustness by the TLP-measured secondary breakdown current (It2).

2. Device structures

In the LTPS process, a buffer oxide and an α-Si:H film were deposited on glass substrate by plasma enhanced chemical vapor deposition (PECVD) system and then the XeCl excimer laser was used to crystallize this film [17]. The thickness of α-Si film deposited in this work is about 50 nm. After active islands were defined, the ion doping process was carried out to form the P^- and the N^+ regions. Following, double gate insulator films, SiO_X and SiN_X, were deposited by PECVD system. The gate metal Mo was deposited and then patterned. Subsequently, the N^- and P^+ ion dopings were implanted in the lightly doped drain (LDD) region and the P^+ region of LTPS TFT on panel, respectively. Here, the N^- doping is a self-aligned process without extra mask. After all ion doping processes were completed, the doping activation was performed by rapid thermal annealing (RTA). All implanted junctions directly reach to the underlying buffer oxide. Moreover, hydrogenation was used to improve the device performance [18]. Finally, all LTPS thin-film devices, including diodes and transistors, were finished after their contact holes and metal pads formation.

The LTPS thin-film diodes, as shown in Fig. 1(a)–(c), formed by different doping types in the center region are named as the P^+–P^-–N^+ diode, the P^+–N^-–N^+ diode, and the P^+–i–N^+ diode, respectively. To avoid implanting N^- doping in center regions of the P^+–i–N^+ diode and the P^+–P^-–N^+ diode, the gate metal must be formed above center regions for the shielding mask application. The spacing S

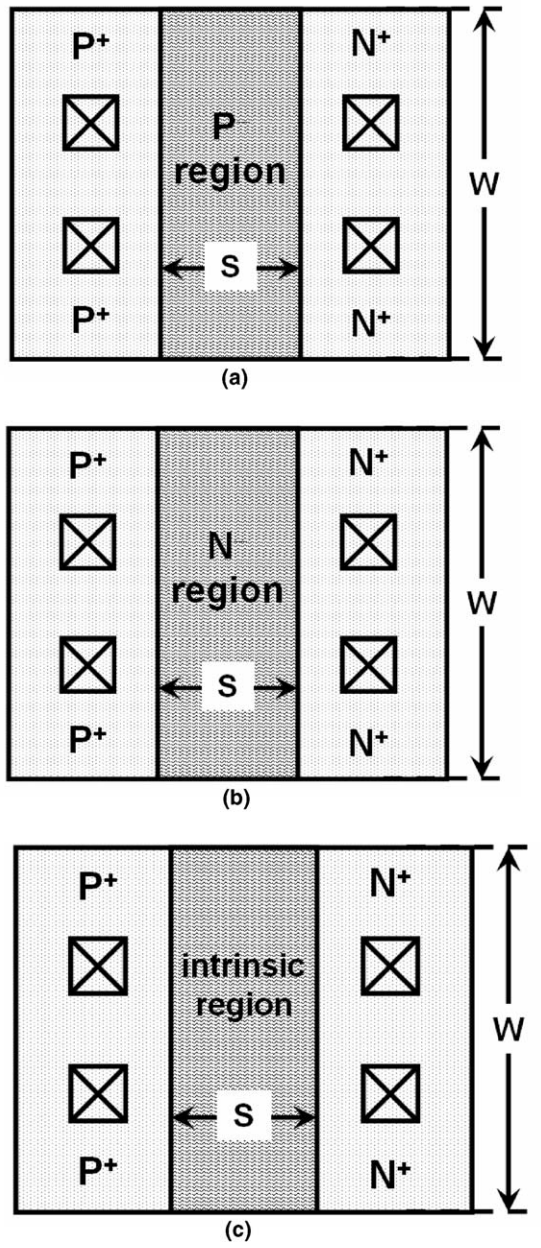

Fig. 1. The layout top views of three LTPS thin-film diodes with (a) P^-, (b) N^-, and (c) intrinsic, ion doping in the center region.

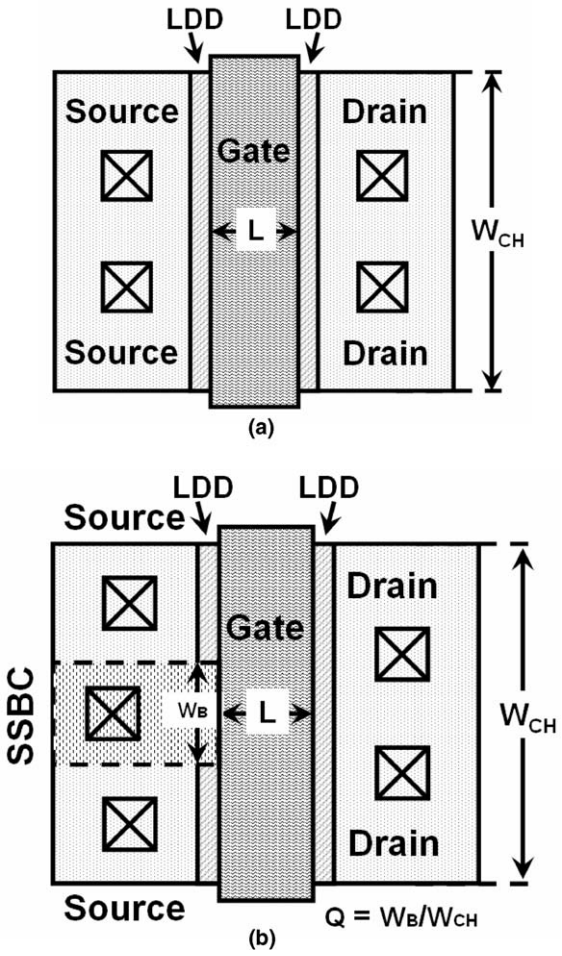

Fig. 2. The layout top views of (a) the conventional N-type TFT, and (b) the source-side-body-contact (SSBC) N-type TFT, in LTPS technology.

of LTPS diodes varied from 2 μm to 10 μm is the main layout parameter for ESD consideration. The conventional N-type TFT with an LDD structure is shown in Fig. 2(a). The source-side-body-contact (SSBC) N-type TFT with a P^+ body pickup in the source region is shown in Fig. 2(b). The SSBC percentage of SSBC TFT is defined by a Q factor of W_B/W_{CH}. W_B and W_{CH} are the source-side-body-contact width and the channel width, respectively. All LTPS thin-film devices are drawn in finger style, which each finger has a width of 50 μm. The total widths of LTPS diodes and LTPS TFTs are drawn as 400 μm and 600 μm on the test panel, respectively. The channel length (L) varies from 3 μm to 15 μm and the Q factor is also drawn in different values to verify their impact on ESD robustness of LTPS TFTs.

3. Experimental results and discussion

3.1. TLPG system for LTPS thin-film devices

To investigate ESD robustness of CMOS devices, TLPG system has been used to measure their turn-on resistance (R_{device}) and second breakdown current (It2) [19]. From the TLPG measurement results, the human body model (HBM) [20] ESD level (VESD) can be approximated as [21]

$$\text{VESD} \approx (1.5\ \text{k}\Omega + R_{device}) \times \text{It2}, \quad (1)$$

where 1.5 kΩ is the equivalent resistance of human body. Therefore, the device with a larger It2 value is expected to have a higher HBM ESD level.

The configuration of TLPG system applied for LTPS thin-film devices is shown in Fig. 3. The transmission line is initially charged by the high voltage source, and then it generates a 100-ns current pulse into the device under test (DUT) on the probe station. The TLP-current and TLP-voltage waveforms are monitored on the oscilloscope by current probe and voltage probe, respectively. The sensitivity of the current probe is 5 mV/1 mA. The shunt resistor (R_M) with an impedance of 50 Ω is added between the DUT and the transmission line for impendence matching. Therefore, the stimulated ESD current generated by TLPG system can completely inject into the high-resistance DUT.

The failure criterion is defined when the permanent damage is observed to cause a huge leakage current (over 1 μA) or an open characteristic on the thin-film device, DUT. After the DUT is damaged, the DUT will have an abnormal turn-on resistance so that the measured waveforms on the oscilloscope are changed abruptly. The damaged junction seems to be melted from the TLP-current injected node to the thin active channel. The failure spot region is hollow with almost no poly-Si film. It causes a large series resistance at the injected side with an open or short characteristic. This result is unlike in silicon-based CMOS device under TLP stress, which presented only large leakage current to the deep substrate after the CMOS device fails. As shown in Fig. 4(a), with the TLP energy increasing step-by-step, the TLP-voltage and the TLP-current waveforms are almost kept as square pulses before the DUT fails. On the contrary, Fig. 4(b) shows that the TLP current sharply increases but with the TLP voltage decreasing after the DUT fails. Therefore, from the TLP I–V curves, It2 of the DUT can be obtained by increasing TLP current step-by-step until the permanent damage occurs.

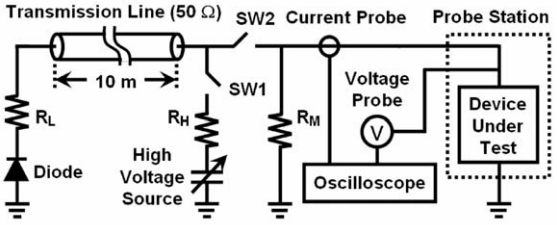

Fig. 3. The configuration of TLPG system used to measure the LTPS thin-film devices.

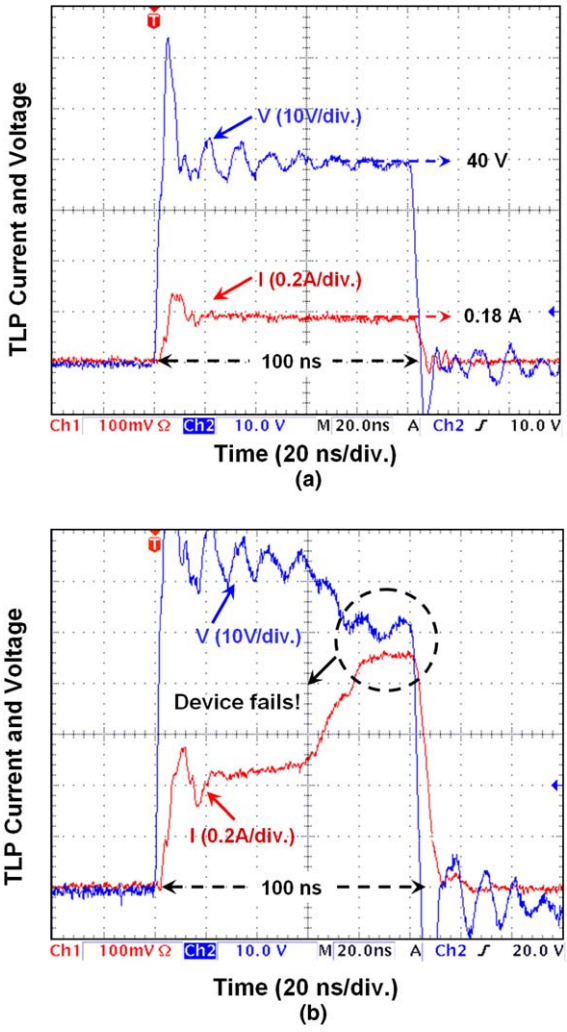

Fig. 4. The TLP waveforms on LTPS thin-film devices are monitored by the oscilloscope (a) before and (b) after the device fails.

3.2. TLP I–V characteristics of LTPS thin-film diodes

The diode is usually used as the ESD protection device in CMOS technology because it has good ESD robustness within a small device dimension. However, the LTPS diode with a small dimension cannot sustain such high ESD current stress due to hard heat dissipation. The TLP *I–V* curves of different LTPS diodes with dimension (*W*/*S*) of 400 μm/5 μm under forward-biased condition are shown in Fig. 5, where a TLP-current pulse injects from the P^+ node to the N^+ node. The P^+–P^-–N^+ diode has the smallest turn-on resistance in the TLP *I–V* curves, corresponding with the highest It2 among these thin-film diodes under forward TLP stress. When the TLP current is smaller than 0.3 A, the P^+–N^-–N^+ diode without gate-metal shielding above the center region has the largest turn-on resistance among three diodes. On the contrary, the P^+–i–N^+ diode and the P^+–P^-–N^+ diode have gate-metal shielding above their center regions, which can improve the turn-on efficiency. Especially, the TLP *I–V* curve of the P^+–N^-–N^+ diode has a skew characteristic due to the unsettled process of N^- ion doping and no gate-metal shielding above the P^+–N^-–N^+ diode. The N^- ion doping in the LTPS process is designed for the LDD structure in N-type TFT to improve the device reliability. However, the N^- ion dopants in the poly-Si film are hardly activated during RTA process, compared with the P^+ ion dopants. When the TLP current is greater than 0.3 A, the carriers are filled within the N^- center region of the P^+–N^-–N^+ diode during TLP stress. Therefore, the turn-on resistance of the P^+–N^-–N^+ diode under over 0.3-A TLP-current stress becomes smaller than that of the other two LTPS diodes.

The relations between It2 and the spacing S among these three different LTPS diodes under forward TLP stresses are shown in Fig. 6. As the spacing *S* is increased from 2 μm to 10 μm, the It2 of these diodes is decreased gradually under forward TLP stress. While the spacing *S* is smaller than 5 μm, the It2 values of the P^+–P^-–N^+ diode and the P^+–N^-–N^+ diode dominated by the turn-on resistance in the center region are higher than that of the P^+–i–N^+ diode. Besides, the reason why the It2 of the P^+–N^-–N^+ diode degrades abruptly when the spacing *S* of the P^+–N^-–N^+ diode is larger than 5 μm is the skew TLP *I–V* curve caused larger TLP voltage on the device at the same TLP current. The skew TLP *I–V* curve causes larger power dissipation on the P^+–N^-–N^+ diode with a longer spacing *S*. Therefore, the It2 is below 0.45 A if the spacing *S* of the P^+–N^-–N^+ diode is longer than 9 μm, as shown in Fig. 6.

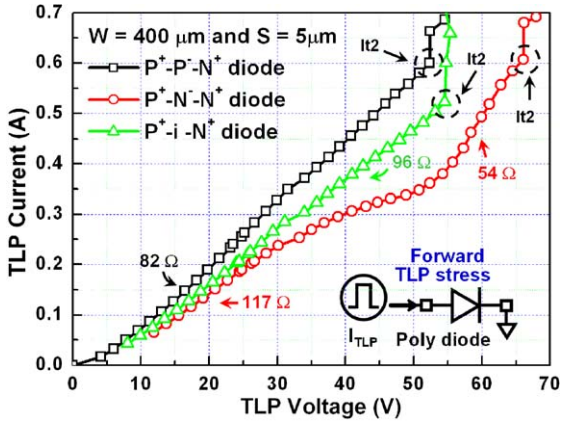

Fig. 5. The TLP-measured *I–V* curves of three different LTPS diodes under forward TLP stress.

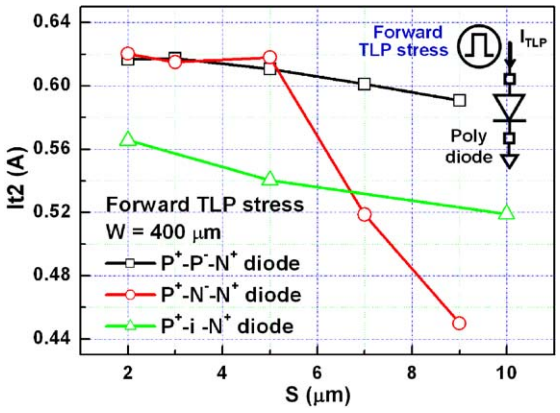

Fig. 6. The relations between It2 and the spacing *S* of different LTPS diodes under forward TLP stress.

The It2 values of these LTPS diodes under reverse TLP stress are all below 0.3 A, and they are much smaller than those under forward TLP stress. The diode under reverse TLP stress conducts the TLP current by the junction breakdown. The LTPS diode with the spacing *S* of 5 μm under reverse-biased condition has a junction breakdown voltage of 40 V. Such reverse breakdown voltage in TLP measurement is increased with the increasing spacing *S*. The long-spacing diode under reverse-biased condition has more power dissipation during ESD stress. So, the LTPS diode under reverse-biased condition has weak ESD robustness. In summary, the LTPS diode should be designed to conduct ESD current under forward-biased condition for achieving good ESD robustness, especially using the P^+–P^-–N^+ diode.

3.3. TLP I–V characteristics of LTPS TFTs

The TLP *I–V* characteristics of LTPS TFTs are also investigated in this work. The TFT has three terminals, drain, source, and gate. If a TFT is used as an ESD protection device at the input pad, it must be kept in off-state under normal circuit operation. The N-type TFT is under reverse TLP stress when a positive TLP (ESD) current injects from drain to source with the gate of N-type TFT connected to the grounded source. On the contrary, when a positive TLP (ESD) current injects from source to drain, the N-type TFT is under forward TLP stress. Because the source of SSBC N-type TFT is grounded under normal circuit operation, the extra P^+ region in source region does not interfere with the normal function on panel.

Fig. 7 shows the TLP-measured *I–V* curves of conventional and SSBC N-type TFTs with the same device dimension of 600 μm/5 μm under reverse TLP stress. Here, the source-side-body-contact (SSBC) percentage of SSBC N-type TFT has a factor *Q* of 14%. The schematic circuit of TFT under reverse TLP stress is also inserted in Fig. 7. The relations of It2 and different channel lengths (*L*) between SSBC and conventional N-type TFTs under reverse TLP stress are compared in Fig. 8. The It2 of these N-type TFTs is decreased when *L* is increased from 3 μm to 15 μm. Moreover, the It2 of SSBC N-type TFT is higher than that of conventional one. When a TFT is subjected to a high voltage or current stress, it generates many electron–hole pairs in the channel to cause serious degradation. Although the SSBC N-type TFT conducts the TLP current by drain junction breakdown during such high-current stress, its P^+ body pickup in the source region can absorb these hot holes generated in channel to alleviate the device degradation [22]. Consequently, the ESD robustness of SSBC N-type TFT can be improved under reverse TLP stress.

Fig. 9 shows the TLP-measured *I–V* curves of conventional and SSBC N-type TFTs with the same device dimension under forward TLP stress. Under forward TLP stress, the It2 of SSBC N-type TFT with a forward-biased diode path in the active channel is larger than that of conventional one. This result indicates that the SSBC N-type TFT can sustain higher ESD current under forward TLP stress. Moreover, the TLP current is discharged by device turn-on mechanism but not by junction breakdown when the N-type TFT is under forward-biased condition that the energy band diagram suits the electron existence. Consequently, the TFT under forward TLP stress has a higher It2 than that under reverse TLP stress, compared with Figs. 7 and 9. Fig. 10 indicates that the It2 values of SSBC and conventional N-type TFTs are function of different channel lengths (*L*) under forward TLP stress. The thin-film device with a longer *L* has a lower forward diode efficiency so that the It2 values of SSBC and conventional N-type TFTs with long channel lengths are almost the same under forward TLP stress. Particularly, under forward TLP stress, the short-channel device applied the electrical field near the drain and the gate insulator causes high energy carriers crowding in channel surface to reduce its It2, especially in the conventional N-type TFT with a channel length of 3 μm.

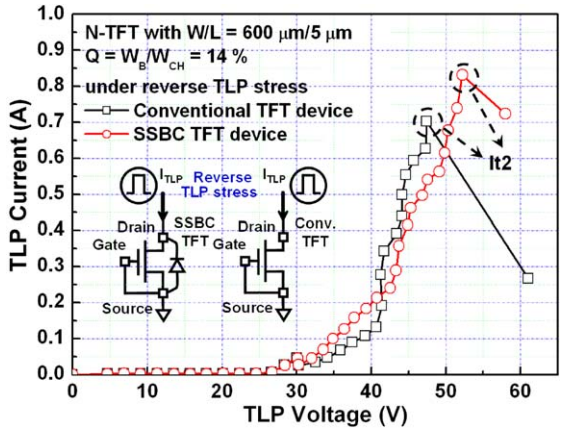

Fig. 7. The TLP-measured *I–V* curves of conventional N-type TFT and SSBC N-type TFT under reverse TLP stress.

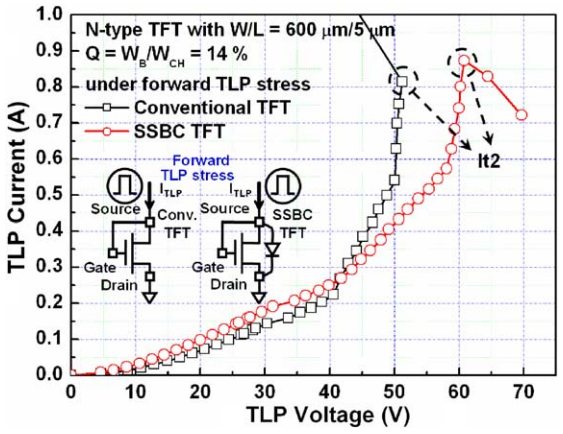

Fig. 9. The TLP-measured *I–V* curves of conventional N-type TFT and SSBC N-type TFT under forward TLP stress.

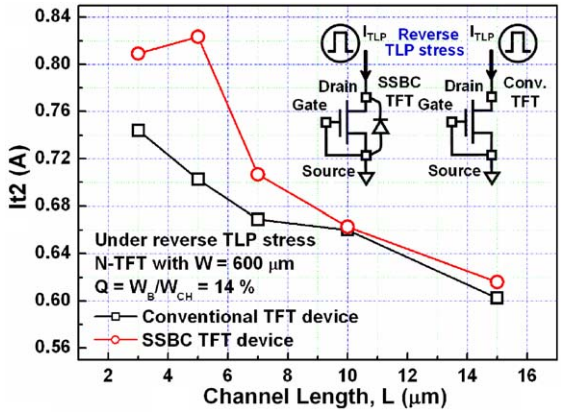

Fig. 8. The dependence on It2 and channel length of conventional N-type TFTs and SSBC N-type TFTs under reverse TLP stress.

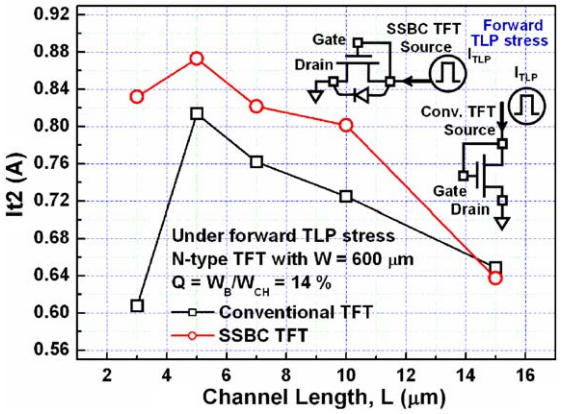

Fig. 10. The dependence on It2 and channel length of conventional N-type TFTs and SSBC N-type TFTs under forward TLP stress.

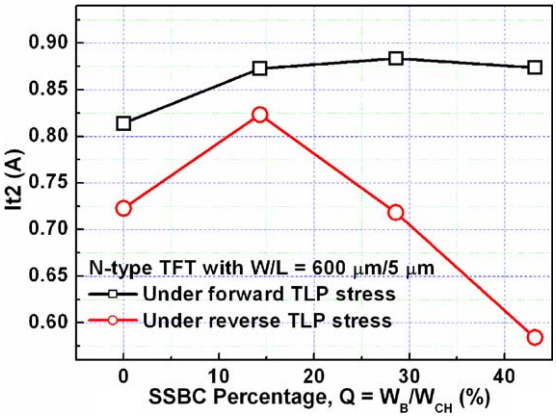

Fig. 11. The dependence of It2 on SSBC percentage in the test structure under forward and reverse TLP stresses.

After the TLP characteristics of SSBC N-type TFTs are investigated, the influence on SSBC percentage defined by a Q factor of W_B/W_{CH} is studied here. The It2 values of SSBC N-type TFTs under forward TLP stresses are larger than 0.86 A with the increasing Q factor, as shown in Fig. 11. Even if the P^+ body pickup in the source region can alleviate the device degradation, the It2 values of SSBC N-type TFTs under reverse TLP stress are decreased with the increasing Q factor. When the Q factor is increased from 14% to 42%, the It2 of SSBC N-type TFT is decreased from 0.81 A to 0.56 A under reverse TLP stress. The reason is that the SSBC N-type TFT with the increasing Q factor under reverse TLP stress resembles the P^+–P^-–N^+ diode structure under reverse-biased condition which has a lower It2 value. So, the N-type TFT with a Q factor of 14% in source region can obtain a higher It2 value, no matter under forward or reverse TLP stress.

4. Applications for whole-panel ESD protection

With more ESD problems, the on-panel ESD protection designs were proposed by some companies [23–25]. The common ESD protection architecture used in LCD panel with an ESD bus around panel and the ESD protection element at each input pad is shown in Fig. 12. The ESD protection element has two nodes. One node is connected to the input pad and the other node is connected through the ESD bus to another node of ESD protection element. Wherever the ESD current injects into an input pad, the ESD energy can be quickly released from the injected input pad to the grounded pad through the ESD bus, so that the TFTs on panel are prevented from ESD damage. In α-Si technology, the ESD bus fabricated on panel is just a wide metal line to quickly conduct ESD current. In LTPS technology, however, the number of input pads can be reduced because the most circuits have been integrated on panel, such as DC-to-DC convectors, shift register circuits, or driving circuits. The circuits on panel need individual supply powers to control every scan line and data line under normal circuit operation. Therefore, in LTPS technology,

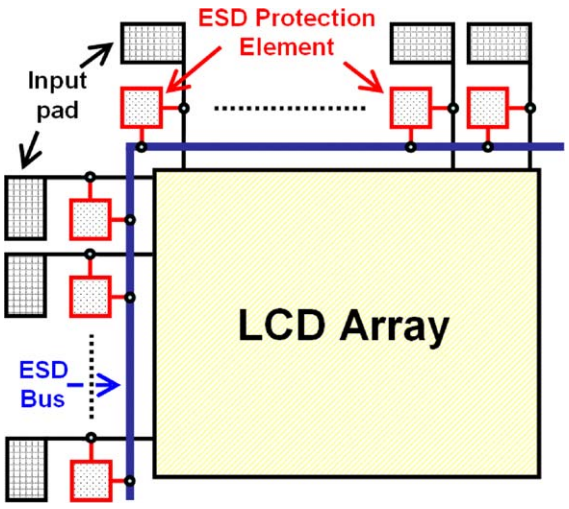

Fig. 12. The common ESD protection architecture contains an ESD bus around LCD panel and the ESD protection element at each input pad.

the wide enough power line at each input pad can be also used as the ESD bus on panel for ESD protection.

In this work, the whole-panel ESD protection design with the ESD protection element at each input pad and power-rail ESD clamp circuit on LTPS LCD panel is shown in Fig. 13. This whole-panel ESD protection design can discharge the ESD current by all forward-biased paths but not reverse-biased paths among four ESD-zapping modes, including the positive-to-VSS (PS) mode, the negative-to-VDD (ND) mode, the positive-to-VDD (PD) mode, and the negative-to-VSS (NS) mode. If a PS-mode ESD zap is applied at one input pad, the main ESD current flows through the LTPS diode in forward-biased path to VDD power line, and then it is discharged through the ESD clamp device (MESD) to ground by device turn-on mechanism. This on-panel ESD protection architecture can conduct the ESD current through the forward-biased paths under any pin-to-pin ESD-zapping conditions.

The power-rail ESD clamp circuit is designed to conduct ESD current when the ESD voltage drops across the VDD and VSS power lines, but to be kept off when the panel is under the normal power-on condition [26]. The rise time of an ESD voltage is within 10 ns. The voltage level of the node Vx in the power-rail ESD clamp circuit increases

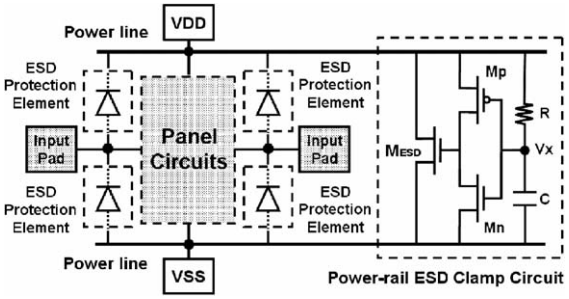

Fig. 13. The schematic view of the ESD protection design on LCD panel with the ESD protection elements at input pads and the power-rail ESD clamp circuits between power lines.

more slowly than that of the VDD power line because the resistor–capacitor (R–C) circuit has a time constant in the order of microseconds (μs) [26]. A 2.2-in. LCD panel with the P^+–i–N^+ diodes at each input pad and four power-rail ESD clamp circuits, whose adjacent distance is about 5500–7000 μm among the power lines of LCD panel, has successfully achieved a machine-model (MM) ESD level of 275 V [27]. From the TLP I–V characteristics of LTPS thin-film devices in previous section, if the P^+–i–N^+ diodes and the ESD clamp device (MESD) are replaced by the P^+–P^-–N^+ diodes and the SSBC N-type TFT, respectively, the ESD robustness of LCD panel can be further improved.

5. Conclusion

The ESD robustness of LTPS thin-film devices fabricated on LCD panel has been investigated in this work. The modified TLPG system with a shunt resistor of 50 Ω for impedance matching is used to measure the secondary breakdown current (It2) of LTPS thin-film devices. The P^+–P^-–N^+ diode under forward TLP stress has the best ESD robustness among three LTPS thin-film diodes due to its small turn-on resistance, which depends on the doping type and the spacing S in the center region. The skew TLP I–V curve of the P^+–N^-–N^+ diode causes a lower It2 owing to larger power dissipation. The LTPS diode under reverse TLP stress has worse ESD robustness because it discharges the ESD current by junction breakdown. On the other hand, the LTPS TFT under forward TLP stress is more robust than that under reverse TLP stress. Besides, the It2 of SSBC N-type TFT with a Q factor of 14% is higher than that of conventional one, no matter under forward or reverse TLP stresses. The whole-panel ESD protection design with P^+–i–N^+ diodes and power-rail ESD clamp circuits has gained a machine-model (MM) ESD level of 275 V in a practical LCD panel product. The P^+–P^-–N^+ diode and the SSBC N-type TFT are the best ESD protection devices to achieve whole-panel ESD protection scheme in LTPS technology.

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