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PAPER

A CMOS Bandgap Reference Circuit for Sub-1-V Operation without Using Extra Low-Threshold-Voltage Device

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SUMMARY A new sub-1-V CMOS bandgap voltage reference without using low-threshold-voltage device is presented in this paper. The new proposed sub-1-V bandgap reference with startup circuit has been successfully verified in a standard 0.25-μm CMOS process, where the occupied silicon area is only 177 μm × 106 μm. The experimental results have shown that, with the minimum supply voltage of 0.85 V, the output reference voltage is 238.2 mV at room temperature, and the temperature coefficient is 58.1 ppm/°C from −10°C to 120°C without laser trimming. Under the supply voltage of 0.85 V, the average power supply rejection ratio (PSRR) is −33.2 dB at 10 kHz.

key words: *voltage reference, bandgap voltage reference, temperature coefficient, PSRR (power supply rejection ratio), startup circuit*

1. Introduction

Low voltage and low power are two important design criteria in both analog and digital systems. It has been expected that the whole electronic system will be operated down to a single 1-V supply in near future. The bandgap reference (BGR) generators which can be operated under 1-V supply have been widely used in DRAM, flash memories, and analog-to-digital converter (ADC). So far, many techniques have been proposed to develop voltage or current references, which can be almost independent to temperature and power-supply voltage. The bandgap reference is the major design to provide a precision voltage reference with low sensitivity to the temperature and the supply voltage.

When CMOS technologies enter the nano-scale eras, the demand for battery-operated portable equipments will increase. The supply voltage has been scaled down from 1.8 V (in 0.18-μm technology) to 1.2 V (in 0.13-μm technology), and will drop to only 0.9 V in the next generation technology [1]. In CMOS technology, the parasitic vertical bipolar junction transistor (BJT) had been commonly used to implement P-N junction of the bandgap reference. But, the traditional CMOS bandgap reference circuits did not work in sub-1-V supply voltage. The reason, that the minimum supply voltage can not be lower than 1 V, is constrained by two factors. One is the bandgap voltage of around 1.25 V in silicon [2]–[11], which exceeds 1 V supply. The other factor is that the low-voltage design of the proportional to absolute temperature current generation loop is limited by the input common-mode voltage of the amplifier [2], [5]. These two limitations can be solved by using the resistive subdivision methods [6], [7], low-threshold voltage (or native) device [6]–[8], BiCMOS process [5], or DTMOST device [9]. However, those approaches often require specialized processes and characterization, which increase fabrication cost and process steps.

In this work, a new bandgap reference is proposed, which can be successfully operated with sub-1-V supply in a standard 0.25-μm CMOS process without special process technology [12]. Without laser trimming, the new proposed bandgap voltage reference has been proven in the silicon chip with a stable output voltage V_{REF} of 238.2 mV at room temperature and a temperature coefficient of 58.1 ppm/°C under VDD power supply of 0.85 V.

2. Traditional Bandgap Reference Circuit

A typical implementation of bandgap reference in CMOS technology is shown in Fig. 1. In this circuit, the output is the sum of a base-emitter voltage (V_{EB}) of BJT and the voltage drop across the upper resistor. The BJTs (Q_1 and Q_2) are typically implemented by the diode-connected vertical PNP bipolar junction transistors. The output voltage of the traditional bandgap reference circuit can be written as

$$V_{REF-TRAD} = V_{EB2} + \frac{R_2}{R_1} V_T \ln\left(\frac{A_1}{A_2}\right), \quad (1)$$

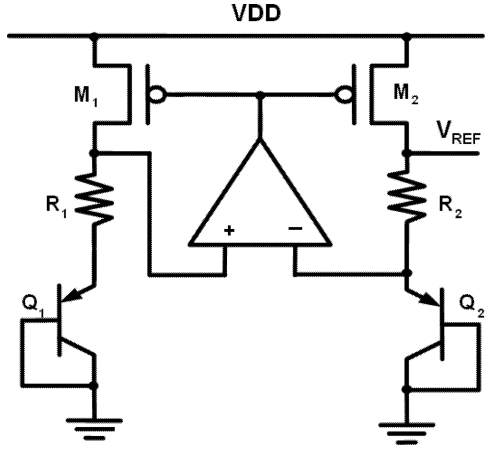

Fig. 1 The traditional bandgap reference circuit in CMOS technology.

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where A_1 and A_2 is the emitter areas of Q_1 and Q_2, and V_T is the thermal voltage. The second item in (1) is proportional to the absolute temperature (PTAT), which is used to compensate the negative temperature coefficient of V_{EB}. Usually, the V_{PTAT} voltage comes from the thermal voltage V_T with a temperature coefficient about + 0.085 mV/°C, which is quite smaller than that of V_{EB}. After multiplying V_{PTAT} with an appropriate factor and summing with V_{EB}, the bandgap reference will have a very low sensitivity to temperature. Hence, if a proper ratio of resistors is kept, an output voltage with very low sensitivity to temperature can be obtained. In general, the V_{REF} is about 1.25 V in CMOS process, so that the traditional bandgap reference circuit can not be operated in low voltage application, such as 1 V or below.

3. New Proposed Bandgap Reference Circuit

The design concept of the new proposed bandgap reference is that the two voltages (which are proportional to V_{EB} and V_T, respectively) are generated from the same feedback loop. The two-stage operational amplifier with p-channel input is used in this new proposed bandgap reference. The p-channel input has a lower input common-mode voltage than that of the n-channel input to keep the transistors working in the saturation region.

The new proposed bandgap reference is shown in Fig. 2, which uses the resistive subdivision R_{1a}, R_{1b}, R_{2a}, and R_{2b} to reduce the input common-mode voltage of the amplifier. The voltages V_1 and V_2 in Fig. 2 have a negative temperature coefficient as that of V_{EB}. In the traditional bandgap reference, the negative input of the operational amplifier is connected to V_{EB2}, whose value is varying from 0.65 V to 0.45 V when the temperature is changed from 0°C to 100°C. The minimum supply voltage (VDD) of the traditional bandgap reference circuit needs $V_{EB2} + 2|V_{DS\,sat}| + |V_{THp}|$. The V_{THp} is the threshold voltage of PMOS. The supply voltage of the traditional bandgap reference is more than 1 V. In Fig. 2, the dimensions of PMOS devices M_1 and M_2 are kept the same. The resistance of R_{1a} and R_{2a} is the same, and the resistance of R_{1b} and R_{2b} is also the same. Following the KCL at the nodes of V_1 and V_2 in Fig. 2, the node equation can be written as

$$\frac{\Delta V}{R_3} = \frac{V_{REF} - V_2}{R_4}, \tag{2}$$

$$\frac{\Delta V_{EB} - \Delta V}{R_{1a}} = \frac{\Delta V}{R_{1b}}, \tag{3}$$

where $\Delta V_{EB} = V_{EB2} - V_{EB1}$ and $\Delta V = V_2 - V_1$. According to Eqs. (2) and (3) reference voltage V_{REF} can be expressed as

$$\begin{aligned} V_{REF} &= \frac{R_{1b}}{R_{1a}+R_{1b}}\left[\left(R_4+\frac{R_{1a}R_{1b}}{R_{1a}+R_{1b}}\right)\frac{\Delta V_{EB}}{R_3} + V_{EB2}\right] \\ &= \frac{R_{1b}}{R_{1a}+R_{1b}}\left[V_{REF-TRAD} + \left(\frac{R_{1a}R_{1b}}{R_{1a}+R_{1b}}\right)\frac{\Delta V_{EB}}{R_3}\right]. \end{aligned} \tag{4}$$

The item of $V_{REF-TRAD}$ in (4) is identical to the traditional reference voltage in (1). In order to achieve sub-1-V operation, the ratio of $R_{1b}/(R_{1a} + R_{1b})$ is used to scale down the reference voltage level. Therefore, the minimum supply voltage of the new proposed bandgap reference can be effectively reduced to only

$$VDD_{(Min)} = V_2 + \left|V_{THp}\right| + 2\left|V_{DS\,sat}\right|. \tag{5}$$

The new proposed bandgap reference can be operated under sub-1-V supply voltage.

The whole complete circuit to realize the proposed sub-1-V bandgap reference is shown in Fig. 3. The circuit is composed of a bias circuit, a bandgap core, two startup circuits, and a two-stage operational amplifier. The bandgap reference circuit has two stable points. To ensure that it ends up to the correct state, a startup circuit must be added. The startup circuit for the bias circuit is used to avoid the bias circuit working in the zero-current state, which is realized by $M_{S1a} - M_{S3a}$ in Fig. 3 [3]. Similarly, another startup circuit is used to ensure that the input voltage of the amplifier is not kept at zero in the initial state. The M_{S1a} and M_{S2a} form a function of inverter in the startup circuit. The device dimensions (W/L) of M_{S2a} and M_{S2b} are chosen to be much less than one. When the circuit operates in zero-current state, the gate voltages of M_{S1a} and M_{S1b} are pulled high and close to VDD. The drain voltages of M_{S2a} and M_{S2b} are pulled low to turn on the M_{S3a} and M_{S3b}, which inject current to the bandgap core circuitry (by M_{S3b}) and the bias circuit (by M_{S3a}). The drain voltages of M_{B3} and M_4 are decreased, therefore the bandgap core circuitry and bias circuit start to operate. Once the drain voltage of M_{B4} and the gate voltages of M_1, M_2, M_{A1}, and M_{A6} are decreased, the drain voltages of M_{S1a} and M_{S1b} are pulled high to cut off M_{S3a} and M_{S3b}. The device dimensions (W/L) of M_{S2a} and M_{S2b} are critical since the loop of the bandgap reference could be destroyed, if M_{S3a} or M_{S3b} were not completely cut off after startup. To ensure a complete cutoff operation of M_{S3a} and M_{S3b}, the device dimensions (W/L) of M_{S3a} and M_{S3b} should be designed with the considerations of both maximum supply voltage and operating temperature [3]. The capacitors C_1 and C_2 are used to stabilize the circuit. The bulk and the source of the input pair transistors M_{A2} and M_{A3} in the amplifier should be connected together to avoid the body effect.

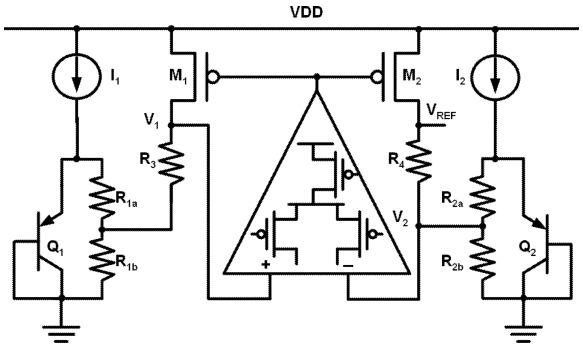

Fig. 2 The new proposed bandgap reference circuit for sub-1-V operation.

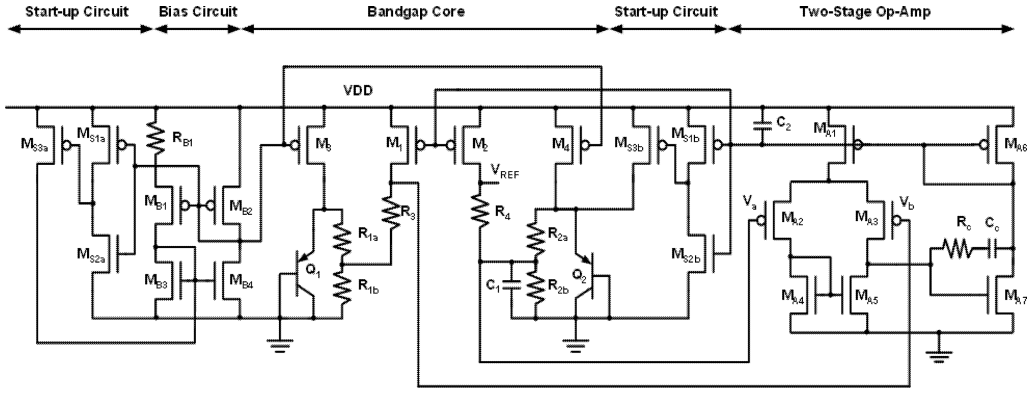

Fig. 3 Complete schematic of the new proposed bandgap reference.

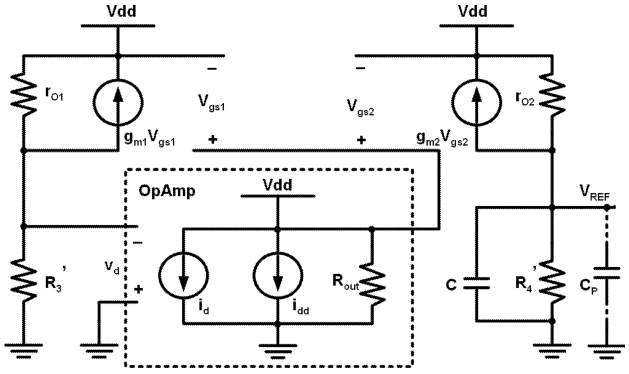

Fig. 4 Small signal model of the proposed bandgap reference.

In real-world applications, the power supply voltage is never perfect. It consists of a DC level plus AC noise caused by transient currents from circuit operations. Another important factor of the bandgap reference circuit operated in sub-1-V supply voltage is the power supply rejection ratio (PSRR) [13], which represents the resistance against the noise from the supply voltage in the unit of decibel (dB). The small-signal model of the proposed bandgap reference circuit with the operational amplifier of p-channel input is shown in Fig. 4, where only considers the noise from the supply voltage. The resistances of $R_3^{'}$ and $R_4^{'}$ in Fig. 4 are $R_3 + (R_{1a}//R_{1b})$ and $R_4 + (R_{2a}//R_{2b})$, respectively. The capacitor C is the parasitic drain-to-bulk junction capacitance of M_2. Since the turn-on resistance of the PNP transistors is small, both Q_1 and Q_2 can be simplified as short-circuit path to the ground. The amplifier is modeled with an output resistor R_{out} and two voltage-controlled current sources i_d and i_{dd}, which are driven by the differential input voltage v_d and power supply voltage v_{dd}, respectively. The power supply rejection ratio (PSRR) of this new proposed bandgap reference circuit, which is the ratio of the output reference voltage and the noise from the supply voltage, can be expressed as

$$\frac{V_{REF}(s)}{V_{DD(Noise)}(s)} = \frac{1}{sCr_{o2} + \dfrac{r_{o2}}{R_4^{'}} + 1}. \tag{6}$$

From (6), the PSRR of the proposed bandgap reference will become worse at high frequency. It is apparent that the pole location can be shifted by changing the capacitance at V_{REF} node. Moving the pole to the left in the s-plane will result in an improvement in high-frequency noise rejection. This can be achieved by inserting a capacitance C_p to ground at V_{REF} node. Thus, the PSRR in (6) is modified to

$$\frac{V_{REF}(s)}{V_{DD(Noise)}(s)} = \frac{1}{s(C + C_p)r_{o2} + \dfrac{r_{o2}}{R_4^{'}} + 1}. \tag{7}$$

A larger C_p provides better stability, but the startup time will become longer. The pre-regulated circuit [14] also used to improve the PSRR of the bandgap circuit. However, minimum supply voltage is the tradeoff.

The operational amplifier in Fig. 3 under sub-1-V operation has a limited gain. Thus, there will be a nonzero input-referred offset voltage V_{OS}. Considering the offset voltage of V_{OS}, the V_{REF} in (4) including the offset voltage can be written as

$$V_{REF} = \frac{R_{1b}}{R_{1a}+R_{1b}}\left[\left(R_4+\frac{R_{1a}R_{1b}}{R_{1a}+R_{1b}}\right)\frac{\Delta V_{BE}}{R_3}+V_{BE2}\right] - \frac{R_4}{R_3}V_{OS}. \tag{8}$$

The offset voltage, V_{OS}, is a temperature dependent voltage. To reduce the impact of V_{OS} on V_{REF}, the ratio of R_4/R_3 should be designed as small as possible.

4. Experimental Results

4.1 Simulation

The proposed bandgap reference circuit has been simulated by varying its operating temperature from 0 to 100°C. The dependence of V_{REF} (output reference voltage) on the operating temperature is shown in Fig. 5 under difference power supply voltage (from 0.8 to 1.1 V). The temperature coefficient is around 75 ppm/°C with the supply voltage of 0.85 V. With supply voltage of 0.8 V, the temperature coefficient grows sharply to be above 200 ppm/°C. The dependence of V_{REF} on the supply voltage is shown in Fig. 6 under

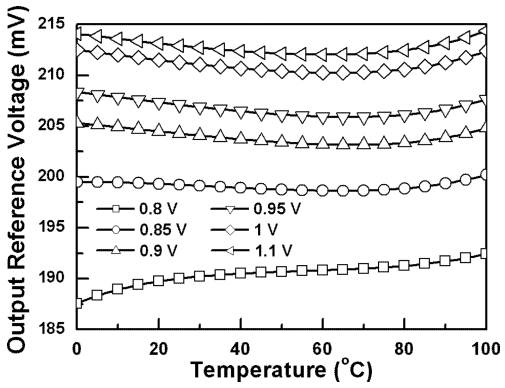

Fig. 5 Simulated reference voltage of the proposed bandgap reference with different supply voltages.

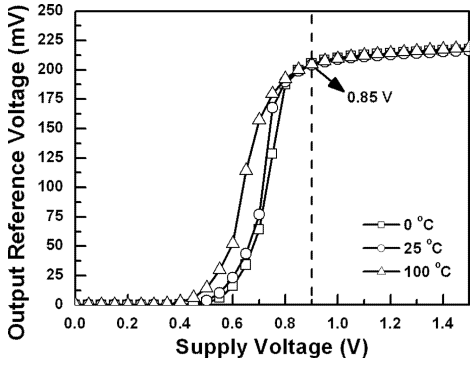

Fig. 6 Simulated minimum supply voltage of the proposed bandgap reference.

the temperatures of 0, 25, and 100°C. The curves of output reference voltages under the temperatures of 0, 25, and 100°C grow together while the supply voltage of the proposed bandgap reference is above 0.85 V. This means that the minimum supply voltage for the new proposed bandgap reference can be as low as 0.85 V. The PSRR at low frequency of the proposed bandgap reference, which works in the low supply voltage of 0.85 V, is −30.2 dB.

4.2 Silicon Verification

The proposed bandgap reference circuit has been fabricated in a 0.25-m single-poly-five-metal (1P5M) CMOS process. Figure 7 shows the overall die photo of the new sub-1-V bandgap reference circuit. The occupied silicon area of the new proposed bandgap reference circuit is only $177\,\mu\text{m} \times 106\,\mu\text{m}$. The active devices (MOSFETs) have been drawn in a common centroid layout to reduce process mismatch effect. The bipolar transistors in this chip are the parasitic vertical PNP BJTs in CMOS process. The ratio between the emitter areas of Q_1 and Q_2 is 8. The total emitter area of Q_1 is $200\,\mu\text{m}^2$ and that of Q_2 is $25\,\mu\text{m}^2$ in the layout. The resistors in this chip are formed by salicided ploy resistors, which have minimum process variation to improve the accuracy of resistance ratio. The bandgap reference circuit has been measured by varying its operating temperature from −10 to 120°C. The power supply voltage was set from 0.8 to 1.2 V. The measured results are shown in Fig. 8. The measured temperature coefficient of the new proposed bandgap reference circuit is around 58.1 ppm/°C under the supply voltage of 0.85 V. The dependence of output reference voltage on the *VDD* supply voltage under different temperatures is shown in Fig. 9. The experimental results in Fig. 9 have confirmed that the minimum supply voltage for this sub-1-V bandgap reference is 0.85 V.

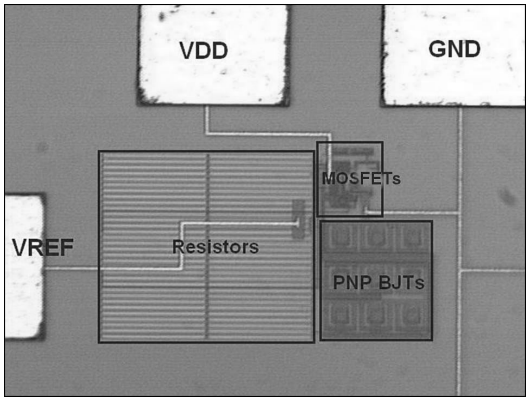

Fig. 7 Chip micrograph of the new proposed bandgap reference circuit fabricated in a 0.25-μm CMOS process.

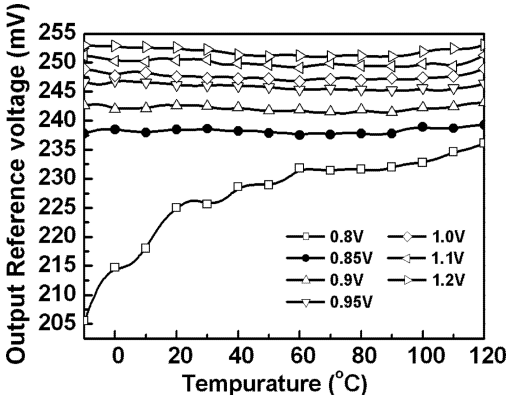

Fig. 8 Dependence of output reference voltage on the temperature under different *VDD* voltage levels.

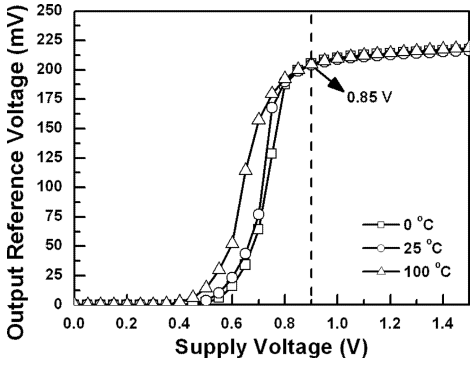

Fig. 9 Dependence of output reference voltage on the *VDD* supply voltage under different temperatures.

Table 1 Comparison among the low voltage bandgap references.

	This work	Ref. [2]	Ref. [3]	Ref. [7]
Technology (CMOS)	0.25 μm	1.2 μm	0.6 μm	0.4 μm
Minimum Supply Voltage	0.85 V	1.2 V	0.98 V	0.84 V
Temperature Coefficient	58.1 ppm/°C	100 ppm /°C	15 ppm /°C	59 ppm /°C
Extra Modification / Process	No	No	Laser Trimming	Native NMOS

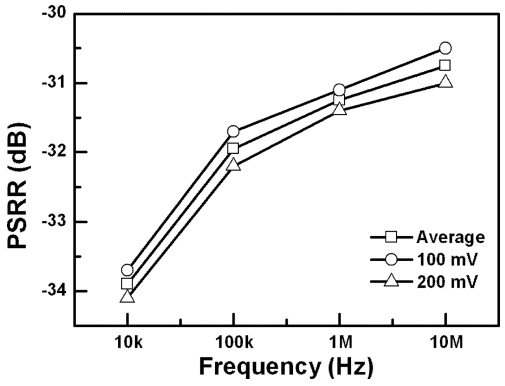

Fig. 10 Dependence of PSRR on the frequency under different input sinusoidal amplitudes.

About the measurement setup for power supply rejection ratio (PSRR), a sinusoidal ripple is added on power supply to measure the small-signal gain between the supply voltage and output reference voltage. The AC input signal at the power supply pin must include a DC offset that corresponds to the normal power supply voltage so that the bandgap reference circuit remains powered up [15]. The dependence of measured PSRR on the frequency under different input sinusoidal amplitudes is shown in Fig. 10. The averaged power supply rejection ratio (PSRR) is −33.8 dB at 10 kHz, whereas the reference output voltage is 238.2 mV at 25°C under the *VDD* power supply of 0.85 V. The comparison among the proposed sub-1-V bandgap reference of this work with other prior-art low voltage bandgap references is summarized in Table 1. The new proposed bandgap reference has the advantages of low operating voltage and low temperature coefficient in the general standard CMOS technology without special low-threshold-voltage device.

5. Conclusion

A CMOS bandgap voltage reference with V_{REF} of 238.2 mV and temperature coefficient of 58.1 ppm/°C, which consumes a maximum current of 28 μA at 0.85 V supply, has been presented. The sub-1-V operation of the bandgap reference has been successfully achieved in this work without using the low-threshold-voltage devices. Moreover, other techniques to achieve sub-1-V operation have been described, such as low voltage startup circuit and the lower common-mode input range of the amplifier by using the resistive subdivision method. Without using low-threshold-voltage device, the proposed bandgap reference circuit can be implemented in general CMOS technology.

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