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ESD PROTECTION FOR SLEW-RATE-CONTROLLED OUTPUT BUFFER IN A 0.5 μm CMOS SRAM TECHNOLOGY

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Abstract—A new ESD protection design by using the well-coupled field-oxide device (WCFOD) is proposed to protect the slew-rate-controlled output buffer in a 0.5 μm *P*-well/*N*-substrate CMOS SRAM technology. The ESD transient voltage is coupled to the *P*-well of the ESD protection field-oxide device through a parasitic capacitor to trigger on the bipolar action of the field-oxide device. The ESD trigger voltage of the WCFOD can be lowered to below the snapback-breakdown voltage of the output *N*MOS transistor, so it provides effective ESD protection for the slew-rate-controlled output transistors without causing any degradation on the circuit performance. The coupling capacitor is made by inserting a poly layer right under the wire-bonding metal pad without the increase of layout area. A modified WCFOD structure is also proposed for output ESD protection in deep-submicron CMOS technology with polycide or salicide processes. Three conventional output ESD protection designs with the series resistor, the double-diode structure, and the field-oxide device, are also made for comparison. Five test chips with the same 256 K SRAM core but only different output ESD protection designs have been fabricated in a same wafer to practically verify the ESD protection efficiency of this proposed WCFOD and modified WCFOD structures.

1. INTRODUCTION

Electrostatic discharge (ESD) robustness of CMOS ICs had been found to be seriously degraded by the advanced submicron or deep-submicron CMOS technologies[1–3]. Especially, the drains of output transistors are often directly connected to the output pad to drive external load, so the output transistors are more sensitive to ESD stresses. In CMOS ICs, the output transistors had been conventionally used as ESD protection elements to protect the ICs and themselves. In order to improve ESD protection capability and also to drive/sink current to/from the external heavy load, the output transistors are generally designed with larger device dimensions. But, even with such larger device dimensions, the ESD reliability of output buffers is still much degraded by the advanced CMOS technologies[4–6]. One of the most important effects to degrade ESD robustness of output transistors is the LDD structure[1–6], which had been widely used in submicron CMOS devices to overcome the hot-carrier issue[7–9]. To improve ESD robustness of CMOS output buffers, some submicron CMOS technologies include an extra ''ESD implant'' mask into process flow to make a stronger device structure for ESD protection[10–13]. But, the cost of IC fabrication is also increased by the additional mask and process steps.

To improve ESD robustness of the output transistors, the symmetrical layout structure is much emphasized to realize the large-dimension output transistors by ensuring the uniform turn-on phenomenon along the multiple fingers of an output transistor[14–16]. To more emphasize the uniform turn-on phenomenon among the multiple fingers of an output *N*MOS, a dynamic gate-coupling design was reported to couple ESD transient voltage to the gate of output *N*MOS to achieve uniform ESD power distribution on the large-dimension output *N*MOS[16–18]. But in many practical applications, the output buffers with large device dimensions are often designed by the slew-rate-controlled technique to reduce the switching noise and the ground-bouncing level[19–25]. The poly gates of the slew-rate-controlled output *N*MOS is not in parallel to each other but in series to each other. A typical layout example of a slew-rate-controlled output *N*MOS is shown in Fig. 1(a), and the equivalent circuit diagram is shown in Fig. 1(b). There exists a series resistor between the gates of every two adjacent fingers of the output *N*MOS. These series resistors are designed to cause a time delay to one-after-one turn

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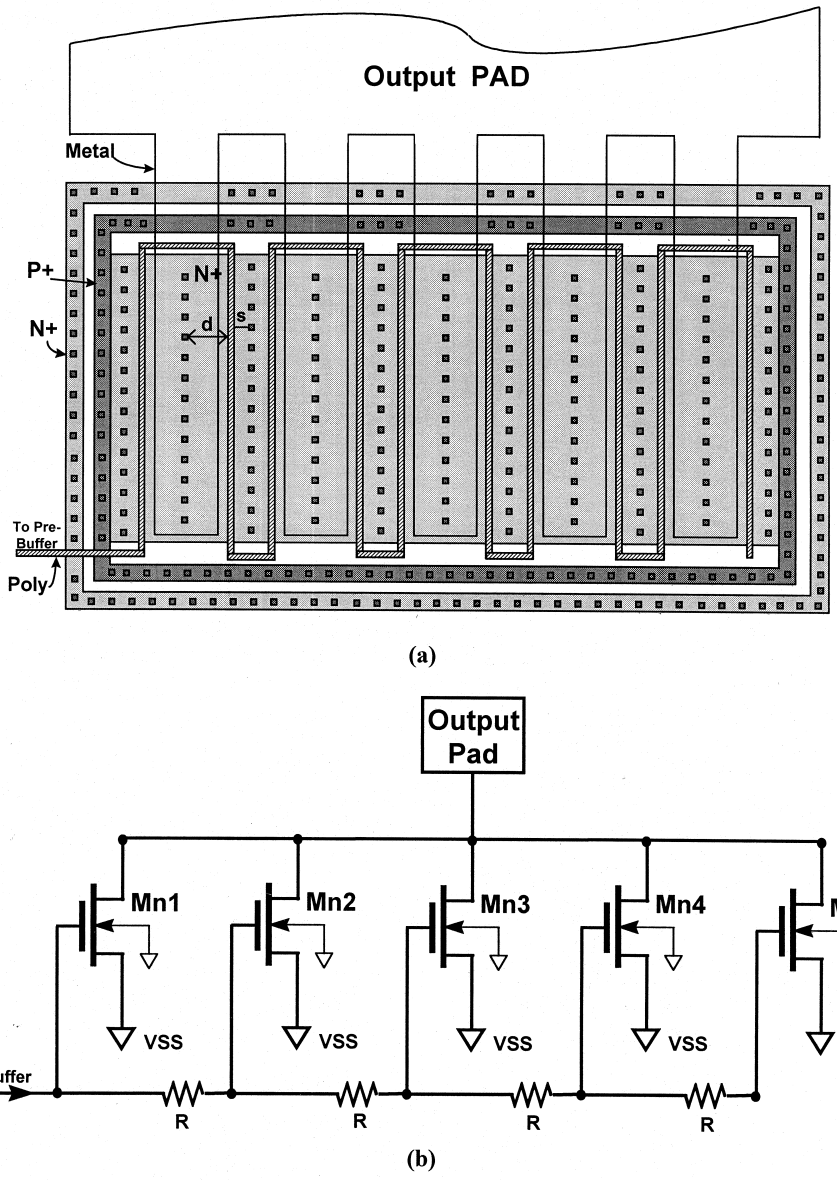


Fig. 1. The (a) schematic layout example, and (b) equivalent circuit diagram, of a slew-rate-controlled output *N*MOS.

on the fingers, so the d*i*/d*t* switching noise due to the turn-on of the output *N*MOS can be reduced. But in the slew-rate-controlled output buffer with series poly-gate connection, the uniform turn-on phenomenon of the finger-type output *N*MOS becomes absent. Due to the non-symmetrical resistance on the poly gate of each finger of the slew-rate-controlled output *N*MOS, the *RC* time constants among the fingers are quite different even if the gate-coupling design[16–18] is used to enhance the turn-on uniformity. This generally causes a very low ESD withstand level for a slew-rate-controlled output transistor even with a large device dimension.

Another commonly-used method to improve the ESD withstand level of output buffers is to adopt additional ESD protection elements to the output buffers[26–31]. The schematic circuit of a slew-rate-controlled output buffer with the additional ESD protection element is shown in Fig. 2, where the ESD protection element is added between the output buffer and the output pad. In[26–28], the drain of output *N*MOS is connected to the output pad by means of an extra resistor to improve its ESD robustness. This series resistor is used to limit ESD current toward output transistors, but they also limit the driving/sinking capability of output transistors. The timing specification of the output signal is also delayed by the series resistor. In[28–30], an extra *n*-type field-oxide device (or a lateral *n–p–n* bipolar junction transistor) was placed in parallel with the output *N*MOS to improve ESD robustness

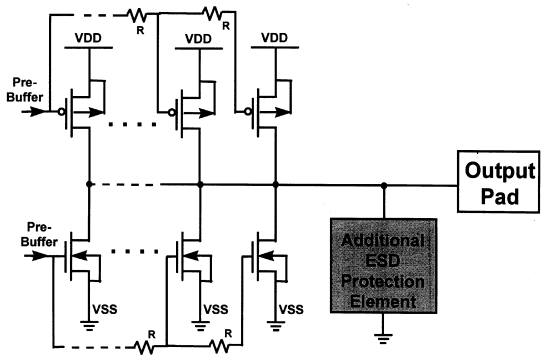


Fig. 2. The schematic circuit diagram to show the slew-rate-controlled output buffer with additional ESD protection elements.

of the output buffer. Because there is no LDD peak structure in the drain/source regions of the field-oxide device, the ESD failure threshold of a field-oxide device is generally higher than that of a thin-oxide *N*MOS with the same device dimension. But the snapback-breakdown voltage of the field-oxide device is higher than that of a short-channel thin-oxide output *N*MOS, the output *N*MOS could be first damaged before the field-oxide device is turned on in the ESD stress conditions.

To effectively protect the output buffer by using the field-oxide device, a series resistor has to be inserted between the output buffer and the field-oxide device. A schematic circuit of such design is shown in Fig. 3. If the series resistor R is too small, the ESD current could be still first discharged through the output *N*MOS rather than the field-oxide device. In[31], a field-oxide device is placed in parallel with the output *N*MOS, as well as the drain of output *N*MOS is modified with a series *N*-well resistor as that of[27]. With the suitable large resistor R, the field-oxide device can be turned on to bypass ESD current before the output transistor is damaged. But the series resistor will much degrade the circuit performance on the driving/sinking capability and the output timing, especially in the slew-rate-controlled output buffer.

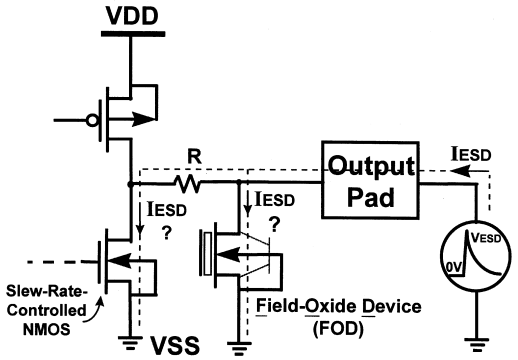


Fig. 3. Output ESD protection with the additional field-oxide device and a series resistor R.

If the turn-on voltage of the field-oxide device can be lowered below the snapback-breakdown voltage of the short-channel output transistor, the series resistor between the output transistor and the output pad can be removed. Therefore, the field-oxide device can perform excellent ESD protection for the output buffer without increasing much layout area to the pad, as well as the output driving/sinking capability is not degraded. In this paper, a well-coupled technique is proposed to reduce the turn-on voltage of the field-oxide device. With a lower turn-on voltage, this well-coupled field-oxide device can offer excellent ESD protection for the slew-rate-controlled output buffer alone without using the series resistor between the output transistor and the output pad.

2. DEVICE CHARACTERISTICS OF THE FIELD-OXIDE DEVICE

The device structure of an *n*-type field-oxide device in a *P*-well is shown in Fig. 4(a). The initial breakdown voltage (current) of the field-oxide device with a 0 V bulk (*P*-well) voltage is 13.0 V (3.9 mA), and the minimum holding voltage (current) of its snapback region is 7.8 V (6.5 mA). With such a 13 V breakdown voltage, the field-oxide device needs the help of a series resistor R to protect the output *N*MOS as that shown in Fig. 3.

If some voltage bias is added to the *P*-well of the *n*-type field-oxide device, the breakdown behavior of the field-oxide device becomes quite different. Figure 4(b) shows the setup to measure the breakdown characteristics of the *n*-type field-oxide device with different *P*-well biases. The bulk (*P*-well) of field-oxide device is biased with different positive voltages and the measured results are shown in Fig. 4(c). The increase of voltage step on the *P*-well bias is 0.1 V in Fig. 4(c). As the *P*-well bias is increased above 0.6 V which is near to the cut-in voltage of the base-emitter junction, the snapback-trigger voltage is significantly reduced. If the *P*-well bias is increased above 0.8 V, the lateral bipolar action in the field-oxide device is fully turned on when its drain bias is still in the low voltage region. As the drain bias increases higher, the turned-on field-oxide device finally enters into its snapback region. The relation between the *P*-well bias and the trigger voltage for the field-oxide device entering into the snapback region is shown in Fig. 5. The snapback-trigger voltage of the field-oxide device is significantly reduced as the *P*-well bias is above 0.6 V. As the bias voltage is up to 0.8 V, the snapback-trigger voltage is lowered to only about 8 V. With such a lower snapback-trigger voltage, the field-oxide device can provide effective ESD protection to the slew-rate-controlled output buffer without adding any series resistor to the drain of output transistors.

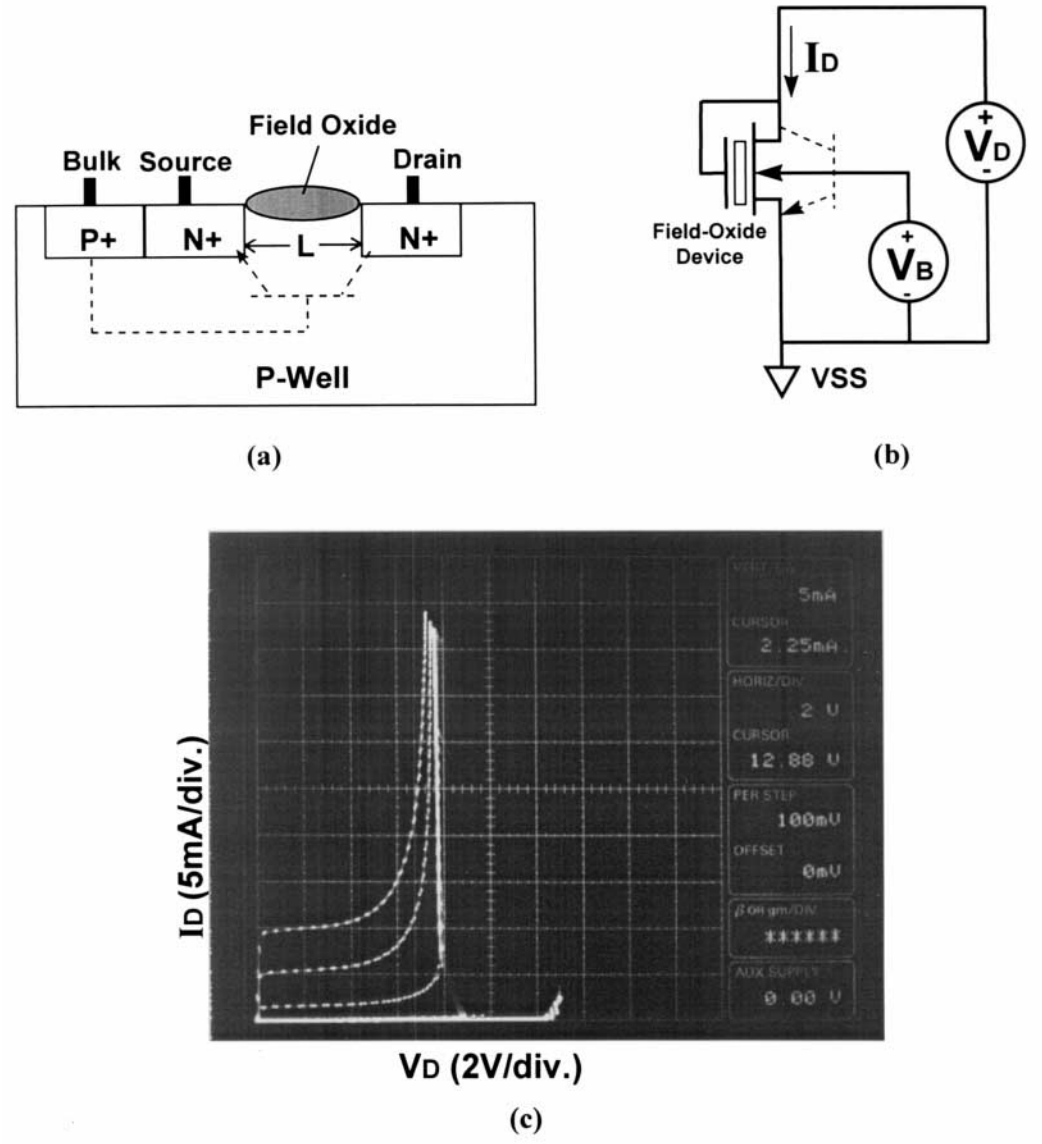


Fig. 4. (a) The device structure of an *n*-type field-oxide device in a *P*-well. (b) An experimental setup to measure the snapback-breakdown characteristics of an *n*-type field-oxide device with different *P*-well biases. (c) The measured *I–V* curves of the *n*-type field-oxide device with different positive *P*-well biases.

To investigate the ESD performance of the *n*-type field-oxide device with different *P*-well biases, the TLPG (Transmission-Line Pulse Generator)[32,33] is used to measure the It2 (secondary breakdown current) of the field-oxide device. The It2 of a device, which is measured by the TLPG pulse with a pulse width about 100 ns, is proportional to the HBM (human body model) ESD failure threshold of the device with a factor of about 1500[13]. A device with a higher It2 can sustain higher ESD voltage[13,34,35]. The TLPG-measured snapback behaviors of an *n*-type field-oxide device with different substrate biases are shown in Fig. 6, where an output *N*MOS with zero-voltage substrate bias is also measured as a reference. The dependence of It2 per channel width on the substrate bias is shown in Fig. 7. The output *N*MOS with a 0 V substrate bias has an It2 of 4.8 mA/μm in the 0.5 μm SRAM CMOS process. The It2 of the field-oxide device with a 0 V substrate bias is 9.0 mA/μm, but the It2 is increased to 18.2 mA/μm when the field-oxide device has a substrate bias of 0.8 V. In Fig. 7, the It2 (mA/μm) of the field-oxide device with a substrate bias above 0.6 V is about four times greater than that of the output *N*MOS in the 0.5 μm SRAM CMOS process. This implies that the field-oxide device with a substrate bias greater than 0.6 V can provide four times higher ESD failure threshold than the output *N*MOS per channel width.

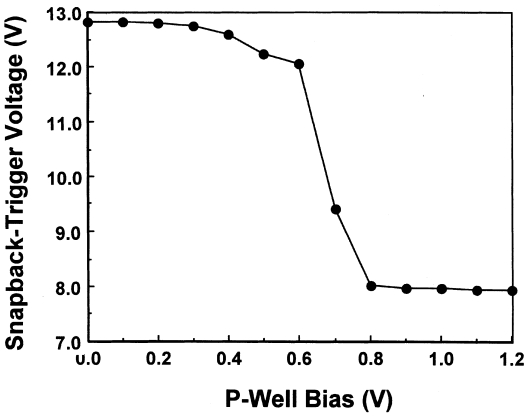


Fig. 5. The dependence of *P*-well biases on the snapback-trigger voltage of an *n*-type field-oxide device.

Through detailed investigation on the device characteristics, the snapback-trigger voltage of the field-oxide device can be lowered by increasing the substrate bias, as well as the It2 and the ESD failure threshold of the field-oxide device can be significantly increasing by the substrate bias. If the *P*-well potential of the *n*-type field-oxide device can be increased under the ESD stress conditions, the field-oxide device can be triggered on with a lower trigger voltage to protect the slew-rate-controlled output *N*MOS without adding the series resistor R. Moreover, the field-oxide device with a positive *P*-well bias can provide much higher ESD failure threshold, therefore the device size of the field-oxide device used to protect the output *N*MOS can be reasonably reduced to save the layout area. If some suitable ESD transient voltage can be coupled to the *P*-well of the field-oxide device, the field-oxide device can be fully turned on to bypass ESD current before the output transistors are damaged by ESD pulse. This is the basic concept to design the efficient ESD protection for output buffers with the proposed well-coupled technique[36].

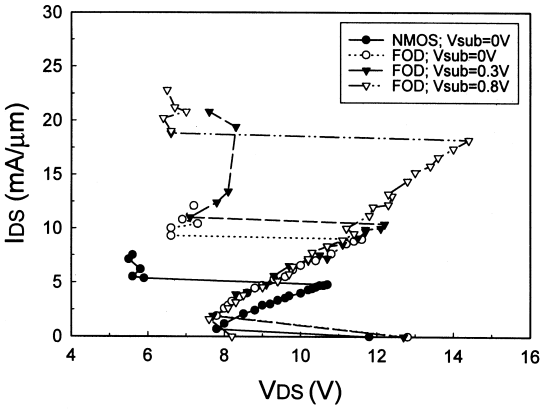


Fig. 6. The TLPG-measured snapback behaviors of a field-oxide device with different substrate biases and an *N*MOS with 0 V substrate bias.

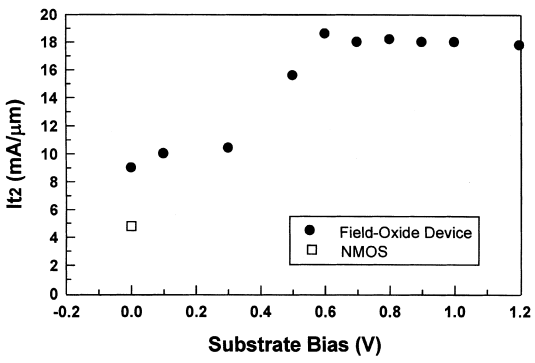


Fig. 7. The dependence of It2 (per unit channel width) on the substrate biases of a field-oxide device.

3. ESD PROTECTION FOR SLEW-RATE-CONTROLLED OUTPUT BUFFER

The slew-rate-controlled output buffer of a 256 K high-speed SRAM product includes a pull-up *N*MOS device, MN1, and a pull-down *N*MOS device, MN2. A resistor R1 of 30 Ω connected between the drain of MN1 and VDD is used to limit the short-circuit transient current when the MN1 and MN2 are both turned on during logic transition. An *N*MOS rather than a *P*MOS device is used as the pull-up transistor to save layout area of the output buffer, because the output driving current of an *N*MOS device can be 2–3 times higher than that of a *P*MOS device under the same device dimension. Another reason is due to the consideration of VDD-to-VSS latchup issue. If a *P*MOS

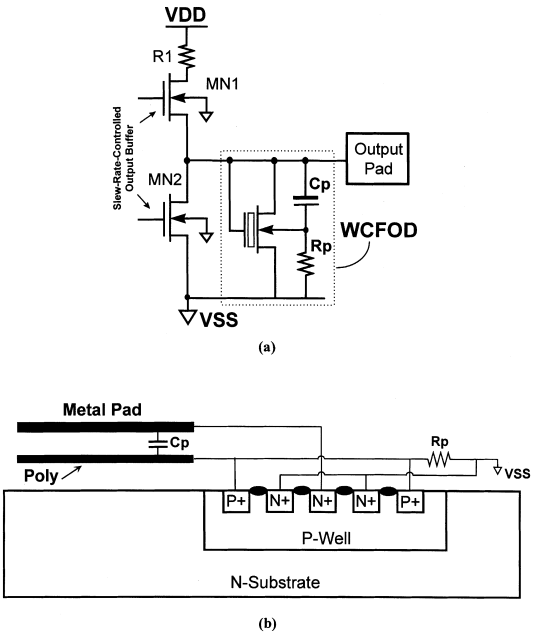


Fig. 8. (a) Output ESD protection with the proposed well-coupled field-oxide device (WCFOD); (b) the schematic cross-sectional view of the WCFOD structure.

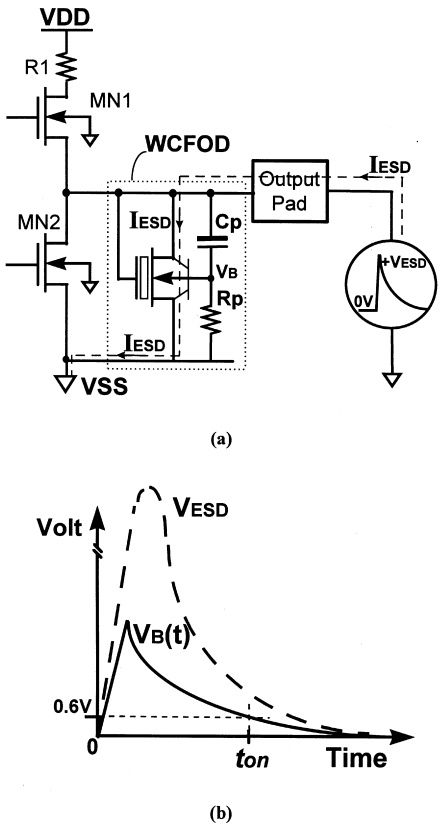


Fig. 9. (a) The operating principles of the WCFOD in the PS-mode ESD stress condition; (b) the schematic voltage waveforms on the WCFOD during the PS-mode ESD events.

device is used as the pull-up output transistor, the double guard rings to surround both output *P*MOS and *N*MOS devices as well as a wider spacing to separate these two different output transistors have to be added into the layout. Thus, the layout area will be much increased. For IC products, especially in SRAM ICs, the chip size is expected to be as small as possible. With both considerations on output driving capability and chip size, the device dimensions (W/L) of MN1 and MN2 in this SRAM output buffer are designed as 281/1.0 and 256/1.0 (μm/μm), respectively.

There are four different modes of ESD events on a pin of IC[37]. The PS-mode ESD stress, a positive ESD voltage on the output pad with relatively grounded VSS but VDD floating, has been found to be the worst case of ESD stress on the SRAM output buffer due to the snapback breakdown of output *N*MOS. The PS-mode ESD failure voltage of such a slew-rate-controlled output buffer is only around 1 kV in HBM (human body model) ESD testing, but its NS-mode ESD failure voltage can pass above 8 kV. The NS-mode ESD stress is tested by applying a negative ESD voltage to the output pad with relatively grounded VSS but VDD floating. The asymmetrical connection on the poly gates of the slew-rate-controlled output transistors leads to a much lower ESD failure voltage. The ESD failure threshold of a output pad is defined as the lowest ESD failure voltage of the four modes of ESD stresses, so the most important work of ESD protection for such a slew-rate-controlled output buffer is to improve the ESD failure voltage of output transistor under the PS-mode ESD stress.

3.1. *ESD protection with well-coupled field-oxide device*

The proposed output ESD protection with the *w*ell-*c*oupled *f*ield-*o*xide *d*evice (WCFOD) for slew-rate-controlled output buffer is shown in Fig. 8(a), and the corresponding schematic cross-sectional view of this WCFOD is shown in Fig. 8(b). In Fig. 8(b), the field-oxide device is formed by the N+ diffusions which are close to each other in a separated *P*-well. This separated *P*-well is connected to VSS through a resistor Rp. A capacitor Cp is connected from the output pad to the separated *P*-well to perform the well-coupled function under the PS-mode ESD stress.

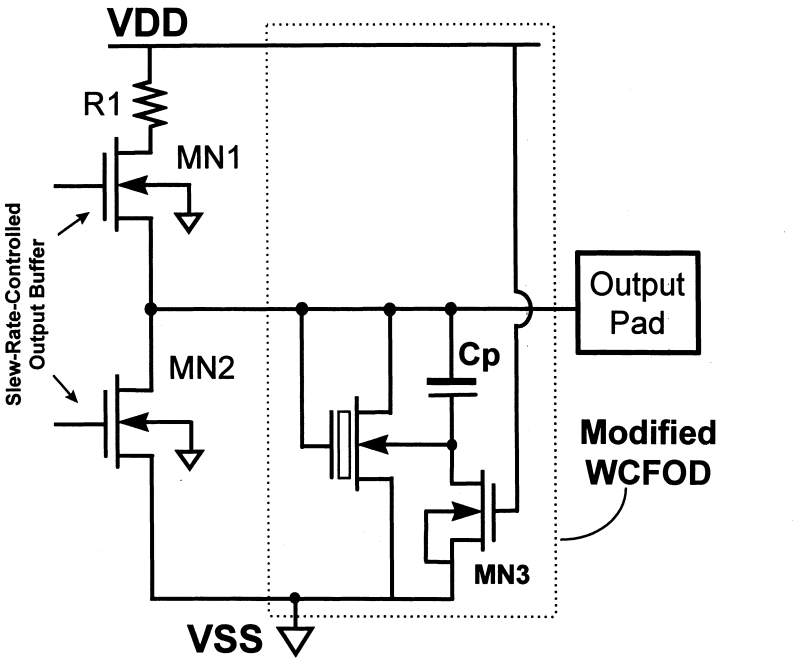
The operating principles of the WCFOD in the ESD stress condition is illustrated in Fig. 9. While the PS-mode ESD voltage occurs on the output pad as shown in Fig. 9(a), some positive ESD transient voltage will be coupled to the separated *P*-well through the capacitor Cp. The *P*-well is the base of the lateral bipolar transistor in the field-oxide device, which is marked as the node VB in Fig. 9(a). This coupled positive ESD transient voltage in the separated *P*-well is sustained longer in time by the resistor Rp. Due to the positive voltage in the separated *P*-well, the bulk-to-source junction of the field-oxide device is forward biased. This leads to the lateral bipolar action in the field-oxide device to happen earlier with a turn-on voltage much lower than its breakdown voltage. The schematic voltage waveforms on the node VB in the WCFOD during the PS-mode ESD events are illustrated in Fig. 9(b). Thus, the WCFOD can be fully turned on to bypass ESD current before the output transistor is damaged by the PS-mode ESD voltage. So, the slew-rate-controlled output transistors can be effectively protected by this proposed WCFOD without using the series resistor between the drains and the output pad.

This WCFOD is quite different to the field-oxide device in[16–18]. In[16–18], the field-oxide device is used only as a coupling device, not as the ESD current discharging device. The ESD current is still discharged through the output *N*MOS transistor in[16–18]. The ESD failure voltage per unit layout area of the field-oxide device can be about 3–4 times higher than that of the thin-oxide short-channel *N*MOS device with LDD structure. So, this WCFOD can perform high ESD protection within a smaller layout area for the slew-rate-controlled output buffer to save the chip size.

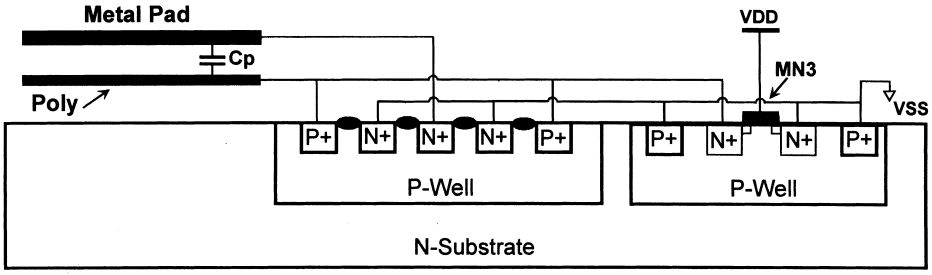
The coupling capacitor Cp in WCFOD can be realized by inserting the poly layer right under the wire-bonding metal pad, as shown in Fig. 8(b), without increasing layout area to the output pad. Such layout skill to realize the coupling capacitor had been successfully verified in an input ESD protection circuit[37,38]. The sustaining resistor Rp can be realized by the poly line around the output pad without increasing the total layout area of the chip. The Cp and Rp are designed to keep the field-oxide device off in the normal operating conditions, but to turn on the field-oxide device in the PS-mode ESD stress condition. Because the voltage level and the rise time between the normal output signal and the ESD pulse are quite different, the suitable Cp and Rp can be easily selected. The practical design for the Cp and Rp in the WCFOD can be calculated by using the equations of capacitor couple technique as derived in[37]. For a field-oxide device with a dimension (width/length) of 173/0.9 (μm/μm) in the SRAM process, the coupling capacitor Cp is chosen as 0.86 pF, and the sustaining resistor Rp is chosen as 24 kΩ.

3.2. *Modified well-coupled field-oxide device for advanced processes*

A modified structure for the WCFOD is shown in Fig. 10(a) with the corresponding cross-sectional view shown in Fig. 10(b). In this modified WCFOD, the Rp is realized by a long-channel thin-



(a)



(b)

Fig. 10. (a) The modified WCFOD for output ESD protection without using the ploy resistor; (b) the corresponding cross-sectional view of the modified WCFOD.

oxide *N*MOS device MN3 with its gate connected to VDD. The MN3 device is made in another *P*-well, which is directly biased at VSS. This modified WCFOD is especially suitable for output ESD protection in the advanced deep-submicron CMOS technology with polycide or salicide processes, because the sheet resistance of poly layer in the polycide/salicide process, is very small. The realization of a 24 kΩ resistor by the poly line becomes inefficient because it occupies too much layout area. But the voltage sustaining effect in the *P*-well of the field-oxide device can be easily realized by the MN3 with only a very small device dimension to save layout area.

In normal operating condition of the slew-rate-controlled output buffer, the separated *P*-well of the field-oxide device is biased to VSS through the turned-on MN3 device. Thus, the field-oxide device in the normal operating condition is kept off. In the PS-mode ESD stress condition with grounded VSS pin, MN3 device is initially off while the ESD pulse occurs on the output pad. Thus, the positive ESD transient voltage coupled to the *P*-well through the capacitor Cp is held in the *P*-well by the MN3 in the off state, so as to turn on the field-oxide device to bypass ESD current. Because the MN3 device is not directly stressed by the ESD voltage, MN3 can be designed with a much smaller device dimension to save layout area. A practical design of the device dimension (W/L) of MN3 is only 3/10. Because the gate of MN3 is connected to VDD, the overstress voltage in the VDD-to-VSS ESD stress condition

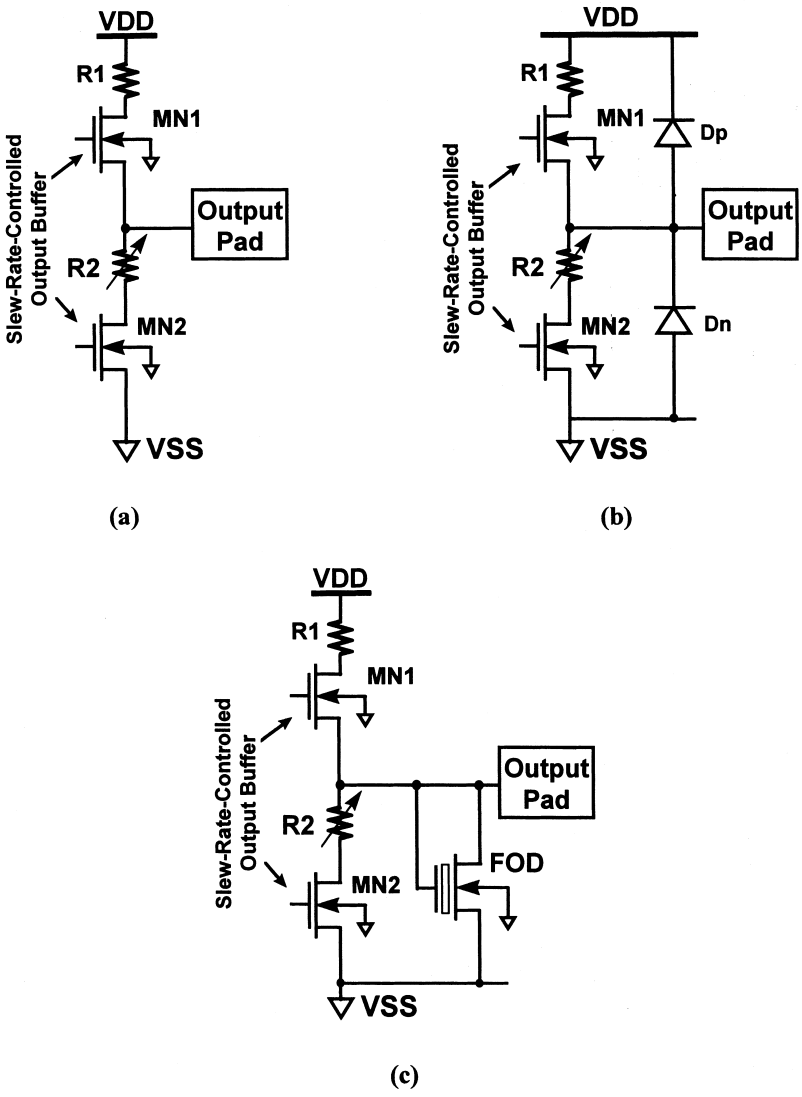


Fig. 11. Three previous designs of output ESD protection for comparison, in (a) using the series resistor, in (b) using the double-diode structure with series resistor, and in (c) using the field-oxide device with series resistor.

may cause the gate-oxide rupture on the MN3 device. An efficient VDD-to-VSS ESD clamp circuit has to be added between the VDD and VSS power lines in the whole-chip ESD protection design[39,40].

3.3. *ESD protection with previous designs*

Three previous designs of output ESD protection are also made in the same chip for comparison. One previous design is to directly add a series resistor into the drain of MN2 device to limit the large ESD transient current through the snapback-breakdown MN2 device. The equivalent circuit of such design with the series resistor R2 is shown in Fig. 11(a). The series resistor R2 is realized by the poly layer with sheet resistance of 60 Ω in this SRAM process. The poly resistor is added between every finger of MN2's drain and the output pad.

In[6], it was reported that the PS-mode ESD protection for output pad can be significantly improved by adding a *P*MOS device from the output pad to VDD. This *P*MOS device can dissipate some ESD energy to the VDD power line through the forward conducting drain-to-bulk junction diode in the *P*MOS device, so as to improve ESD protection for the pull-down output *N*MOS device under the PS-mode ESD stress. But, in this SRAM IC with consideration of layout area and latchup issue, the slew-rate-controlled output buffer has been designed without using the *P*MOS device as the pull-up transistor. Another method to provide a diode from the output pad to VDD without causing latchup issue is to use the double-diode protection structure[26]. The second previous design of output ESD protection by using the double-diode structure is shown in Fig. 11(b). Because the breakdown voltage of Dn is higher than the snapback-breakdown voltage of the short-channel output transistor MN2, the series resistor R2 was added into the drain region of MN2 device as that shown in Fig. 11(b). With the series resistor R2, the diode Dn can be broken down to bypass ESD current before the MN2 device is damaged by the PS-mode ESD voltage.

The third previous design to improve PS-mode ESD protection for the slew-rate-controlled output buffer is to use the field-oxide device[31]. The field-oxide device is placed in parallel with the MN2 device from the output pad to VSS. The equivalent circuit is shown in Fig. 11(c). As reported in[31], the series resistor R2 still has to be added into the drain region of MN2 to protect MN2, because the breakdown voltage of the field-oxide device is higher than that of the MN2 device. The dimension (width/length) of the field-oxide device in Fig. 11(c) in the test chip is kept the same as that in the WCFOD for comparison.

4. EXPERIMENTAL RESULTS AND DISCUSSIONS

An SRAM product is used to verify the ESD protection efficiency on the different protection designs. The five different designs (WCFOD, modified WCFOD, and three previous designs) have been implemented in five 256 K high-speed SRAM chips in a 5 V 0.5 μm *N*-substrate/twin-well CMOS process with LDD structure to investigate the efficiency of ESD protection. All the conditions of these five SRAM chips are set the same excluding the designs of output ESD protection, and they are fabricated in the same wafer. The spacing of drain contact to poly gate edge in the output *N*MOS transistors of the five SRAM chips is kept the same of 5 μm. The internal cores of these five chips are the same but only with different output ESD protection designs. There are eight I/O pads in each 256 K SRAM chip, and the series resistor R2 with different resistance from the drain fingers of the MN2 to the output pad is split in these eight pads. The series drain resistor is split as 0, 80, 150, and 300 Ω in each test chip to investigate its protection efficiency.

4.1. *ESD testing results*

The five 256 K high-speed SRAM chips with five different output ESD protection designs are tested by the *Zapmaster* ESD simulator[41] in the human body model (HBM) to investigate the efficiency of ESD protection. The ESD failure criterion is defined as that the leakage current of the I/O pad with output buffer and ESD protection circuit in its high-impedance state is above 1 μA under VDD (VSS) bias of 6 V (0 V). The high-impedance state of each I/O pin can be controlled by a chip-selected pin of the SRAM IC. The PS-mode ESD testing results of the five designs are summarized in Fig. 12 with different drain series resistance.

In Fig. 12, the PS-mode ESD failure voltage of the slew-rate-controlled output buffer in the SRAM ICs with the three previous ESD protection designs

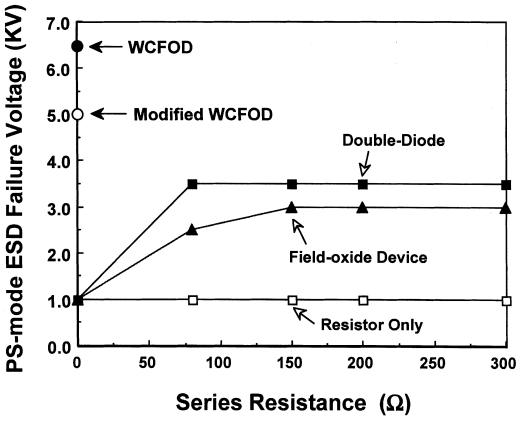


Fig. 12. The ESD failure voltage of the five different output ESD protection designs in the PS-mode HBM ESD testing with different drain series resistance.

is not improved as the series drain resistor R2 is too small. With the output ESD protection design of Fig. 11(a), the ESD failure voltage is not improved even if the series resistor R2 in each drain finger of output transistor is up to 300 Ω. Because there is no other ESD discharging path connected to the output pad except the output transistor, the ESD current is still discharged through the output *N*MOS transistor in Fig. 11(a). In the HBM ESD standard of MIL-STD-833C, the HBM discharging resistor from the HBM capacitor of 100 pF to the DUT (device-under-test) is as large as 1.5 kΩ. The series resistor of 300 Ω in each drain finger of the output transistor is much smaller than the HBM discharging resistor, so the series drain resistor of only 300 Ω has no improvement in the output ESD protection.

In the previous ESD protection design of Fig. 11(b), there are additional double diodes used to protect the output transistor with a series drain resistor R2. The breakdown voltage of the diode Dn in the SRAM process is about 12.2 V but the snapback-breakdown voltage of the short-channel output *N*MOS transistor is only 11.9 V, so the output transistor is first stressed and broken down by the ESD voltage if the series drain resistor R2 is too small. As the resistance of R2 is increased, the diodes Dn and Dp will share more part of ESD current from the output transistor. So, the ESD protection is improved as R2 is increased. From the experimental results, while the resistance of R2 is more than 80 Ω, the improvement of output ESD protection is dominated by the double-diode structure and its ESD failure voltage is kept at about 3.5 kV.

With the previous ESD protection design in Fig. 11(c), the breakdown voltage of the field-oxide device is about 13 V. So, it still needs to add the series drain resistor R2 to perform effective ESD protection for the output transistor. As the resistance of R2 is increased, the ESD failure threshold of the SRAM IC is also increased. As the resistance of R2 is higher than 150 Ω, the ESD protection is dominated by the field-oxide device and its ESD failure voltage is kept at about 3 kV. The larger device dimension of the field-oxide device can provide higher ESD failure voltage, but this also increases more layout area to the output pad. These three previous designs with a series resistor into the drain of output transistor have some improvement on ESD reliability but they also cause much degradation on circuit performance such as the current driving/sinking capability, the output signal timing, and the VOL level.

As the slew-rate-controlled output buffer is protected by the WCFOD with the same device dimensions of output transistors and the field-oxide device, the PS-mode ESD failure voltage is improved as high as 6.5 kV in the SRAM test chip. The ESD failure voltage of the output buffer protected by the modified WCFOD is also improved up to 5 kV under the same device dimensions. The slew-rate-controlled output buffers protected by the WCFOD or the modified WCFOD are also tested in the machine-model (MM) ESD events, and their MM ESD failure threshold is improved as high as 750 V, whereas the MM ESD failure voltage of the original slew-rate-controlled output buffer is only 100 V. The MM ESD failure voltage of the slew-rate-controlled output buffers protected by the diodes or the field-oxide device with drain series resistor is around 350 V. This practically verifies the excellent performance of the WCFOD and the modified WCFOD for ESD protection in the slew-rate-controlled output buffers. Because the ESD transient voltage is coupled to the *P*-well of field-oxide device to trigger on the lateral bipolar action, the WCFOD or the modified WCFOD can be turned on with a much lower trigger voltage to early bypass ESD current from the output pad to VSS. Therefore, the output transistor can be effectively protected by the WCFOD or the modified WCFOD without adding the extra series resistor R2 into the drain of the output transistor. Without adding the series resistor into the drain of output transistor, the output driving/sinking capability of the slew-rate-controlled output buffers is not degraded by the WCFOD or the modified WCFOD. So, this proposed output ESD protection with the WCFOD and the modified WCFOD is very suitable for CMOS ICs in advanced submicron or deep-submicron CMOS technologies to effectively improve ESD reliability of the slew-rate-controlled output buffers without causing any degradation on circuit performance.

4.2. *Leakage current*

Another concern for the *P*-well of the field-oxide device connected to VSS through a poly resistor or a long-channel *N*MOS device is the off-state leakage current as the WCFOD is applied to protect an I/O pad. In an I/O pad, it may become a high-impedance state as the output transistors are kept off by the control of internal circuits. The leakage current on the I/O pads of the five SRAM test chips with different output ESD protection designs has been investigated. A chip-selected pin in the five SRAM test chips, which can keep all the I/O pins in the high-impedance state, is used to turn off the output transistor. A voltage sweeping from 0V to 5 V generated by HP4145 is applied to the I/O pin under the high-impedance condition, and then the input current is observed as the leakage current of the pin.

The five SRAM test chips with different output ESD protection designs and different series resistors are measured. The I/O pin with WCFOD (or modified WCFOD) is found to have the maximum leakage current of 1.8 pA (or 1.9 pA), whereas the maximum leakage current in the original design is

1.7 pA. The maximum leakage current of the I/O pad with the three previous output ESD protection designs is around 1.7–1.8 pA under the different drain series resistance. The maximum leakage current of I/O pin with the WCFOD or the modified WCFOD is a little (about 0.1–0.2 pA) higher than that of the original design due to the indirect bias on the *P*-well of the WCFOD device.

4.3. *Efficiency of the well-coupled design*

To verify the efficiency of well-coupled technique for output ESD protection with the proposed WCFOD and modified WCFOD, a voltage pulse generated from HP8116A (pulse generator) with a pulse width of 400 nS and a rise time around 5 nS is applied to the I/O pin of the test chip under the bias of 5 V VDD and 0 V VSS. An oscilloscope is used to monitor the voltage waveform on the I/O pin. The chip-selected pin is also used to turn the output transistors off, so each I/O pad is in its high-impedance state. If the output ESD protection circuit is not triggered on by the applied voltage pulse, the voltage waveform on the I/O pin is not degraded. If enough transient voltage is coupled through the Cp to the *P*-well of the WCFOD or the modified WCFOD structures due to the rising edge of the applied voltage pulse on the I/O pin, the voltage waveform of the applied voltage pulse will be clamped by the turned-on WCFOD or modified WCFOD. The voltage peak of the applied voltage pulse can be adjusted to find the trigger voltage of the WCFOD and the modified WCFOD in output ESD protection circuit.

When the voltage peak of the applied voltage pulse is increased up to 7.1 V, as shown in Fig. 13(a), the WCFOD in the I/O pad is still not triggered on. Therefore, there is no degradation on the pulse-type voltage waveform in Fig. 13(a). If the voltage peak is increased more than 7.1 V, the WCFOD can be triggered on and the voltage waveform on the I/O pin is degraded. A typical degraded voltage waveform is shown in Fig. 13(b), where the voltage peak of the applied voltage pulse is 8.5 V with a rise time of about 5 nS. In Fig. 13(b), the 8.5 V pulse-type voltage waveform is degraded just after the rising edge of the applied voltage pulse. The rising edge of the applied voltage pulse triggers on the WCFOD, so the voltage waveform on the pad is clamped by the turned-on WCFOD after the rising edge.

Similarly, the output ESD protection with the modified WCFOD is also tested by the same method. The test results show that the applied voltage pulse on the I/O pin with a voltage peak of 7.5 V is still not triggered on the modified WCFOD structure. But, if the voltage peak is higher than 7.5 V, the modified WCFOD can be triggered on and causes degradation on the voltage waveform of the applied voltage pulse.

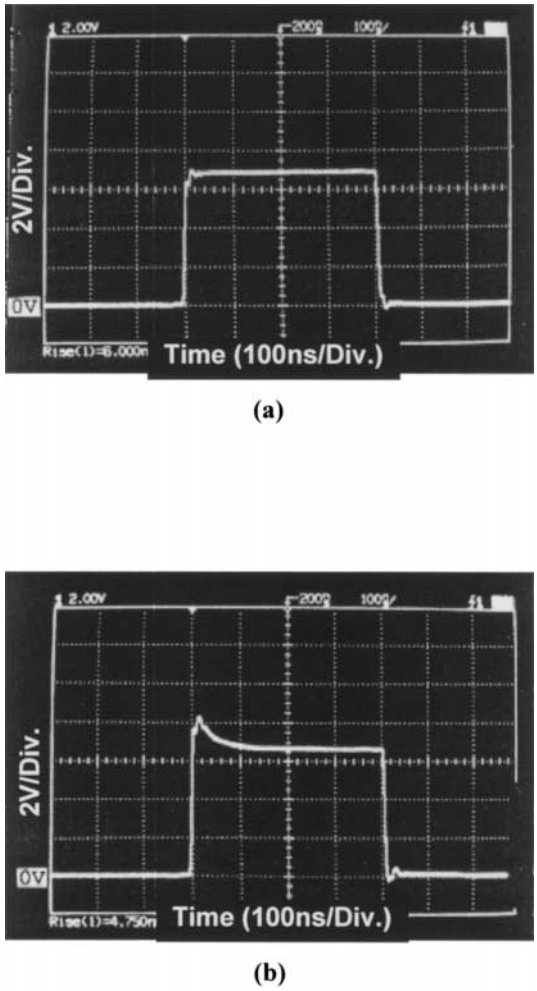


Fig. 13. The voltage waveform of the applied pulse-type voltage on the I/O pin, (a) without triggering on the WCFOD; (b) with triggered-on WCFOD, in the output ESD protection circuit.

With above experimental verification, the minimum voltage peak to trigger on the WCFOD (modified WCFOD) has been found to be about 7.1 V (7.5 V). So, these WCFOD and modified WCFOD structures in the output ESD protection circuit of the I/O pin are not triggered on by the normal 5 V input/output signals. The snapback-trigger voltage of the field-oxide device is 13 V, but the pulse-type trigger voltage of the proposed WCFOD (modified WCFOD) is lowered to only 7.1 V (7.5 V). Therefore, the external overstress voltage, such as the ESD pulse, can be bypassed by the early turned-on WCFOD or modified WCFOD structures to protect the slew-rate-controlled output buffers. This verifies the excellent efficiency of the proposed well-coupled technique. Moreover, because the trigger voltage of the WCFOD is lower than that of the modified WCFOD, ESD current on the I/O pad can be earlier and more effectively bypassed by the WCFOD. The trigger voltage (7.5 V) of the modified WCFOD slightly higher

than that (7.1 V) of the WCFOD is due to the capacitance effect in the MN3 device, because some of the ESD transient trigger current coupled from the Cp to the node VB is bypassed to ground through the parasitic capacitance in the MN3 device. This is the main reason why the WCFOD has a higher PS-mode ESD failure voltage than the modified WCFOD, even if these two structures have the same device dimension of field-oxide device for output ESD protection.

5. CONCLUSION

A new ESD protection technique for slew-rate-controlled output buffer with well-coupled field-oxide device (WCFOD) has been successfully verified and practically applied in a 0.5 μm 256 K high-speed SRAM product. A modified WCFOD for the advanced CMOS technologies with polycide or salicide processes is also proposed. The output ESD protection with the WCFOD or the modified WCFOD has the benefits of lower trigger voltage, higher ESD protection capability, but without adding the series resistor into the drain of output *N*MOS transistors. The ESD reliability of slew-rate-controlled output buffers have been effectively improved without causing any degradation on circuit performance of the high-speed SRAM IC. The HBM (MM) ESD reliability of this SRAM product has been improved up to above 5 kV (750 V), whereas the original output buffer just can sustain the PS-mode ESD stress of 1 kV (100 V) only.

With obvious advantages of lower trigger voltage and higher ESD robustness, the proposed WCFOD and modified WCFOD structures are also suitable to protect the thinner gate oxide of input stages in the deep-submicron CMOS technologies.

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REFERENCES

1. Duvvury, C. and Amerasekera, A., *IEEE Proc.*, 1993, **81,** 690.
2. Voldman, S. and Gross, V., *EOS/ESD Symp. Proc.*, 1993, **EOS-15,** 251.
3. Amerasekera, A. and Duvvury, C., *EOS/ESD Symp. Proc.*, 1994, **EOS-16,** 237.
4. Duvvury, C., McPhee, R., Baglee, D. and Rountree, R., *IRPS Proc.*, 1986, 199.
5. Duvvury, C., Rountree, R. N., Fong, Y. and McPhee, R. A., *IRPS Proc.*, 1987, 174.
6. Duvvury, C. and Rountree, R. N., *EOS/ESD Symp. Proc.*, 1988, **EOS-10,** 206.
7. Hu, C., Tam, S. C., Hsu, F.-C., Ko, P. K., Chan, T. Y. and Terrill, K. W., *IEEE J. Solid-St. Circuits*, 1985, **20,** 295.
8. Sanchez, J. J., Hsueh, K. K. and DeMassa, T. A., *IEEE Trans. Electron Devices*, 1989, **36,** 1125.
9. Aur, S., Chatterjee, A. and Polgreen, T., *IEEE Trans. Electron Devices*, 1988, **35,** 2189.
10. Daniel, S. and Krieger, G., *EOS/ESD Symp. Proc.*, 1990, **EOS-12,** 206.
11. Wei, Y., Loh, Y., Wang, C. and Hu, C., *EOS/ESD Symp. Proc.*, 1992, **EOS-14,** 143.
12. Kurachi, I., Fukuda, Y., Miura, N. and Ichikawa, F., *IEEE Trans. Industry Applications*, 1994, **30,** 358.
13. Diaz, C., Kopley, T. and Marcoux, P., *IRPS Proc.*, 1995, 276.
14. Polgreen, T. L. and Chatterjee, A., *IEEE Trans. Electron Devices*, 1992, **39,** 379.
15. Beebe, S. G., *EOS/ESD Symp. Proc.*, 1996, **EOS-18,** 265.
16. Duvvury, C., Diaz, C. and Haddock, T., *IEDM Technical Digest*, 1992, 131.
17. Duvvury, C. and Rountree, R. N., United States Patent No. 4855620, 1989.
18. Duvvury, C. and Diaz, C., *IRPS Proc.*, 1992, 141.
19. Tomioka, I. *et al.*, *IEEE CICC Proc.*, 1990, 11.7.1.
20. Leung, K., *IEEE CICC Proc.*, 1998, 5.3.3.
21. Senthinathan, R. and Prince, J. L., *IEEE J. Solid-St. Circuits*, 1993, **28,** 1383.
22. Diaz-Olavarrieta, L., *IEEE Int. Symp. on Electromagnetic Compatibility Proc.*, 1991, 387.
23. Vaidyanath, A., Thoroddsen, B. and Prince, J. L., *IEEE Trans. Components, Packaging and Manufacturing Technology, Part B*, 1994, **17,** 480.
24. Vemuru, S. R., *IEEE Int. ASIC Conf. Proc.*, 1994, 7.
25. Gong, S. *et al.*, *IEEE Int. ASIC Conf. Proc.*, 1995, 21.
26. Smooha, Y., United States Patent No. 4990802, 1991.
27. Scott, D. B, Bosshart, P. W. and Gallia, J. D., United States Patent No. 5019888, 1991.
28. Roberts, G. N., United States Patent No. 5218222, 1993.
29. Liu, Y.-J. and Cagnina, S., United States Patent No. 4734752, 1988.
30. Chan, T. C. and Culver, D. S., United States Patent No. 5329143, 1994.
31. Lee, K. F., Lee, A., Marmet, M. L. and Ouyang, K. W., United States Patent No. 5270565, 1993.
32. Maloney, T. J. and Khurana, N., *EOS/ESD Symp. Proc.*, 1985, **EOS-7,** 49.
33. Ashton, R. A., *IEEE Int. Conf. on Microelectronic Test Structures Proc.*, 1995, 127.
34. Amerasekera, A., Roozendaal, L., Bruines, J. and Kuper, F., *IEEE Trans. Electron Devices*, 1991, **38,** 2161.
35. Jiang, C., Nowak, E. and Manley, M., *IRPS Proc.*, 1996, 233.
36. Wu, C.-N. and Ker, M.-D., *IEEE Trans. Electron Devices*, 1997, **44,** 503.
37. Ker, M.-D., Wu, C.-Y., Cheng, T. and Chang, H.-H., *IEEE Trans. VLSI Systems*, 1996, **4,** 307.
38. Ker, M.-D., Wu, C.-Y., Cheng, T., Wu, M. and Yu, T.-L., *IEEE Int. ASIC Conf. Proc.*, 1995, 135.
39. Ker, M.-D. and Liu, S.-C., *IEEE Int. Symp. on Circuits and Systems Proc.*, 1997, 1920.
40. Ker, M.-D., Wu, C.-Y., Chang, H.-H. and Wu, T.-S., *IEEE CICC Proc.*, 1997, 31.
41. *Zapmaster User Manual.* KeyTek, U.S.A., 1994.