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LATCHUP-FREE FULLY-PROTECTED ESD PROTECTION CIRCUIT FOR INPUT PAD OF SUBMICRON CMOS ICs

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Abstract—A latchup-free on-chip input ESD protection circuit with a concept of full protection against ESD damage is proposed. The four modes of ESD stresses on an input pad are one-by-one protected by four effective ESD discharging paths in this proposed ESD protection circuit to avoid unexpected ESD damage. This ESD protection circuit was included in a 0.8 μm cell library to successfully provide high ESD reliability for input pads of CMOS ASICs within a small layout area. © 1997 Elsevier Science Ltd.

1. INTRODUCTION

As a result of using the LDD structure to overcome the hot-carrier degradation in submicron CMOS devices and using the silicided diffusion to reduce the sheet resistance in the drain and source of CMOS devices, ESD (Electrostatic Discharge) protection has become one of the most important reliability issues of submicron CMOS technologies[1–4]. Usually, the gate of a CMOS input stage is connected directly to the input pad for signal delivery. So, a suitable input ESD protection circuit has to be placed around the input pad to clamp the voltage level of input signal, and to protect the gate oxide of the input stage against ESD damage.

Several conventional ESD protection circuits for CMOS input pad were made with the *n*-type field-oxide devices (or called as the thick-oxide device) which were placed only between the input pad and VSS[5–9]. Such conventional ESD protection circuits can offer ESD discharging path from the input pad to VSS, but have no direct ESD discharging path from the input pad to VDD. Without direct ESD discharging path from the input pad to VDD, some unexpected ESD damages were found to locate at the internal circuits beyond the ESD protection circuits[10–14].

Generally, there are four different ESD-stress conditions on an input pin[15], which are illustrated in Fig. 1.

(1) PS mode, ESD stress on a pin with positive voltage polarity to the VSS(GND) pin when the VDD pin and other input/output pins are floating;
(2) NS mode, ESD stress on a pin with negative voltage polarity to the VSS(GND) pin when the VDD pin and other input/output pins are floating;
(3) PD mode, ESD stress on a pin with positive voltage polarity to the VDD pin when the VSS(GND) pin and other input/output pins are floating;
(4) ND mode, ESD stress on a pin with negative voltage polarity to the VDD pin when the VSS(GND) pin and other input/output pins are floating.

These ESD voltages could damage both NMOS and PMOS devices in the input stage or the internal circuits of CMOS ICs.

In Refs[5–9], the ESD-protection devices are only arranged between the input pad and VSS. There is no ESD-protection element arranged between the pad and VDD. Under the ND-mode or PD-mode ESD stresses, the ESD current/voltage is first diverted from the input pin to the floating VSS power line through the ESD-protection devices between the input pad and VSS. Such a non-direct ESD discharging path was reported to cause some unexpected ESD damages on the internal circuits beyond the ESD protection circuits[10–13]. The internal damages are especially easy to happen in the ND-mode ESD stress. Figure 2 shows a schematic diagram to explain the unexpected discharging paths in the internal part of a CMOS IC under the ND-mode ESD-stress condition, in which there is only an input-to-VSS ESD protection circuit at the input pad. The ND-mode ESD voltage between the input pad and the VDD pad is transferred to cause ESD voltage across the VSS and VDD power lines. If this negative voltage across the VSS and VDD power lines cannot be effectively and quickly bypassed through the VDD-to-VSS ESD protection

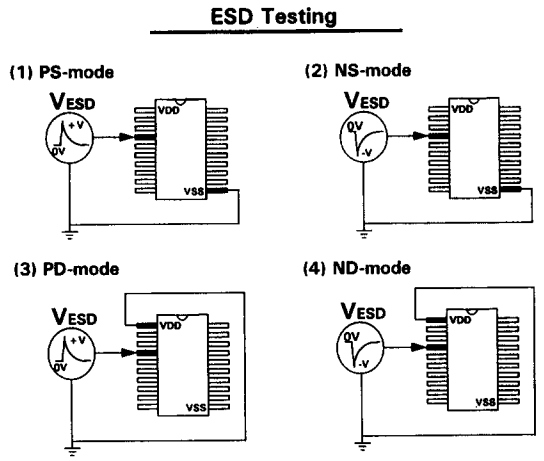

Fig. 1. Four modes of ESD stresses on a pin of CMOS IC.

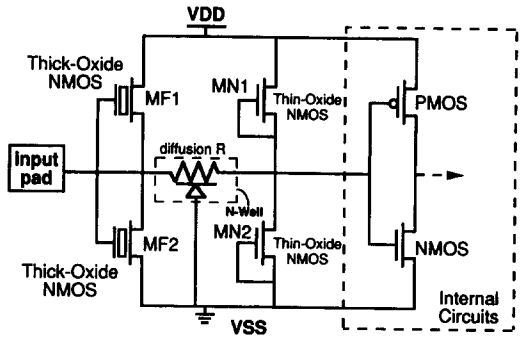

Fig. 3. The proposed latchup-free fully-protected ESD protection circuit for input pad of CMOS ICs.

circuit, this ND-mode ESD voltage will cause unexpected ESD damages on the internal circuits. In Ref. [10], the unexpected ESD damages were found to locate along the VDD-to-VSS latchup paths in the internal circuits of a CMOS IC. This ND-mode ESD voltage across VSS and VDD power lines had also caused internal damages on the parasitic n-type field-oxide devices[10,11], which are parasitically formed by two separated N+ diffusions with a narrow field-oxide spacing. Of course, this ESD voltage between VDD and VSS power lines could cause ESD damage on the active devices of internal circuits[12,13]. In the advanced submicron or deep-submicron CMOS processes, the minimum spacing between PMOS and NMOS devices and the minimum spacing between two $N+$ diffusions are scaled down to improve the integrated density of CMOS ICs. Such scaled-down spacings in the parasitic field-oxide device or the p-n-p-n latchup path make the submicron CMOS ICs more sensitive to the internal ESD damages. Thus, an input ESD protection circuit for advanced submicron CMOS ICs should provide effective ESD discharging paths from the input pad to both the VSS and VDD power lines to avoid the ESD discharging current through the internal circuits. This is especially necessary for a submicron CMOS VLSI/ULSI with a larger die size and longer VDD/VSS power lines which often surround the whole chip.

In this article, an input ESD protection circuit with a concept of full protection is proposed and realized in a 0.8 μm CMOS technology. There are effective ESD-discharging paths arranged from the input pad to both VDD and VSS power lines to protect the CMOS input stage and also to avoid the unexpected internal damages. Because the elements used in this proposed ESD protection circuit are all n-type devices, there is no VDD-to-VSS latchup problem in this ESD protection circuit. Thus, the layout can be drawn more compactly to save silicon area of IC products.

2. LATCHUP-FREE FULLY-PROTECTED ESD PROTECTION CIRCUIT

2.1. *Circuit configuration and device structures*

The proposed input ESD protection circuit is shown in Fig. 3 with its corresponding cross-sectional

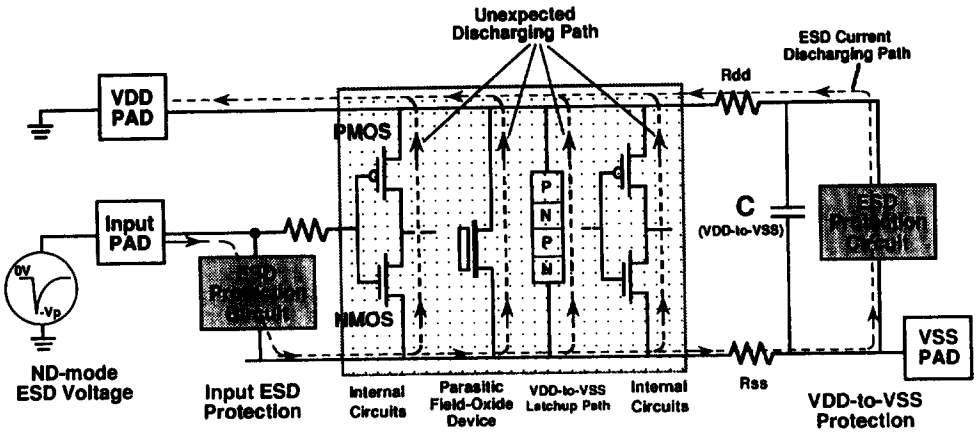

Fig. 2. Schematic diagram to explain the unexpected ESD discharging paths along the internal circuits under the ND-mode ESD-stress condition.

view given in Fig. 4, which is realized in a p-substrate n-well CMOS technology with LDD process. Two thick-oxide devices are used as the primary protection elements because they have no LDD peak near the channel. The LDD peak structure under the side wall of poly gate in the thin-oxide NMOS device is easily damaged by ESD current. Although dual thick-oxide devices were reported to form an input ESD protection circuit[16], the ESD robustness of thick-oxide device is still degraded in submicron CMOS process with shallow junction and LDD structure[1]. To improve the ESD robustness of the thick-oxide device, a "well" structure is inserted into its drain region to increase the lateral bipolar action of the thick-oxide device[17]. Because the ESD current is mainly discharged through the thick-oxide devices, the n-well structure is inserted into both the drain and source regions of the thick-oxide devices MF1 and MF2. The n-well structure is also inserted into the drain and source regions of the thin-oxide devices MN2 and MN1, respectively, because these regions are also accessed to the input pad.

To save the layout area of the proposed input ESD protection circuit, a compact device structure is shown in Fig. 4. The drains of MF1 and MF2 are merged together, and the drain of MN2 and the source of MN1 are also merged, to share the same $N+$ diffusion. The source of MF2 and MN2 are also merged with the $P+$ diffusion in the center of Fig. 4, which are all connected to VSS. Surrounding the MF1, MF2, MN1, and MN2 devices, there are two latchup guard rings (a $P+$ diffusion connected to VSS and an $N+$ diffusion connected to VDD) to prevent the trigger current through the p-substrate into the internal part of a CMOS IC to initiate latchup in the internal circuits. As seen in Fig. 4, all the devices are n-type devices. Therefore, the proposed input ESD protection circuit is itself free to the latchup issue. But, the voltage signal on the input pad caused by overshooting or undershooting may generate the substrate current to trigger latchup in the internal circuits. This substrate current will be absorbed by the guard rings which surround the whole ESD protection circuit. Through the detailed consideration on ESD protection and latchup prevention, a compact and efficient device structure for the proposed ESD protection circuit is demonstrated in Fig. 4.

Besides, in advanced deep-submicron CMOS technologies, the salicided/silicided diffusion has been used to reduce the sheet resistance of CMOS devices[4]. ESD robustness of the thick oxide device is also degraded by such salicided/silicided diffusion process[1,4]. To overcome such degradation, a modified device structure is adopted to break the silicided diffusion in its drain region. The cross-sectional view of this proposed input ESD protection circuit with modified device structure is shown in Fig. 5. The drain region of thick-oxide device is modified with an n-well structure to block the silicided diffusion without adding extra silicide-blocking mask into the process flow. By this modification, the thick-oxide device can be still very suitable as a primary protection element for the input ESD protection in the submicron or deep-submicron CMOS technologies with silicided diffusion.

In Fig. 3, the thin-oxide PMOS device of the input stage is protected by the MF1 (thick-oxide) device, resistor R ($N+$ diffusion surrounding by an n-well), and MN1 (thin-oxide NMOS) device, whereas the thin-oxide NMOS device of the input stage is protected by the MF2 (thick-oxide) device, resistor R, and MN2 (thin-oxide NMOS) device. MF1 and MF2 devices form as the primary ESD protection. Because the turn-on voltage of a thick-oxide device is much greater than 5 V, the metal gates of MF1 and MF2 are connected to the input pad to enhance their turn-on speed. The metal gate of MF1 and MF2 can be also replaced by a poly gate (poly line on the top of the field-oxide region). The gates of MF1 and MF2 can be even removed with nothing on the top of the field-oxide region to behave as a parasitic lateral n-p-n BJT transistor. The resistor R, MN1, and MN2 form as the secondary ESD protection. The poly

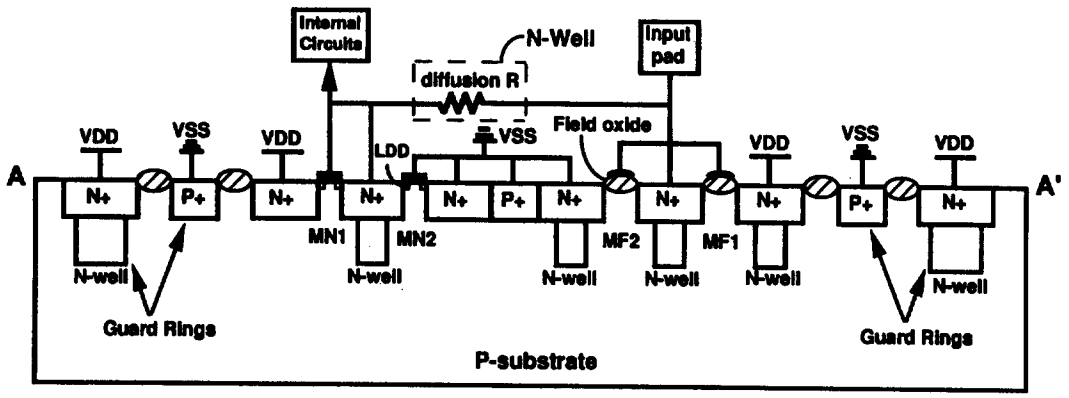

Fig. 4. A cross-sectional view to show device structures of the proposed ESD protection circuit of Fig. 3.

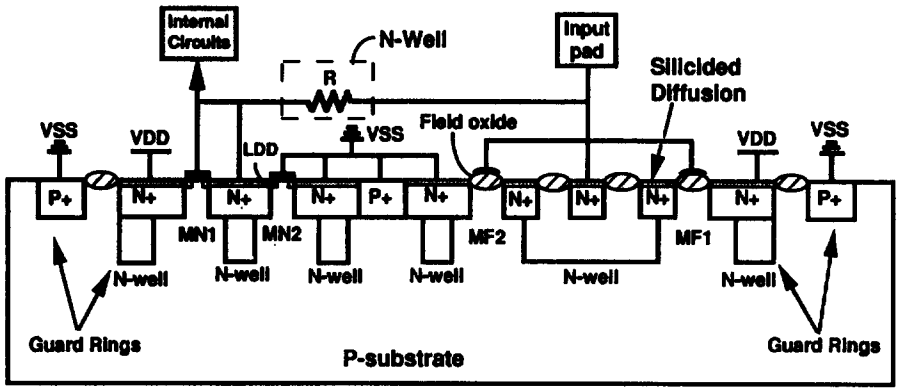

Fig. 5. A cross-sectional view of modified device structures for the proposed ESD protection circuit in advanced submicron CMOS technology with LDD and silicided diffusion.

gates of the thin-oxide MN1 and MN2 are connected to their sources, respectively. The resistor R of $N+$ diffusion is made about 200–300 Ω to limit ESD current through the MN1 and MN2 devices. This resistor R should be fully surrounded by an n-well to avoid the unexpected diode breakdown along the $N+$ diffusion of resistor R before MF1 or MF2 are turned on to bypass ESD current. A larger diffusion R can be cooperated with MN1 and MN2 of smaller device dimensions to perform ESD protection function before MF1 or MF2 are turned on, but this will lead to longer RC time delay between the input pad and the internal circuits. This diffusion resistor R can be replaced by a poly resistor, but the width of the poly line can not be too small. The resistor R formed by a poly line should be designed with a suitable large width to avoid the poly line being burned out before MF1 or MF2 are turned on[18].

The thin-oxide MN1 device with its gate connected to its source, but not to VSS, provides a voltage-clamping effect on the high voltage level of the input signal. As the input signal has an unexpected high-voltage level above VDD + V_{TN} (V_{TN} is the threshold voltage of MN1) because of overshooting, MN1 will be turned on to clamp the voltage level of the input signal. As the input signal has an unexpected low-voltage level below VSS–0.5 V because of undershooting, the parasitic diode formed by the $N+$ diffusion in ESD protection elements (connected to the pad) on the p-substrate (connected to VSS) will be inherently turned on to clamp the input voltage level. Thus, the proposed input ESD protection circuit not only performs on-chip ESD protection but also provides a voltage-clamping effect on the input signal to clamp overshooting/undershooting transient noise.

2.2. *Layout example*

The device structures of MF1, MF2, MN1, and MN2 can be merged together to save total layout area as shown in Figs 4 and 5. The deep n-well structure is inserted into the drain and source regions of ESD protection devices to increase ESD current flowing path and to improve their ESD protection capability. Because all of the elements used in this proposed ESD protection circuit are all n-type devices, there is essentially no VDD-to-VSS latchup problem in this ESD protection circuit. This makes the layout of ESD protection circuit around the bonding pad more compact and feasible to save layout area.

A compact layout example of this input ESD protection circuit is shown in Fig. 6, which is implemented in a 0.8 μm twin-well p-substrate CMOS technology. The dashed A- -A′ line in Fig. 6 is used to show the corresponding cross-sectional view in Fig. 4. The channel length of MF1 and MF2 devices for the primary ESD protection is 2 μm, but the channel length of MN1 and MN2 devices for the secondary ESD protection is 1 μm. The spacing from the drain and source contacts to the diffusion edge in MF1 and MF2 (also in MN1 and MN2) devices is an important layout parameter for ESD protection[2]. This spacing is selected as 5 μm and each contact size is of 2 × 2 μm^2. The whole ESD protection circuit is surrounded by a 5 μm $P+$ diffusion connected to VSS as a base guard ring, and also surrounded by a deep n-well region inside with $N+$ diffusion of 6 μm connected to VDD as a collector guard ring. The purpose of adding $P+$ and $N+$ guard rings is to prevent the unexpected substrate current flowing into internal circuits to cause VDD-to-VSS latchup in the internal circuits, because the input signal may be overshooting or undershooting on the input pad. All the elements of ESD protection circuit and latchup guard rings can be merged together, as shown in Fig. 6, to effectively save layout area for high-density application. Total layout area of this proposed input ESD protection circuit including latchup guard rings in Fig. 6 is only 100 × 152 μm^2.

2.3. *Operating principles*

In normal operating conditions of CMOS IC's with 5 V VDD and 0 V VSS, the MF1, MF2, MN1, and MN2 devices in the ESD protection circuit are all kept off, because the turn-on voltage of thick-oxide

MF1 and MF2 devices is much higher than 5 V as well as the gates of thin-oxide MN1 and MN2 devices are connected to their sources to keep them off. If the input signal is overshooting or undershooting, the voltage level on the input pad will be clamped between VDD + V_{TN} and VSS–0.5 V.

In the PS-mode ESD stress, the positive ESD voltage is diverted to the drain of short-channel thin-oxide MN2 device through the diffusion R. The MN2 device is first turned on by means of snapback breakdown to clamp the positive ESD voltage (about 11–13 V, dependent on the CMOS process) across the gate oxide of the input stage. The breakdown current of MN2 through the diffusion R causes a voltage about $V_{sb} + (I \times R)$ on the drain of MF2, where V_{sb} is the snapback voltage of MN2 device, I is the current through the snapback-breakdown MN2, and R is the resistance of the $N+$ diffusion resistor. When the voltage of $V_{sb} + (I \times R)$ is greater than the breakdown voltage of the thick-oxide MF2 device (about 14–16 V, dependent on the CMOS process), the lateral bipolar action of MF2 will be triggered on to bypass ESD current to VSS. Thus, the ESD current is discharged mainly by the thick-oxide MF2 device, but the voltage level across the gate oxide of the input stage is clamped by the short-channel thin-oxide MN2 device. The shorter channel of MN2 generally leads to a lower snapback voltage of MN2 to more effectively clamp the voltage level across the input gate oxide. MF2 can be turned on to bypass ESD current before the unexpected breakdown occurs on the $N+$ diffusion resistor, because the diffusion resistor R is fully surrounded by an n-well in the layout. The breakdown voltage from an n-well to the p-substrate is as high as 25–30 V, which is much greater than the breakdown voltage of MF2. The current I is proportional to the device dimension (channel width) of MN2 in the snapback-breakdown region. MF2 should be turned on before the current I is greater than the $It2$ (second breakdown current) of the MN2. A suitable resistance R and device dimension of MN2 can be designed to perform effective ESD protection without causing serious RC time delay between the input pad and the internal circuits.

As an NS-mode ESD voltage occurs on the input pad, the $N+$ diffusion in the drain of MF2 device (also in the diffusion resistor R or the drain of thin-oxide MN2 device) is forward conducting to bypass ESD current. ESD current is discharged mainly by the $N+$ diffusion/p-substrate junction diode in a forward-biased condition. The junction diode under its forward-biased condition can perform high ESD protection capability.

In the PD-mode ESD stress, the thin-oxide MN1 device is forward conducting to bypass ESD current because its gate is accessed to the input pad. The transient peak current of ESD through MN1 is limited by the $N+$ diffusion resistor R. MN1 under its forward-conducting condition with the resistor R of several hundreds ohms also performs high ESD robustness.

In the ND-mode ESD stress, the negative ESD voltage is diverted to the source of the short-channel thin-oxide MN1 device through the resistor R with relatively grounded VDD. MN1 is first turned on by means of snapback breakdown to clamp the negative ESD voltage (about −11 to −13 V, dependent on CMOS process) across the gate oxide of the input stage. The breakdown current of MN1 through the

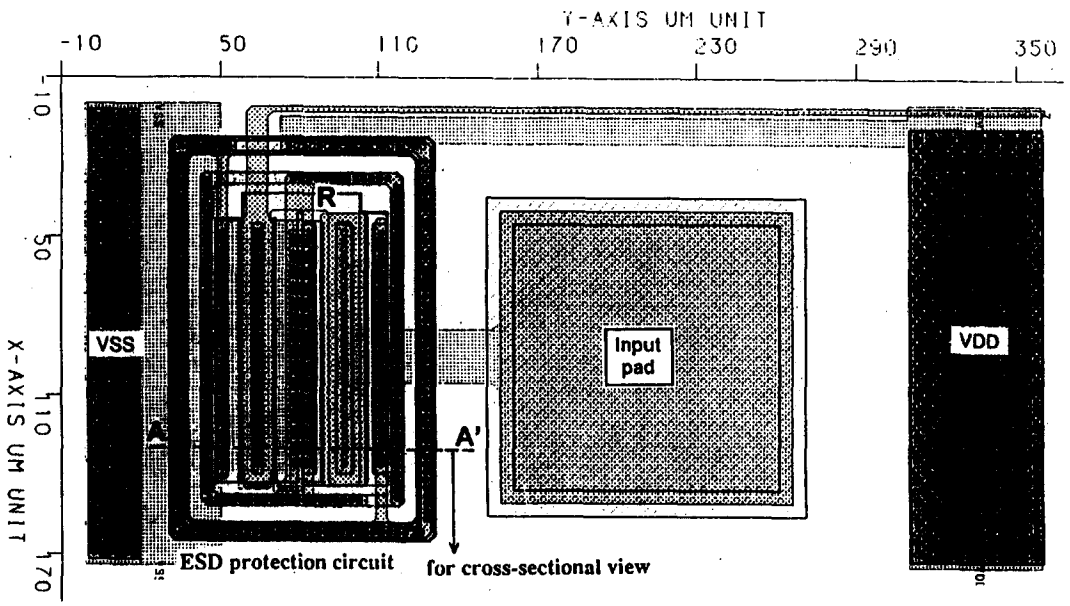

Fig. 6. A compact layout example to realize the input ESD protection circuit in a 0.8 μm CMOS technology.

resistor R causes a voltage about $-[V_{sb} + (I \times R)]$ on the drain of thick-oxide MF1 device, where V_{sb} is the snapback voltage of MN1, I is the current through the snapback-breakdown MN1, and R is the resistance of the $N+$ diffusion resistor. When the negative voltage of $-[V_{sb} + (I \times R)]$ is lower than the breakdown voltage of the thick-oxide MF1 device (about -14 to -16 V with relatively grounded VDD, dependent on CMOS process), the lateral bipolar action of MF1 will be turned on to bypass ESD current to the grounded VDD pad. Thus, the ESD current is discharged mainly by MF1, but the negative ESD voltage across the gate oxide of the input stage is clamped by the short-channel thin-oxide MN1 device. The shorter channel of MN1 generally leads to a lower snapback voltage of MN1. I is proportional to the device dimension of MN1 device. MF1 should be turned on before the current I reaches the second breakdown point of the MN1. So, suitable resistance R and device dimension of MN1 have to be designed to meet above operating requirement.

2.4. *Modification for application in the mixed-voltage system*

In the mixed-voltage system, there are multiple VDD power supplies. For example, an IC in the mixed-voltage system has a VDD of 5 V, but the other has its VDD of 3 V. If this proposed input ESD protection circuit is used in an input pad of 3 V IC but with an input signal coming from an output buffer of a 5 V IC, the 5 V input signal will cause a current flow from the 5 V VDD toward the 3 V VDD due to the forward conducting MN1 device. This limits the MN1 device to perform the clamping effect on the high-voltage level of the input signal.

The mixed-voltage interface causes some limitations to place ESD protection circuit between the input pad and VDD. But, if an input pad has no input-to-VDD ESD protection circuit, the internal circuits are more sensitive to the ND-mode ESD stress as shown in Fig. 2. Thus, the mixed-voltage chip-to-chip interface I/O circuitry with suitable ESD protection circuit must be designed to avoid ESD stress and to prevent undesirable current leakage paths between the different VDD power supplies. In [19] and [20], a five-stage diode string (comprising of $P+$ diffusion/N-well diodes) was reported as an input-to-VDD ESD protection element for the mixed-voltage interface environments. In [20], another self-biased-well ESD circuit for the mixed-voltage interface environment was also reported.

If the gate of MN1 device is connected to VSS, the proposed ESD protection circuit can be still suitable to protect the input pad of the mixed-voltage interface. The modified input ESD protection circuit for the mixed-voltage interface is shown in Fig. 7 with modification on the connection of the gate of MN1 device. This modified input ESD protection circuit can perform effective ESD protection for the mixed-voltage interface and avoid the unexpected ESD damage in the internal circuits of CMOS ICs.

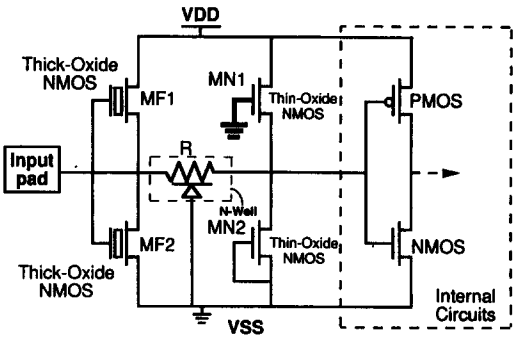

Fig. 7. A modified ESD protection circuit for an input pad in the mixed-voltage interface.

3. EXPERIMENTAL RESULTS

A microphotograph of the fabricated ESD protection circuit corresponding to Figs 3 and 6 in a 0.8 μm twin-well CMOS process with LDD structure is shown in Fig. 8. In Fig. 8, the device dimensions (channel width/ channel length) of MF1 and MF2 are 100/2 (μm/μm), and those of MN1 and MN2 are both 100/1. The I–V characteristics of the fabricated ESD protection circuit are measured and shown in Fig. 9(a) and (b). The curve of Fig. 9(a) is measured by applying an input voltage to the input pad with a grounded VSS but the VDD is floating. The applied positive voltage on the input pad is limited to around 13.6 V, whereas the negative voltage on the input pad

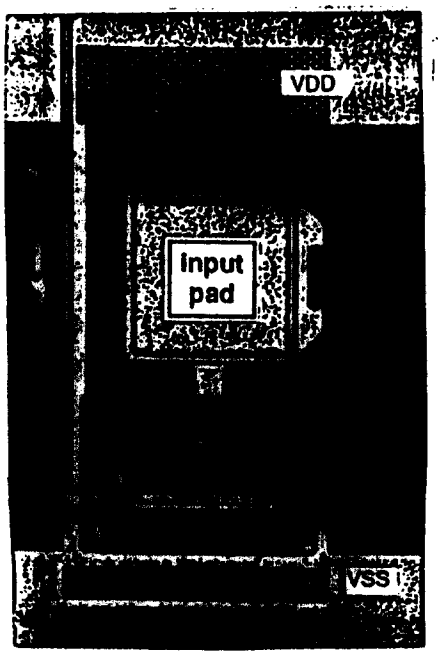

Fig. 8. A microphotograph of the fabricated ESD protection circuit corresponding to the layout in Fig. 6.

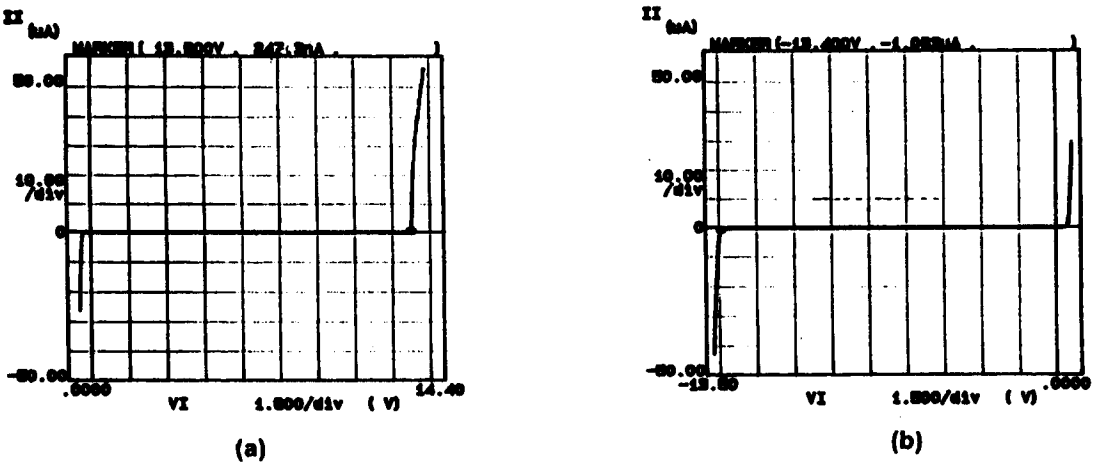

Fig. 9 Characteristics of the voltage-clamping effect of the proposed ESD protection circuit in the ESD-stress condition, (a) the I–V curve measured with grounded VSS but floating VDD; (b) the I–V curve measured with grounded VDD but floating VSS.

is limited to -0.5 V. In contrast, I–V relation of the input ESD protection circuit with a grounded VDD but a floating VSS is shown in Fig. 9(b). It is shown that the positive voltage on the input pad is limited to about 0.8 V but the negative voltage on the input pad is limited to around -13.4 V. With limited voltage of -13.4 V (13.6 V) by the MN1 (MN2) device, the gate oxide of both NMOS and PMOS devices in the input stage with a thickness of 180 Å can be safely protected by this proposed ESD protection circuit. The gates of MN1 and MN2 are also protected by themselves because the drain breakdown voltage of MN1 and MN2 is still lower than the breakdown voltage of the gate oxide.

Under normal CMOS operations with VSS of 0 V and VDD of 5 V, the voltage level of input signal is clamped by the diffusion diode and MN1 device. The I–V relation of this ESD protection circuit under such normal operating condition is shown in Fig. 10,

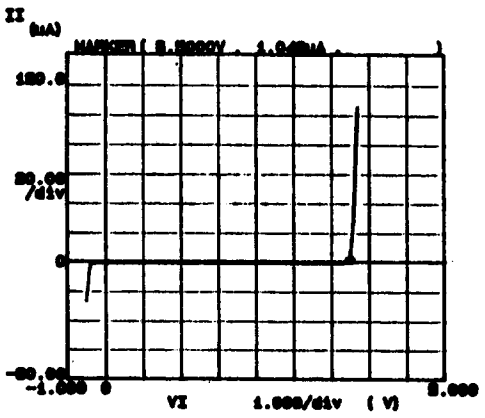

Fig. 10 Characteristics of the voltage-clamping effect of the proposed ESD protection circuit in the normal CMOS operating condition with the bias of 5 V VDD and 0 V VSS.

where the voltage level of input signal on the input pad is really clamped between -0.5 and 6.5 V. If the input ESD protection circuit is modified for mixed-voltage interface as that shown in Fig. 7, the high voltage level of input signal is clamped by the breakdown voltage of MN2 device. The I–V relation of an input pad with such modified ESD protection circuit is similar to that of Fig. 9(a).

There are two industrial ESD testing standards used widely in the world. One is the human body model (HBM), and the other is the machine model (MM). The HBM ESD (MIL-STD-883C method 3015.7) is to simulate the ESD from a human body to ICs. It has a capacitor C_b of 100 pF, and a discharging resistor R_b of 1.5 KΩ. ESD voltage is first stored on the capacitor C_b and then is discharged to DUT (device under test) through the resistor R_b. The MM ESD (EIAJ-IC-121 method 20) is to simulate the ESD from a machine to ICs. It has a larger capacitor C_m of 200 pF, but it has no resistor because the machine is generally made of metal. Resulting from the absence of a resistor in the discharging path of MM ESD, the ESD discharging current in MM is much larger and faster than that in HBM. Generally, the ESD failure threshold voltage in MM is about one tenth to one twelfth of that in HBM for the same ESD protection circuit. With a small layout area of only $100 \times 152\ \mu m^2$ (including latchup guard rings of VSS-biased $P+$ diffusion and VDD-biased $N+$ diffusion), the fabricated ESD protection circuit can sustain HBM (MM) ESD voltage above 4.5 KV (400 V) under the four modes of ESD stresses. The tester machine used in this ESD testing is the ZAPMASTER produced by KeyTek Corp. The ESD failure criterion is defined as the leakage current on the input pad above 1 μA under 5 V VDD bias.

This proposed input ESD protection circuit was included in a 0.8 μm standard cell library[21], which was widely used in many ASICs to provide high ESD

robustness for the input pins. In the whole-chip layout, the VDD and VSS power lines have to be placed in the way with the lowest resistance R_{dd} and R_{ss} (as shown in Fig. 2) to quickly bypass ESD current. An efficient VDD-to-VSS ESD protection circuit has to be added between the VDD and VSS to clamp the ESD voltage across the VDD and VSS power lines[22]. But, a strong input ESD protection circuit, such as the proposed ESD protection circuit in this article, is basically demanded to assemble a chip with high ESD reliability.

4. CONCLUSION

A latchup-free CMOS on-chip ESD protection circuit with thick- and thin-oxide n-type devices was designed, fabricated, and tested in a 0.8 μm CMOS process successfully. There are four effective ESD discharging paths in this input ESD protection circuit to one-by-one protect the internal circuits against the four-mode ESD stresses. The ESD current is mainly discharged by the thick-oxide devices in the PS-mode and ND-mode ESD stresses. The ESD voltage across the input gate oxide is clamped by the short-channel thin-oxide devices. In the NS-mode and PD-mode ESD stresses, the $N+$ diffusion junction diode and the thin-oxide device are forward conducting to bypass ESD current, respectively. Thus, this ESD protection circuit can fully protect the input stage of CMOS IC's without causing the unexpected ESD damage on the internal circuits. The experimental results have shown that this ESD protection circuit can provide effective ESD protection above 4.5 kV (400 V) in HBM (MM) ESD events within a small layout area of only $100 \times 152\ \mu m^2$. The voltage-clamping effect of this ESD protection circuit on the input signal can be also modified for application in the mixed-voltage interface.

With high ESD protection capability and small layout area, this proposed ESD protection circuit is very suitable to protect the input pads of high-integration CMOS ICs in the advanced submicron or deep-submicron CMOS technologies with LDD structure or silicided diffusion.

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