Latch-Up Protection Design With Corresponding Complementary Current to Suppress the Effect of External Current Triggers

Hui-Wen Tsai, *Student Member, IEEE*, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*—The robustness against latch-up in the integrated circuits can be improved by supporting complementary current at the pad under the latch-up current test (I-test). By inserting additional junctions to form parasitic bipolar sensors, the external trigger can be monitored, and the ESD protection devices can be applied to provide such current and decrease the related perturbation to the internal circuits. The proposed design and the previous work with a single guard ring have been fabricated in the same 0.5-μm 5-V process. The experimental results confirm the enhanced latch-up tolerance of this work and the practicability in the SOC era.**

***Index Terms*—Latch-up, electrostatic discharge (ESD) protection, guard ring.**

I. Introduction

IN the submicron scale CMOS process with high-area density or in high-voltage (HV) applications, the integrated circuits (ICs) designers need paying more attention to avoid latch-up problems at the inherent SCR paths [1]–[6]. For many commercial IC products, the resistances against latchup are guaranteed with samples passing the latch-up tests which follow the guidelines in JEDEC standards [7]. Table I is the trigger characterization in latch-up I-test specified in the up-to-dated JEDEC standard. There are positive I-test and negative I-test for distinguishing the applying current triggers and exploring the robustness of the device under test (DUT). Within the perturbation levels from the standards, the robustness of 100 mA or 200 mA against latchup is a familiar requirement in the datasheet of IC products.

In modern CMOS technology, electrostatic discharge protection (ESD) becomes an important design concern of IC products [8], [9]. An input buffer with conventional ESD protection is shown in Fig. 1 as an example. To ensure desired ESD level, conventional ESD-protection PMOS and NMOS transistors are added at input pads in ICs. However, besides for ESD performance, the latch-up immunity is also cared in the development of ESD cells. Several prior arts are thus proposed as [10], [11]. For traditional ESD-protection transistors, guard rings typically surround the devices as shown in the cell layout of Fig. 2 to decrease the susceptibility of latchup in both the input buffer and the internal circuits [12]–[14].

Besides the traditional strategy with guard ring protection, a modification is implemented in this work and verified to have enhanced latch-up immunity. The additional junctions are utilized to pick up some induced currents corresponding to the external trigger currents and turn them into the force to control the existing ESD devices for enhancing the resistance against the external perturbations. The latchup at internal circuit with traditional protection is first reviewed in Section II. The proposed design is then presented in Section III. The silicon realization and measurement results are organized in Section IV. A short discussion and conclusion are presented in Sections V and VI, respectively.

TABLE I
TRIGGER CHARACTERIZATION IN LATCH-UP I-TEST [7]

Latchup I-test	Range of Stress	Force Current
Positive I-test	I	< 50 mA
	II	50 mA to < 100 mA
	III	100 to 150 mA
	IV	150 to 200 mA
	V	>= 200 mA
Negative I-test	I	> -50 mA
	II	-50 mA to > -100 mA
	III	-100 mA to > -150 mA
	IV	-150 mA to >-200 mA
	V	<= -200 mA

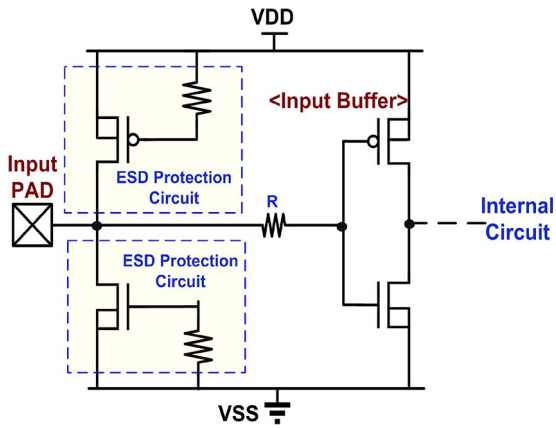

Fig. 1. Input buffer with GGNMOS and GDPMOS to provide general ESD protection.

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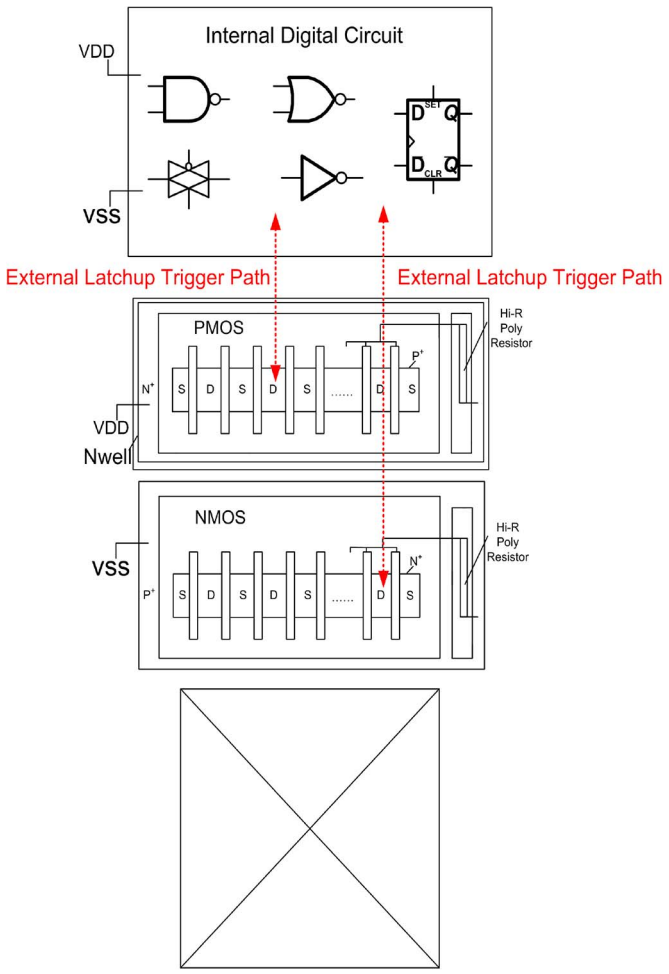


Fig. 2. The cell layout of input buffer with guard ring protection and common latch-up paths.

II. Latchup at Internal Circuits Induced by the Trigger Current at External Pins

In Fig. 3(a) and (b), the simplified cross-section views of traditional ESD-protection cell with guard rings at bulk terminals are shown. The depicted internal p-n-p-n structure represents the simulated detector formed in the internal digital circuits [15]. The related equivalent parasitics which contribute to the trigger of latchup at the internal p-n-p-n structure are also drawn in accordance with the external positive or negative I-test [16], [17]. When sufficient positive current is injected from the input pad as in Fig. 3(a), the parasitic $Q_{PNP}1$, $Q_{NPN}1$, and $Q_{PNP}2$ are turned on to pull high the ungrounded terminal of parasitic resistor Rpw. The internal p-n-p-n structure is thus triggered and causes latchup to happen. For negative current is applied at input pad as shown in Fig. 3(b) and turns on the $Q_{NPN}2$, the sink current will enlarge the emitter to base voltage of the effective PNP BJT at the internal P-N-P-N structure. Once the voltage is over the threshold of the PNP BJT, latchup is fired. For the structures in Fig. 3(a) and (b), the conductivity of the body diodes formed between the source and the bulk rings affect the amount of the induced current toward the external transients.

The advantage for the guard ring protection is the easiness for implementation and less area consumption. However, from the experimental results in [18], the testkeys composed of I/O transistors with 500-μm total width, less than 60-μm distance from pmos to sensitive latch-up detector, and protected by 3-μm wide single guard ring perform less than 40-mA immunity for positive I-test in 0.35-μm silicided bulk CMOS process. The similar trends also happen in the analysis among LDMOS and CMOS structure within 2-μm CMOS high-voltage process. The used testkeys in [19] without extra isolation structure between the MOS cells and the internal P-N-P-N structure performs ~30-mA latch-up immunity which is much less than the 100-mA trigger current level in JEDEC standards. In practical design, the performance can be better or worse depends on the sizes of the guard rings, the arrangement of the locations, the doping concentrations of the process, and etc. The devices or junctions between the internal sensitive paths to the pad also affect the final results of external latch-up test for the IC product. Sometimes in high-voltage applications, improper layout arrangements may cause EOS problem induced by the latch-up I-test and thus degrade the expected performance for the designs with guard ring protection [20], [21].

III. New Design to Generate Complementary Current Corresponding to External Triggers in Latch-Up I-Tests

To enhance the latch-up immunity against the perturbations, a novel design is shown in Fig. 4(a). The main function for this structure is to wake up the ESD-protection transistors (Mnesd and Mpesd) during latch-up I-test. Additional junctions are added to build effective bipolar transistor structures Qn_sen and Qp_sen at the gate terminals of Mnesd and Mpesd. The Qn_sen and Qp_sen work as the sensors to detect the amount of latch-up trigger current. One of the layout implementations is shown in Fig. 4(b) with related cross-section view as shown in Fig. 5. In this case, the additional n+ and p+ junctions located outside the guard ring of Mpesd are planned to be the effective collector terminals of Qn_sen and Qp_sen. The emitter and the base of Qn_sen and Qp_sen are implemented with existing drain terminals of the Mnesd or Mpesd and the substrate or n-well with n+ OD junction as depicted in Fig. 5. The collectors are connected to 10-kΩ Hi-R poly resistors (Rnsed or Rpesd) and the gate terminals of Mnesd or Mpesd, respectively. The operations for the proposed design under positive and negative I-test are shown in Fig. 6(a) and (b). The other intrinsic parasitic devices related to the latch-up triggered path are shown as $Q_{PNP}1$, $Q_{PNP}2$, $Q_{NPN}1$, $Q_{NPN}2$ which are also presented in the mentioned cross-section views at Fig. 3(a) and (b). When positive trigger current (Ipos_source) is applied from external source, the voltage of PAD is pulled over the supply voltage VDD. Therefore, Qp_sen may be turned on and produces sensing current related to the voltage difference between PAD and VDD generated by the trigger current. The external source current separately flows in the chip and can be presented as the composition by

$$I_{pos\_source} \cong I_{sink} + I_{p\_sen} + I_{db} + I_{pos\_trigger}, \quad (1)$$

where the Isink is the current sunk by the Mnesd, Ip_sen is the sensing current through Qp_sen, Idb is the drain to bulk current of Mpesd, and the Ipos_trigger is the trigger current flew to

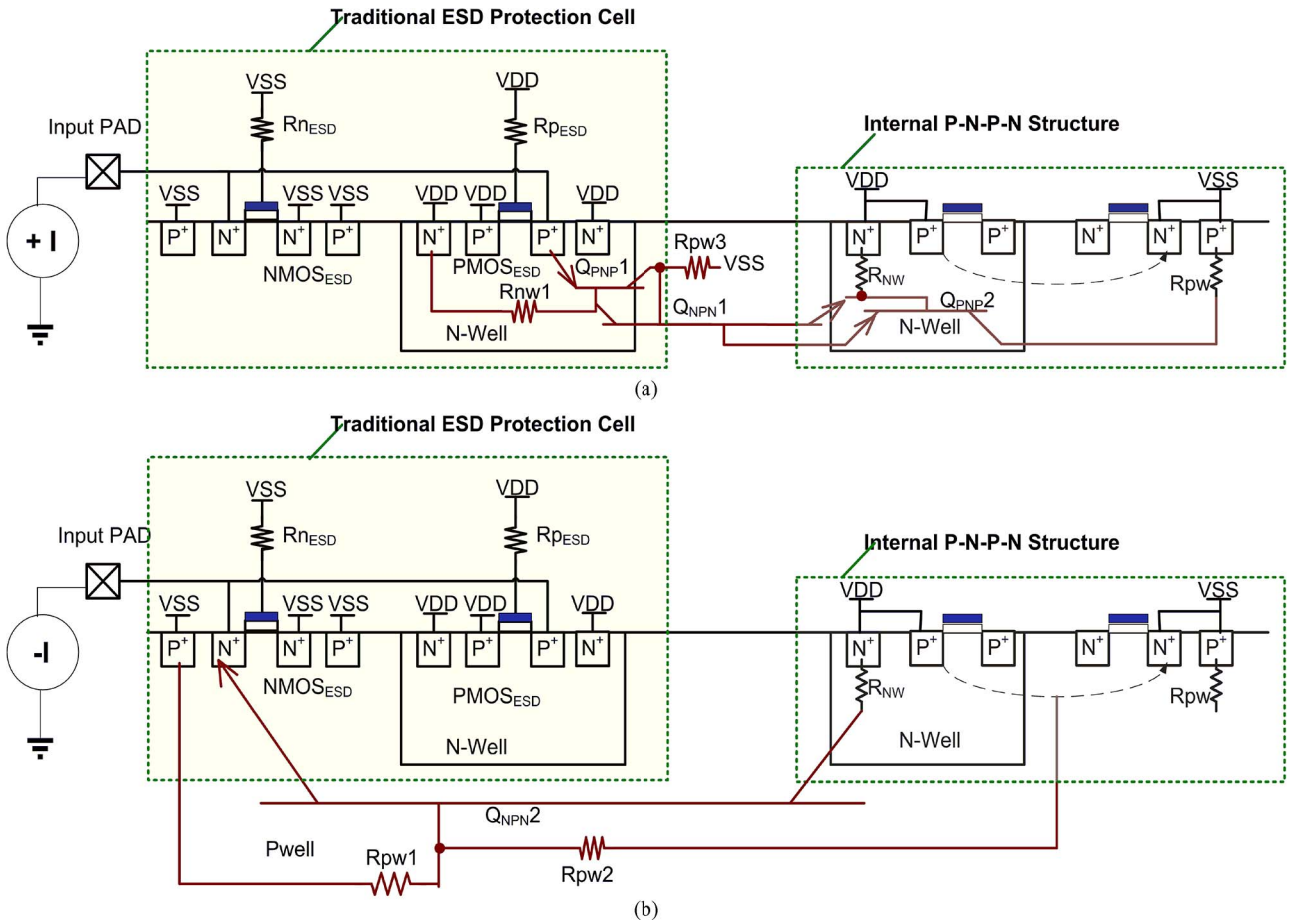


Fig. 3. Simplified cross-sectional views of traditional ESD-protection cell with guard rings to depict the related parasitic trigger paths to the internal P-N-P-N structure under (a) positive I-test and (b) negative I-test.

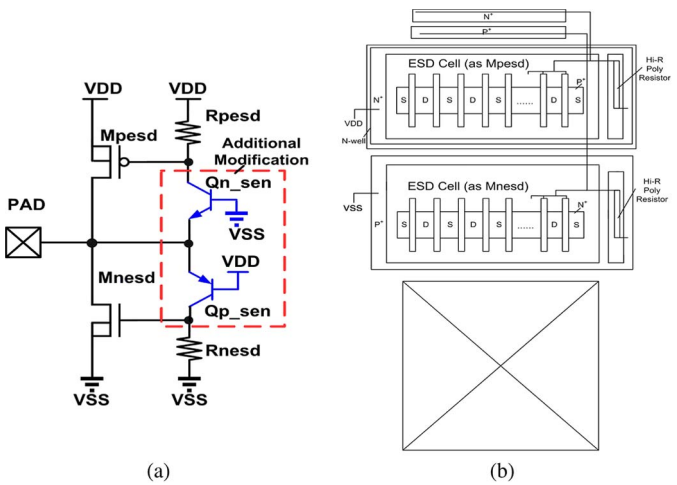


Fig. 4. (a) Schematic and (b) layout structure for the proposed design with additional modification.

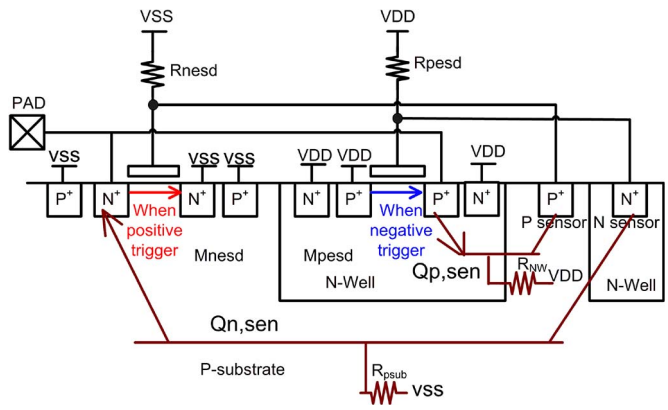


Fig. 5. Cross-sectional view for the proposed design.

Rpw3a. If the Ipos_trigger is large enough to make the base voltage of NPN bipolar transistor in the internal P-N-P-N structure high enough, latchup will be induced. Since Isink shares part of current from external positive source together with Ipos_trigger, the amount of Ipos_trigger is reduced corresponding to same Ipos_source by enhancing the amount of Isink. If Ip_sen is sufficient to pull high the gate terminal of Mpesd and turn on the transistor, quite amount of Isink current can be produced depending on the sizes of the devices. Thus, the latch-up immunity to the positive I-test can be improved with increased Isink generated due to the additional modification. Similar situation is also shown in negative I-test. The trigger current sunk by the external source can be approximately decomposed to several parts as indicated in

$$\mathrm{I_{neg\_source}} \cong \mathrm{I_{source}} + \mathrm{I_{n\_sen}} + \mathrm{I_{bd}} + \mathrm{I_{neg\_trigger}}, \qquad (2)$$

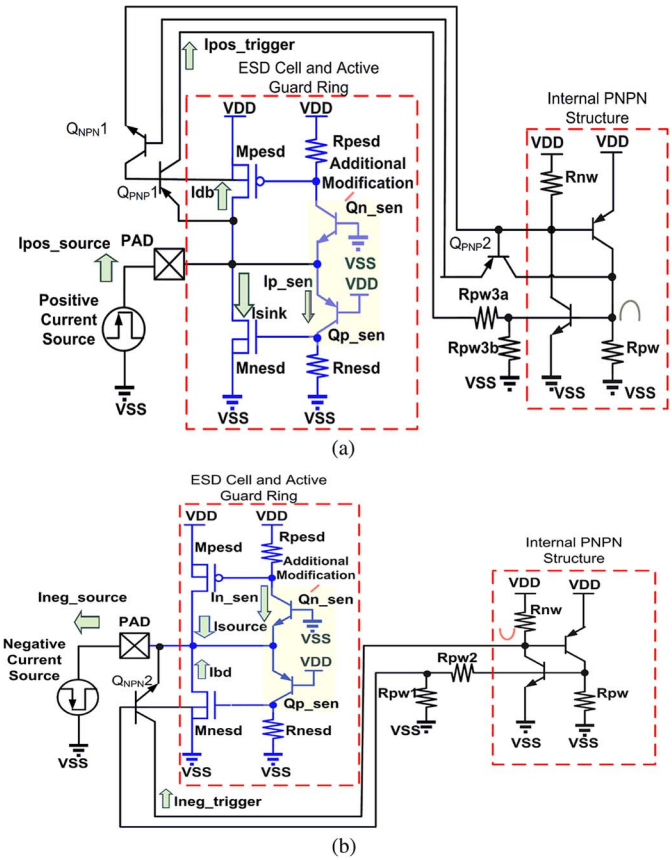


Fig. 6. Operations for the proposed design under (a) positive I-test and (b) negative I-test.

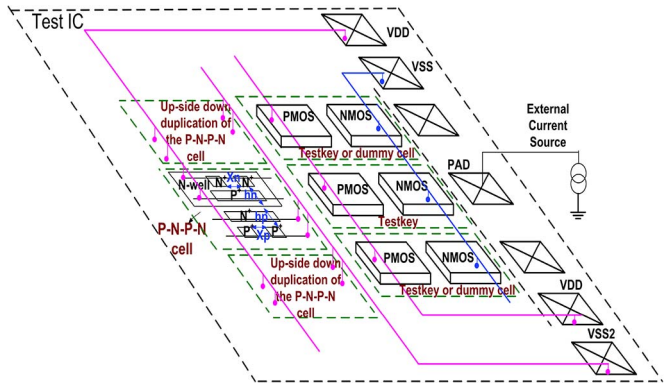


Fig. 7. Structure to verify the latch-up resistance of the previous and proposed works.

where the Isource is the current sourced from the Mpesd, In_sen is the sensing current through Qn_sen, Ibd is the bulk to drain current of Mnesd, and the Ineg_trigger is the trigger current flew from $Q_{NPN}2$. Sufficient Ineg_trigger can bring about enough emitter-to-base voltage to turn on the effective PNP BJT of the internal P-N-P-N structure and thus lead to the occurrence of latchup. From (2), Ineg_trigger can be reduced apparently if Isource is increased due to the turn-on of Mnesd under same negative trigger current from the PAD. With relatively diminished Ineg_trigger, the proposed design has better performance than the original guard ring design.

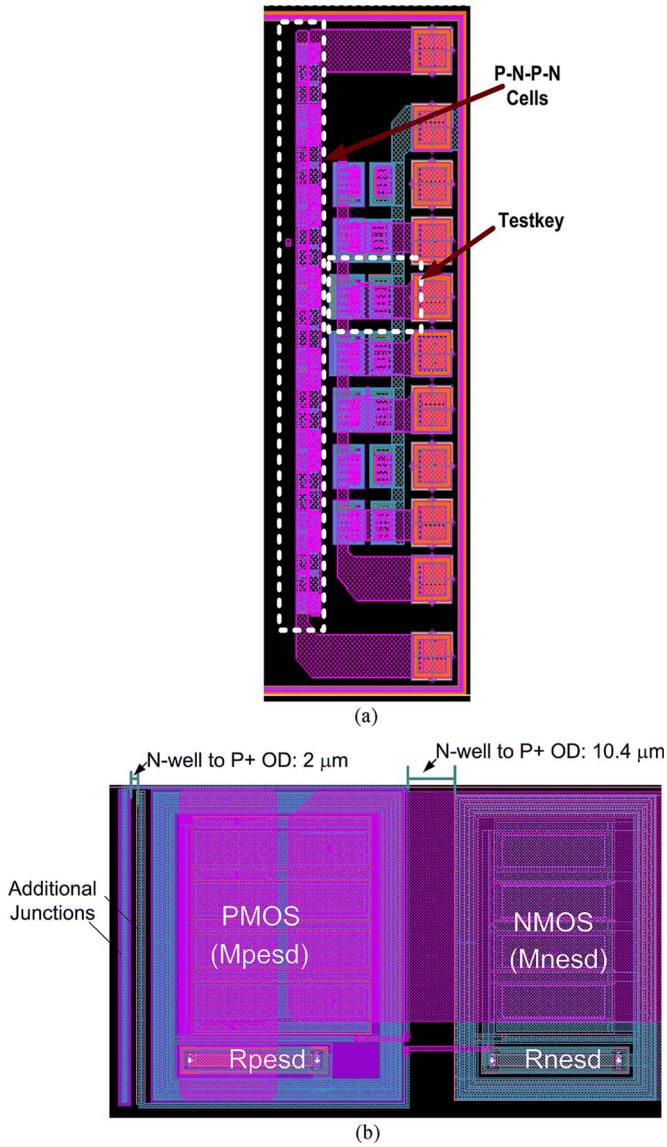


Fig. 8. Layout photo for (a) test chip and (b) testkey with proposed design.

IV. Experimental Results

The proposed design has been verified with the 5-V CMOS devices embedded in a 0.5-μm 5 V/15 V/25 V/40 V BCD process. Although the proposed design was not verified with a pure 5-V technology, the proposed design will still work at the pure 5-V CMOS technology. The simplified graph for the structure to investigate the latch-up resistance of the previous and proposed works is shown in Fig. 7 [18]. The P-N-P-N cell is used to emulate the latch-up structure in general circuits at internal blocks and are repeatedly placed behind the testkeys. The specified distances (hn, hp, Xn, Xp) in each P-N-P-N cell are 35 μm, 35 μm, 20 μm, and 20 μm, which follow the typical suggested maximum values provided by foundry. Whether latchup is triggered in these cells or not in accordance with different trigger currents is affected by the test cell placed between the pad and the P-N-P-N cells. Thus, those P-N-P-N cells serve as internal latch-up detector to judge latch-up immunity of the testkeys. Fig. 8(a) shows the layout photo in the fabricated test chip which contains mentioned test structures. Fig. 8(b) shows

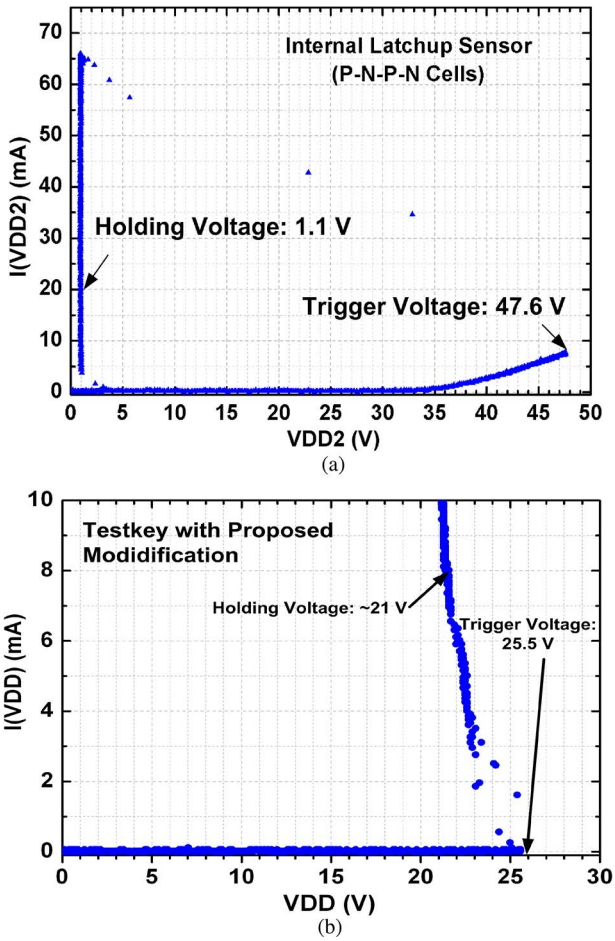


Fig. 9. Measured latch-up I–V characteristics of (a) internal latch-up sensor and (b) testkey with proposed modification.

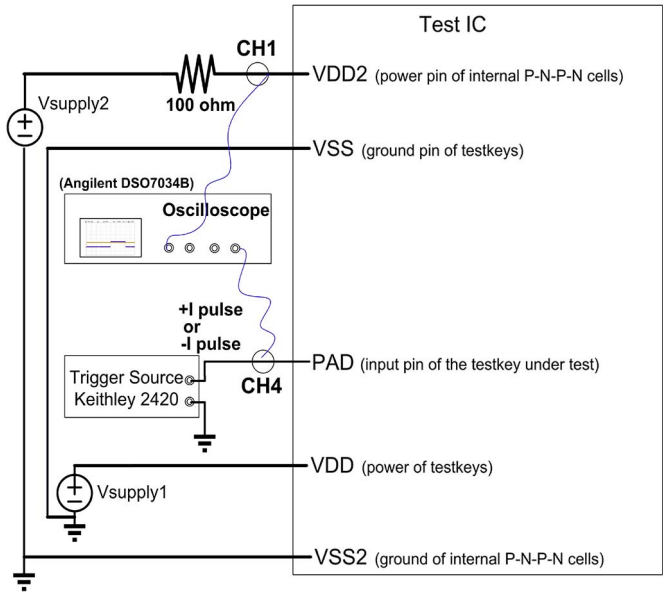


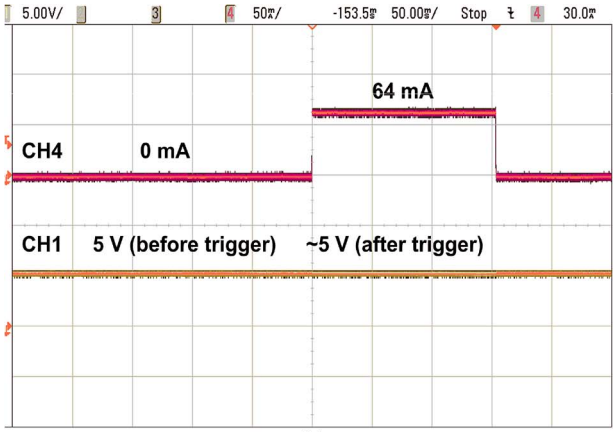
Fig. 10. Experimental setup to verify the latch-up resistance for previous art and the designs with proposed modification.

the enlarged layout graph for a test cell with proposed design in the tape-out chips. The additional junctions are drawn as wide to place one row of contacts on the OD strobes. The distance between the p+ and n+ rings is 10.4 μm and the distance between the testkeys and internal P-N-P-N cells is 30 μm.

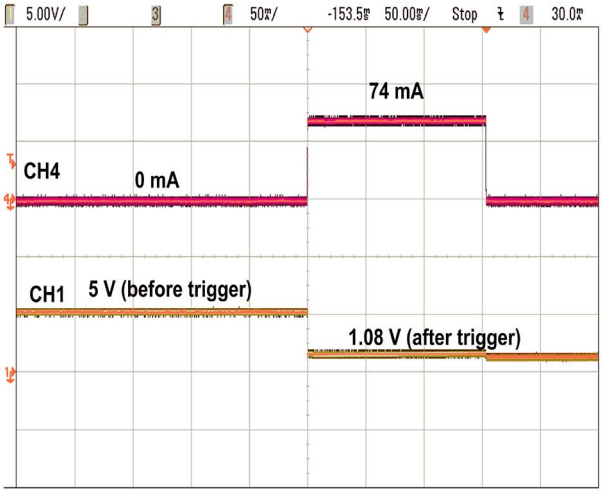
The I–V characteristics of the inner P-N-P-N cells and proposed design are measured by the *Tek*370B curve tracer at room temperature. The trigger voltages of these P-N-P-N cells are near 47.6 V and the holding voltages are near 1.1 V as shown in the I–V curve in Fig. 9(a). The I–V curve of the proposed work is also presented in Fig. 9(b), where the trigger voltage is near 25.2 V and the holding voltage is near 21 V, respectively. The 47-V breakdown voltage is due to the junction breakdown between the n-well layer and the p-type substrate in the given high-voltage process. Besides, in the testkey, the I/O cell is implemented with 5-μm single guard ring around both Mpesd and Mnesd and the related distance between the bulk rings of Mpesd and Mnesd transistors is 10.4 μm. The 21-V high holding voltage of the parasitic SCR path (from VDD to VSS) in the I/O cell is due to the surrounding guard rings and sufficient distance for the PNPN path between the Mpesd and Mnesd in the adopted 0.5 μm 5 V/15 V/25 V/40 V BCD process. The purpose of the high holding voltage in the I/O cell is to maintain latch-up free at the I/O cell, so that the latch-up performance can be judged accurately due to the triggering of the internal PNPN cells toward different external trigger current levels that applied at the I/O pad. The latchup occurrence located in the internal circuit blocks (but not located at the I/O cell) was illustrated in Fig. 3, when the positive/negative trigger current is applied to the I/O pad.

The I/V curves show that if trigger source is applied at supply, P-N-P-N cells can sustain much higher voltage perturbation to launch latchup than the proposed test cell does. Thus, the occurrence of latchup for the P-N-P-N cell can be attributed to the perturbations from the pad instead of its supply voltage if the proposed test cell itself is not triggered in the external latch-up test of pad.

The experimental setup to verify the latch-up resistance for the previous art and the design with proposed modification is shown in Fig. 10. The *Keithley* 2420 serves as required trigger current source and is connected to the pad. Two dc power supplies (Vsupply1 and Vsupply2) are used to bias the supply voltages of test designs and P-N-P-N cells at 5 V, separately. A resistor of 100 Ω is connected between the external power supply and the supply pin of the internal P-N-P-N cells (VDD2) to limit the large latch-up current and avoid immediate damage in the experiments. Measured waveforms from oscilloscope for one implemented testkey with proposed design are shown as Figs. 11 and 12 for positive and negative I-test. The total widths for ESD protection PMOS and NMOS are 720 μm and 480 μm. Minimum lengths are also used as 0.6 μm and 0.7 μm for all the NMOS and PMOS in the test chips, respectively. When 64-mA positive trigger current (as CH4) is applied at PAD as shown in Fig. 11(a), the voltage at VDD2 (as CH1) keeps at $\sim$5V since latchup is not happened and few current flows through the resistor. When larger trigger current is applied as 74 mA as shown in Fig. 11(b), the voltage at VDD2 drops suddenly and keeps near 1.08 V which means latchup happens at the internal P-N-P-N cells. For negative I-test presented in Fig. 12(a) and (b), the latchup doesn't happen when $-$810-mA trigger current is applied while it is occurred as $-$820-mA

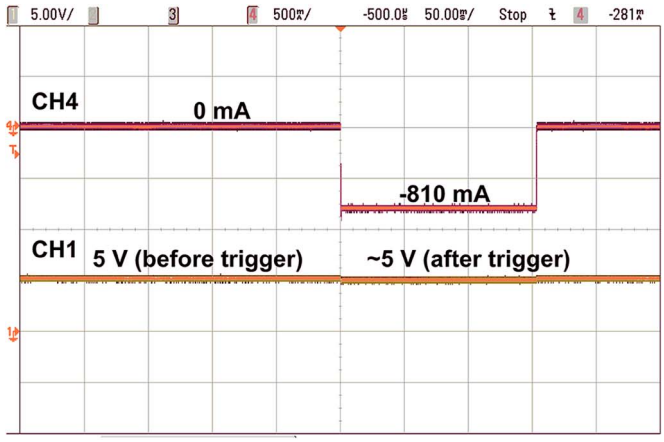


(a)

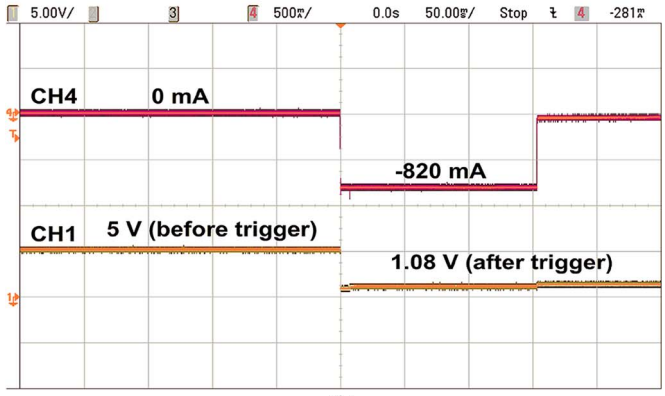


(b)

Fig. 11. Measured waveforms of proposed design under positive I-test with (a) 64-mA and (b) 74-mA trigger current applied at input pad.



(a)



(b)

Fig. 12. Measured waveforms of proposed design under negative I-test with (a) 810-mA and (b) 820-mA negative trigger current applied at input PAD.

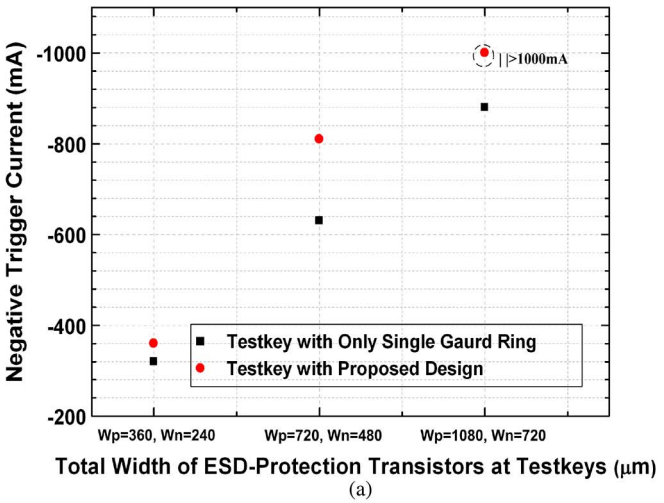
current pulse is provided at input pad. With intrinsic NPN BJT from the drain terminal of Mnesd to the bulk terminal of Mpesd as current provider and inherently farer distance between internal latch-up sensor to NMOS than to PMOS, the proposed design and the prior art tolerate higher trigger level in negative I-test than in positive I-test.

Further organizations for the trigger current to fire latchup and the relations with the dimensions of the ESD-protection transistors in the testkeys are shown in Fig. 13(a) and (b). The designs with proposed modification has higher latch-up immunity compared with the previous art with only single guard ring at both positive and negative I-test. For total widths as Wp $= 360$ μm and Wn $= 240\mu$m, the proposed design can sustain up to $\sim$32-mA positive current and 360-mA negative current without encountering latchup while the previous art can only tolerate $\sim$13-mA positive trigger current and $\sim$320-mA negative trigger current. When the transistor dimensions are larger, the sustainable current is also increased. For the proposed design with Wp $= 1080$ μm and Wn $= 720$ μm, the trigger current to induce latchup can be up to $\sim$94 mA and larger than 1000 mA for positive and negative trigger current, respectively. The HBM (human body model) ESD robustness under different pin combinations of ESD test on the I/O pin [22] is also examined and shown in Table II for the testkeys with Wp $= 360$ μm and Wn $= 240$ μm. The weakest mode is the ND mode with 3-kV performance, and 8-kV performance is achieved in the NS and PD mode. Since the tolerated levels for the listed ESD modes are similar at both designs, it has been verified that the proposed design of this work can improve the latch-up immunity without degrading the ESD robustness.

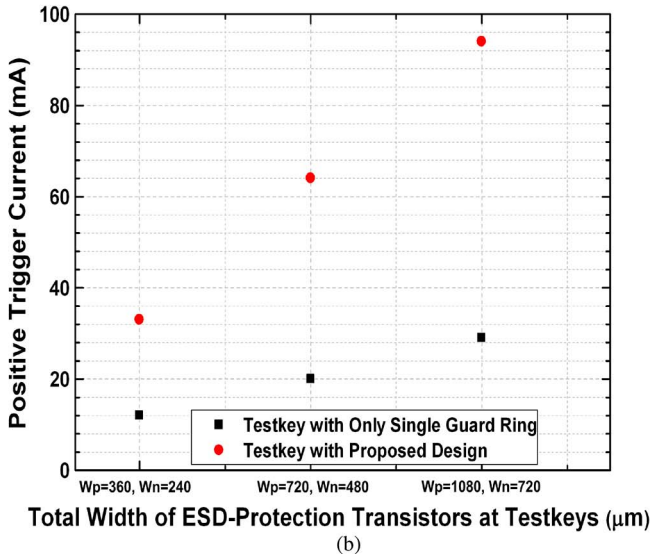
V. Discussion

Since the latch-up immunity of proposed design is deeply related to the dimensions of the ESD-protection transistors, for commercial product with requirements of 100-mA trigger current tolerance, design with sufficient ESD-protection transistor sizes help to meet the specifications. For the cases without sufficient dimensions for ESD devices or higher trigger current requirements is demanded, multiple rings [18], [19] may be also considered to achieve the goal with the trade of area consumption.

For the application of the proposed design, the required device sizes of the ESD transistors for latch-up immunity enhancement can be initially estimated by the simulation. The Rpesd and Rnesd can be chosen with a typical value for ESD protection such as 10 kΩ. The parameters of the additional parasitic bipolar transistors can be investigated by splitting testkeys at the target process. In this work, the optimization was not covered. However, according to the measured improvement (from 13-mA to 94-mA under the positive I-test) of the testkey



(a)



(b)

Fig. 13. Relations between the applied trigger current at input pad to fire latchup and the dimensions of the ESD-protection transistors used in the testkeys (with only single guard ring and with proposed design) under (a) positive I-test and (b) negative I-test.

TABLE II
HBM ESD ROBUSTNESS OF THE TESTKEYS

ESD-test Mode	Types for Testkeys	
	Testkey with Single Guard Ring	Testkey with The Proposed Design
Positive-to-VSS mode (PS mode)	5.5 kV	5.5 kV
Negative-to-VSS mode (NS mode)	>8 kV	>8 kV
Positive-to-VDD (PD mode)	>8 kV	>8 kV
Negative-to-VDD (ND mode)	3 kV	3 kV

without optimization, the novel concept for latchup prevention proposed in this work has been verified to be a considerable solution without degradation of ESD performance if sufficient dimension of ESD devices are available.

VI. CONCLUSION

The presented design shows an embodiment to activate the existing ESD devices by additional junctions when latch-up current perturbations are applied. With ESD-protection PMOS and NMOS transistors sized as 1080 μm/0.7 μm and 720 μm/0.6 μm for the total width/ length, the testkey with proposed design can tolerate ~94-mA positive trigger current and larger than 1000-mA negative trigger current, respectively, compared with the immunity of ~29-mA positive and ~890-mA negative currents for the testkey drawn with single guard ring. The enhancement can be more if the driving abilities of the ESD-protection transistors are improved. This novel design can be combined with the traditional guard ring design to offer higher latch-up immunity without degradation ESD levels of the I/O cells.

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