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TRANSIENT ANALYSIS OF SUBMICRON CMOS LATCHUP WITH A PHYSICAL CRITERION

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Abstract—A new physical criterion and an analytical timing model for transient latchup in a p–n–p–n structure are developed and verified. In the new physical transient latchup criterion, two new parameters called the large-signal transient current gains of the parasitic vertical and lateral BJTs in the p–n–p–n structure are defined. If their product rather than the forward beta-gain product becomes larger than unity right after triggering and remains larger than unity, the latchup occurs. With the piecewise-linearized device currents of the parasitic BJTs and the averaged junction depletion and diffusion capacitances in the p–n–p–n structure, the large-signal transient current gains are derived as functions of time and device parameters. Moreover, the dynamic behaviors and the associated timing of transient latchup can also be fully characterized. Model calculation results using the developed criterion and timing model agree very well with both SPICE simulation and experimental results. Thus the developed criterion and timing model can be applied to transient latchup analysis and prediction in CMOS ICs.

1. INTRODUCTION

As the device dimensions are scaled to the submicron range, latchup becomes a more serious problem to be solved. Latchup, which creates a low impedance path in the inherent parasitic p–n–p–n structure from the power supply V_{DD} to ground, is one of the major failure mechanisms of bulk CMOS ICs. Thus latchup characterization and prevention are important issues in developing submicron CMOS technology.

Since latchup is mostly triggered in the dynamic mode, transient latchup and its mechanism have attracted much attention recently[1–15]. Some efforts have been contributed to characterize transient latchup[1–9], including using 2-D numerical simulations[10–15]. However, a good criterion for transient latchup is required so that it can be used with the accurate characterization models to judge whether the p–n–p–n structure is triggered into its latchup state. Otherwise, extensive trial-and-error steps are required, which may consume too much computing resource.

A criterion for transient latchup initiated by current pulses has been proposed[8]. In that criterion, a quantitative change of charges stored in the junction capacitances of the p–n–p–n structure was selected to predict the occurrence of latchup. It was found that the change of charges remains unchanged when the p–n–p–n structure is triggered into latchup by different pulse currents. The constant change of charges can only be obtained empirically from the trial-and-error SPICE simulations and used as a criterion to judge the occurrence of latchup triggered by different pulse currents. The reason why the change of charges at the base nodes of a p–n–p–n structure keeps constant when it is triggered into latchup is still not clear. Thus an explicit formula for the change of charges and the criterion cannot be obtained. This not only complicates the numerical calculation but blocks the physical understanding on the mechanism of transient latchup, although the criterion can accurately predict the required current pulse to trigger latchup.

In our work, the dynamic mechanism of transient latchup is explored and a general physical criterion is developed[16]. As compared to the previous criterion, this new criterion has an explicit formula which is associated with both device parameters and circuit parameters of the p–n–p–n structure. The criterion can also provide a clear understanding of the mechanism of transient latchup. Thus it is called a physical criterion. Based upon the developed criterion, the time and the magnitude of trigger sources required to cause a latchup in any p–n–p–n structure can be accurately calculated through a timing model without any trial-and-error process. Using the definition in the previous work[8], the change of charges at the base nodes of a p–n–p–n structure can be directly calculated from the new developed criterion and timing model. Our criterion is general because it can be applied to various triggering cases and to analytical and numerical analyses.

In order to enhance the physical understanding of the latchup transition, a rigorously simplified quasi-analytical timing model was developed. It is based upon the physical criterion[16] and the classical two-transistor model of a p–n–p–n structure[1–8] with the

device parameters extracted from the fabricated p–n–p–n structure in CMOS ICs. With the physical criterion and the exactly extracted device parameters including the current-dependent beta gain, the voltage-dependent junction capacitances, and the transit time (calculated from the measured unity-gain frequency), the developed timing model can provide a reasonably accurate characterization on the transient latchup parameters.

The dynamic behaviors of transient latchup in a p–n–p–n structure are analyzed and the large-signal transient current gains are defined and derived in Section 2. From the theoretical analysis of the current i_{DD} which flows out from the voltage supply V_{DD} source and the verification of SPICE simulated waveforms, a physical criterion for transient latchup which is related to the product of large-signal transient current gains is proposed[16]. With the piecewise-linearized bipolar junction transistor (BJT) currents and the averaged junction capacitances, a timing model of transient latchup is developed in Section 3. Using the timing model and the physical criterion, the relations between the minimum pulse width and the magnitude of pulse-type trigger currents for transient latchup initiation can be directly calculated. Comparisons of theoretical calculations results with both SPICE simulated and experimental results are given in Section 4. Good agreement among these results confirms the validity of the proposed latchup criterion and timing model. Finally, a conclusion is given in Section 5.

2. TRANSIENT LATCHUP CRITERION

To simplify the analysis and get a physical insight into the dynamic mechanism, transient latchup is characterized by the traditional two-transistor model [1–8]. Figure 1(a) shows the cross-sectional view of a CMOS inverter and its parasitic p–n–p–n latching path in p-well n-substrate CMOS technology. The corresponding lumped two-transistor equivalent circuit is shown in Fig. 1(b), where $Q1$ is the parasitic lateral p–n–p transistor and $Q2$ is the parasitic vertical n–p–n transistor. The $Q1$ transistor is

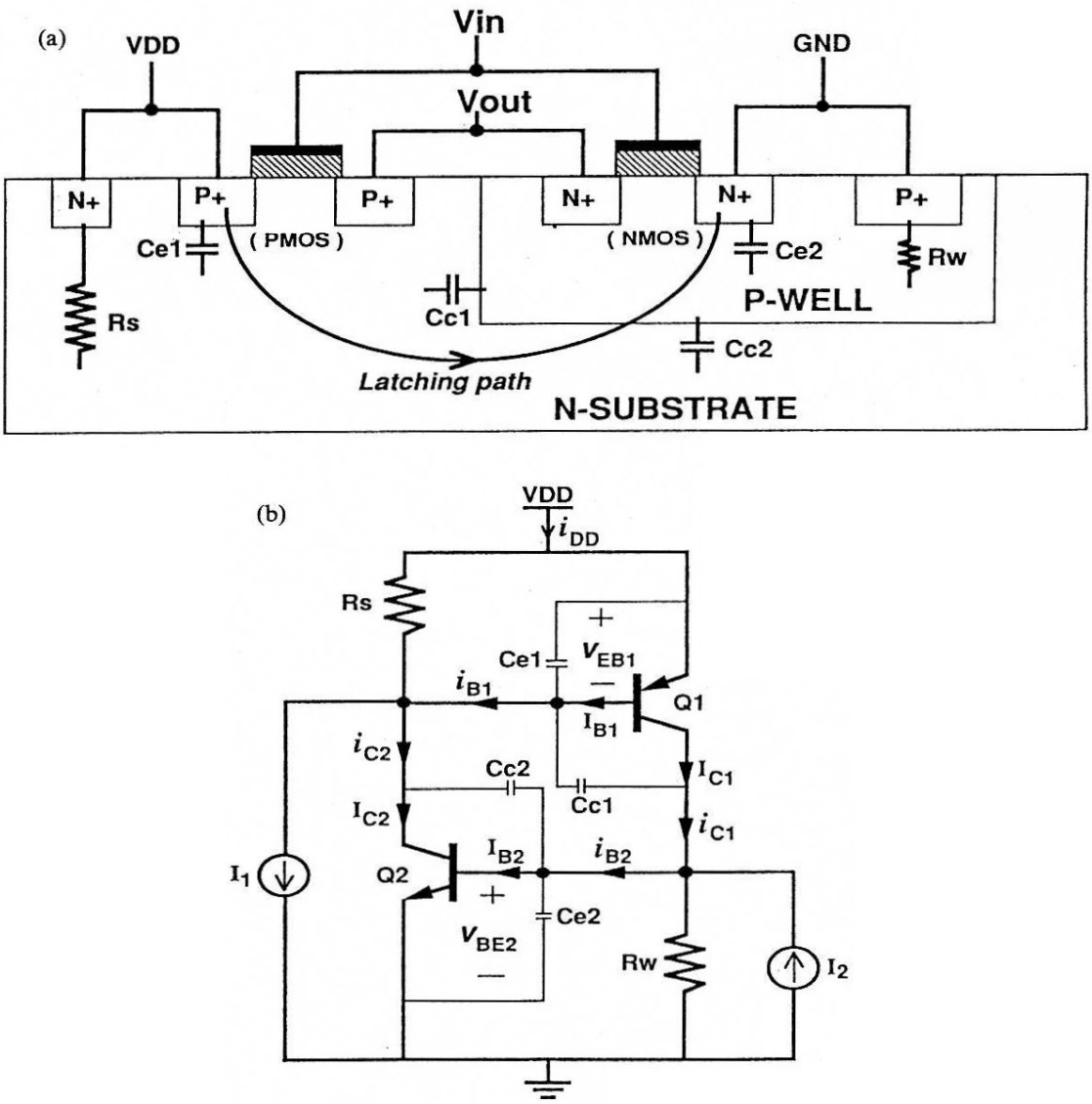

Fig. 1. (a) The cross-sectional view of a CMOS inverter and the parasitic resistances and capacitances of a p–n–p–n structure; (b) the lumped equivalent circuit of the p–n–p–n structure in (a).

Table 1. The current equations of the BJT used in SPICE[18]

The modified Gummel–Poon model in forward active region

1. Base current:

$$I_B = \frac{I_S}{\beta_F} \cdot (e^{V_{BE}/V_T \cdot N_F} - 1) + I_{SE} \cdot (e^{V_{BE}/V_T \cdot N_E} - 1) + \frac{I_S}{\beta_R} \cdot (e^{V_{BC}/V_T \cdot N_R} - 1) + I_{SC} \cdot (e^{V_{BC}/V_T \cdot N_C} - 1).$$

2. Collector current:

$$I_C = \frac{I_S}{q_b} \cdot (e^{V_{BE}/V_T \cdot N_F} - e^{V_{BC}/V_T \cdot N_R}) - \frac{I_S}{\beta_R} \cdot (e^{V_{BC}/V_T \cdot N_R} - 1) - I_{SC} \cdot (e^{V_{BC}/V_T \cdot N_C} - 1).$$

3. Emitter current:

$$I_E = I_B + I_C,$$

where

$$q_b = \frac{q_1}{2} \cdot [1 + (1 + 4 \cdot q_2)^{0.5}]$$

$$q_1 = \frac{1}{1 - \frac{V_{BC}}{V_{AF}} - \frac{V_{BE}}{V_{AR}}}$$

$$q_2 = \frac{I_S}{I_{KF}} \cdot (e^{V_{BE}/V_T \cdot N_F} - 1) + \frac{I_S}{I_{KR}} \cdot (e^{V_{BC}/V_T \cdot N_R} - 1)$$

V_T(thermal voltage) $= k \cdot T/q$.

composed of p^+ diffusion as emitter, n-substrate as base, and p-well as its collector. The $Q2$ transistor is composed of n-substrate as collector, p-well as base, and n^+ diffusion in p-well as its emitter. The interconnected bases and collectors of the transistors $Q1$ and $Q2$ form a silicon controlled rectifier (SCR) circuit. *Rs* and *Rw* represent the inherent substrate and well shunt resistances across the base–emitter junctions of the transistors $Q1$ and $Q2$, respectively. *Ce*1, *Cc*1, *Ce*2, and *Cc*2 in Fig. 1(a,b) are the bias-dependent junction capacitances. In the equivalent circuit, $I_1(I_2)$ is the external trigger current in the n-substrate (p-well).

Taking the effects of junction depletion and diffusion capacitances into considerations and using the modified Gummel–Poon model of BJTs in SPICE [17,18], the base–emitter voltages $v_{EB1}(t)$ and $v_{BE2}(t)$ in Fig. 1(b) can be expressed as:

$$\frac{\partial v_{EB1}(t)}{\partial t} = \frac{I_{F1} \cdot (Cc1 + Cc2 + Ce2) - I_{F2} \cdot (Cc1 + Cc2)}{\Delta_C} \quad (1)$$

$$\frac{\partial v_{BE2}(t)}{\partial t} = \frac{I_{F2} \cdot (Cc1 + Cc2 + Ce1) - I_{F1} \cdot (Cc1 + Cc2)}{\Delta_C}, \quad (2)$$

where

$$\Delta_C \equiv (Cc1 + Cc2) \cdot (Ce1 + Ce2) + Ce1 \cdot Ce2 \quad (3)$$

$$I_{F1} \equiv I_{C2} - I_{B1} - \frac{v_{EB1}}{Rs} + I_1 \quad (4)$$

$$I_{F2} \equiv I_{C1} - I_{B2} - \frac{v_{BE2}}{Rw} + I_2. \quad (5)$$

The detailed derivation of the above equations is given in Appendix A with a reasonable assumption of "$\partial(C_j \cdot v_j)/\partial t \cong C_j \cdot (\partial v_j/\partial t)$", where the C_j and v_j represent the capacitance and its voltage bias of each junction in the p–n–p–n structure. I_{B1}, I_{B2}, I_{C1}, and I_{C2} in (4) and (5) are the intrinsic base and collector currents of the BJTs $Q1$ and $Q2$, respectively. These currents are exponential functions of the BJT terminal voltages as shown in Table 1. The *Ce*1(2) and *Cc*1(2) in (1)–(3) are the base–emitter and base–collector junction capacitances of $Q1(2)$, respectively. All these capacitances are dependent upon their junction voltages as shown in Table 2. Thus, $v_{EB1}(t)$ and $v_{BE2}(t)$ are nonlinear differential equations of time, trigger currents, and device parameters of the BJTs $Q1$ and $Q2$ in the p–n–p–n structure. These equations can only be solved by intricate numerical methods. The time-varying $v_{EB1}(t)$ and $v_{EB2}(t)$ are the basically dominant factors in the lumped equivalent circuit and can be used to model the latchup transition in Section 3.

To develop the transient latchup criterion, new transient parameters called the time-dependent large-signal transient current gains $\beta_{1tr}(t)$ and $\beta_{2tr}(t)$ of the transistors $Q1$ and $Q2$, respectively, are defined from

Table 2. The equations of junction diffusion and depletion capacitances of a BJT used in SPICE[18]

1. The junction diffusion capacitances: C_{tbe} and C_{tbc}

$$C_{tbe} = \tau_F \cdot \frac{\partial(I_{BE}/q_b)}{\partial V_{BE}} \quad \text{for forward-biased base–emitter junction;}$$

$$C_{tbc} = \tau_R \cdot \frac{\partial(I_{BC})}{\partial V_{BC}} \quad \text{for reverse-biased base–collector junction,}$$

where

$$I_{BE} = I_S \cdot (e^{V_{BE}/V_T \cdot N_F} - 1) \quad \text{for } V_{BE} > 0$$

$$I_{BC} = I_S \cdot (e^{V_{BC}/V_T \cdot N_R} - 1) \quad \text{for } V_{BC} < 0$$

q_b has been listed in Table 1.

2. The junction depletion capacitances: C_{jbe} and C_{jbc}

$$C_{jbe} = \frac{C_{je0}}{\left[1 - \frac{V_{BE}}{\phi_E}\right]^{m_E}} \quad \text{for } V_{BE} < FC \cdot \phi_E,$$

$$C_{jbe} = \frac{C_{je0}}{[1 - FC]^{(1+m_E)}} \cdot \left[1 - FC \cdot (1 + m_E) + m_E \cdot \frac{V_{BE}}{\phi_E}\right] \quad \text{for } V_{BE} \geq FC \cdot \phi_E;$$

and

$$C_{jbc} = \frac{C_{jc0}}{\left[1 - \frac{V_{BC}}{\phi_C}\right]^{m_C}} \quad \text{for } V_{BC} < FC \cdot \phi_C,$$

$$C_{jbc} = \frac{C_{jc0}}{[1 - FC]^{(1+m_C)}} \cdot \left[1 - FC \cdot (1 + m_C) + m_C \cdot \frac{V_{BC}}{\phi_C}\right] \quad \text{for } V_{BC} \geq FC \cdot \phi_C.$$

where

C_{je0} = zero-biased base–emitter junction capacitance;

C_{jc0} = zero-biased base–collector junction capacitance;

m_E and $m_C = 0.5$ for abrupt junction;

m_E and $m_C = 1/3$ for grading junction;

$FC = 0.5$ (default);

ϕ_E = base–emitter built-in potential (0.75 V, default);

ϕ_C = base–collector built-in potential (0.75 V, default).

the large-signal base and collector currents which include the transient currents of junction capacitances. $\beta_{1tr}(t)$ and $\beta_{2tr}(t)$ can be written as:

$$\beta_{1tr}(t) \equiv \frac{i_{C1}(t)}{i_{B1}(t)} \tag{6}$$

$$\beta_{2tr}(t) \equiv \frac{i_{C2}(t)}{i_{B2}(t)}. \tag{7}$$

Using the relations of (1)–(5) and (A1)–(A11), $\beta_{1tr}(t)$ and $\beta_{2tr}(t)$ can be derived as:

$$\beta_{1tr}(t) = \frac{\Delta_C \cdot I_{C1} - I_{F1} \cdot Cc1 \cdot Ce2 - I_{F2} \cdot Cc1 \cdot Ce1}{\Delta_C \cdot I_{B1} + I_{F1} \cdot (\Delta_C - Cc2 \cdot Ce2) - I_{F2} \cdot Ce1 \cdot Cc2} \tag{8}$$

$$\beta_{2tr}(t) = \frac{\Delta_C \cdot I_{C2} - I_{F2} \cdot Cc2 \cdot Ce1 - I_{F1} \cdot Cc2 \cdot Ce2}{\Delta_C \cdot I_{B2} + I_{F2} \cdot (\Delta_C - Cc1 \cdot Ce1) - I_{F1} \cdot Ce2 \cdot Cc1}. \tag{9}$$

Note that $\beta_{1tr}(t)$ and $\beta_{2tr}(t)$ are heavily dependent upon the junction capacitances of $Q1$ and $Q2$. In the d.c. case, they reduce to the forward beta gains. The product of $\beta_{1tr}(t)$ and $\beta_{2tr}(t)$ is an important parameter to judge the transient latchup occurrence as will be described later.

Based upon the definition of $\beta_{1tr}(t)$ and $\beta_{2tr}(t)$ in (6) and (7), respectively, the instantaneous current i_{DD} flowing out from the voltage source V_{DD} right after the current triggering can be derived by taking all the transient currents in the device capacitances into considerations and expressed as:

$$i_{DD} = \frac{\beta_{1tr} \cdot \beta_{2tr} \cdot (v_{BE2}/Rw + v_{EB1}/Rs) + \beta_{2tr} \cdot (v_{BE2}/Rw) + \beta_{1tr} \cdot (v_{EB1}/Rs)}{\beta_{1tr} \cdot \beta_{2tr} - 1}. \tag{10}$$

Note that this i_{DD} also varies with time because $\beta_{1tr}(t)$, $\beta_{2tr}(t)$, $v_{EB1}(t)$, and $v_{BE2}(t)$ are all functions of time during the latchup transition. But, the $v_{EB1}(t)$ and $v_{BE2}(t)$ will hold about 0.8–0.9 V if both $Q1$ and $Q2$ are turned on in the p–n–p–n structure. Thus v_{BE2}/Rw and v_{EB1}/Rs are of some finite values. If $0 < \beta_{1tr} \cdot \beta_{2tr} < 1$ in (10), i_{DD} has a negative value which means that transient current would flow into V_{DD}. But this condition is impossible from the circuit operation and it implies that the degenerative process occurs and latchup is not sustained. This is the state without latchup. If $\beta_{1tr} \cdot \beta_{2tr} \geq 1$, i_{DD} is positive which means the current flows out from V_{DD} after current triggering and the regeneration process starts to sustain latchup. This is the latchup state.

The above latchup judgment has been verified by many SPICE simulation results. One of the typical SPICE simulated waveforms in both latchup and non-latchup cases are shown in Fig. 2(a–d) for different trigger-current pulse widths and Rs (Rw) = 800 (5600)Ω. It is clear from Fig. 2(a) that v_{EB1} (v_{BE2}) in the latchup case maintains at about 0.8 (0.85)V after the pulse-type current triggering, whereas those in the non-latchup case drop to 0 V. Figure 2(b) shows the product of the forward beta gains during the transient operation. The forward beta gain is defined as the ratio of the collector current over its corresponding base current without including the transient currents in the device capacitances of a p–n–p–n structure. Although the forward beta current-gain product in the non-latchup case is even as high as about 206 after triggering, it still does not cause latchup. On the other hand, the curves in Fig. 2(c) show the product of the large-signal transient current gains, which first raises to be above unity and then maintains at 1.431 in the latchup case. In the non-latchup case, the product drops to be below unity right after the pulse-type current triggering. This exactly coincides with the theoretical prediction from (10). Note that the transient currents of the junction capacitances make the product of the forward beta current gains very different from that of the large-signal transient current gains. The corresponding i_{DD} waveform is also shown in Fig. 2(d). It is found that i_{DD} maintains at about 9.3 mA in the latchup case but drops to zero in the non-latchup case. All of the device parameters used in the SPICE simulations are listed in Table 3.

From the above analysis, the transient latchup criterion can be described as:

> The p–n–p–n structure can be triggered to cause a transient latchup if and only if the product of the large-signal transient current gains (not the forward beta gains) of the parasitic n–p–n and p–n–p BJTs becomes larger than unity right after the triggering and remains larger than unity.

This criterion is general and very useful in either analytical or numerical transient latchup analyses under the triggering of various sources. In this work, the criterion will be applied in the analytical modeling of transient latchup.

3. PHYSICAL TIMING MODEL OF TRANSIENT LATCHUP

The dominant factors in the lumped equivalent circuit of a p–n–p–n structure are the base–emitter voltages $v_{EB1}(t)$ and $v_{BE2}(t)$. This is because both base and collector currents as well as the emitter junction capacitances of the BJTs $Q1$ and $Q2$ are basically functions of their base–emitter voltages. If both $v_{EB1}(t)$ and $v_{BE2}(t)$ can be found, not only each branch current or node voltage in the lumped equivalent circuit can be directly calculated by the equations

listed in Tables 1 and 2 and Appendix A, but the large-signal transient current gains $\beta_{1tr}(t)$ and $\beta_{2tr}(t)$ can also be found. Then the above proposed criterion can be used to judge whether the latchup is initiated in a p–n–p–n structure. Unfortunately, the base–emitter voltages $v_{EB1}(t)$ and $v_{BE2}(t)$ expressed in (1)–(5) are nonlinear differential equations of time. They can only be solved by intricate numerical methods.

To clearly understand the physical mechanism of transient latchup, analytical solutions of $v_{EB1}(t)$ and $v_{BE2}(t)$ are presented in this work. This can be achieved by piecewisely linearizing the BJT currents and approximating the bias-dependent junction capacitances by the averaged values within their operating voltage ranges. The piecewise linearization of intrinsic collector and emitter currents of BJTs are derived in Appendix B, whereas the averaged junction capacitances are derived and listed in Table 7. By using the method of piecewise linearization in Appendix B, the intrinsic base and collector currents can be expressed as linear functions of their base–emitter voltages when the base–emitter voltages are greater than their corresponding turn-on voltage V_{EB1on} and

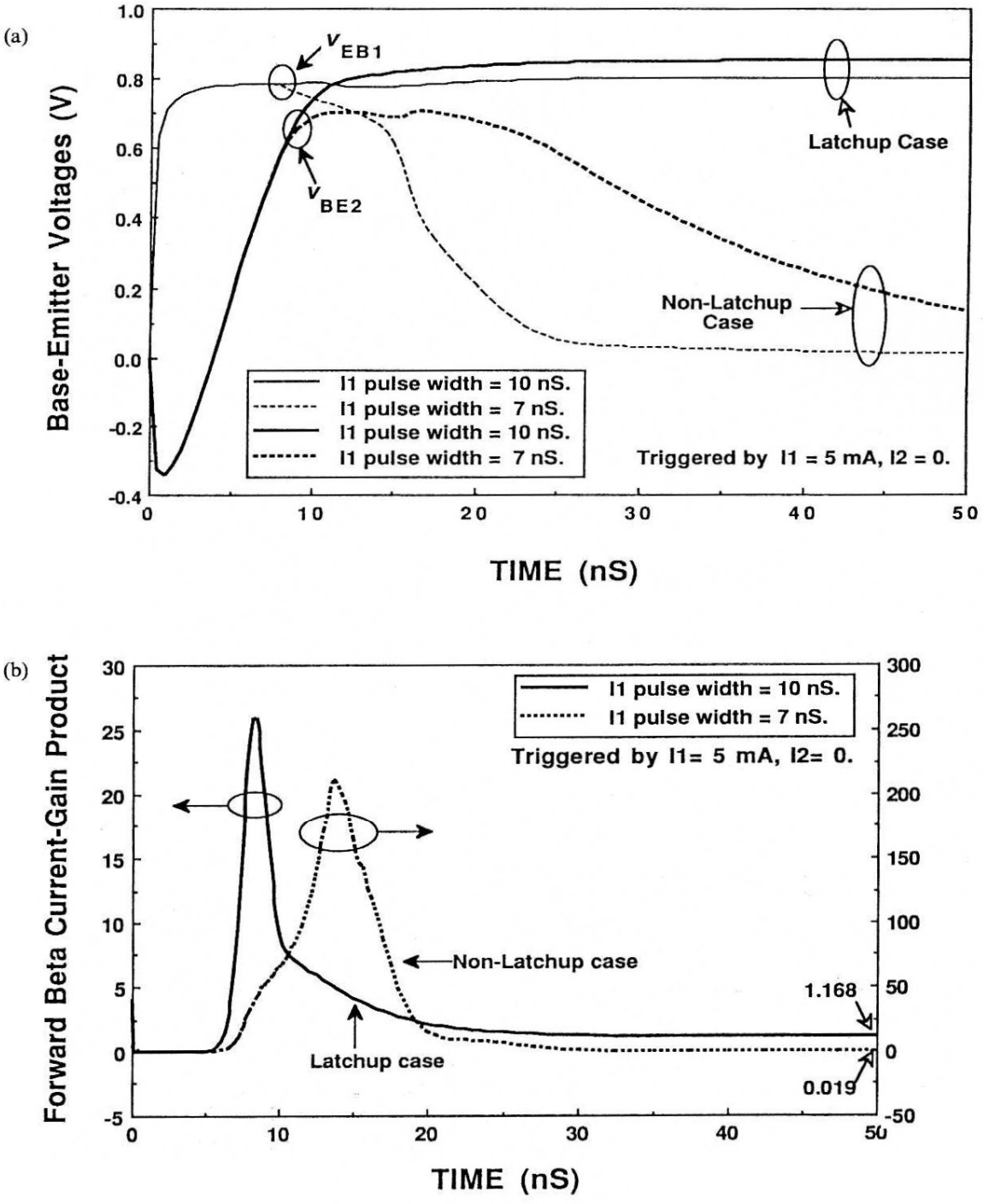

Fig. 2(a, b). *Caption overleaf.*

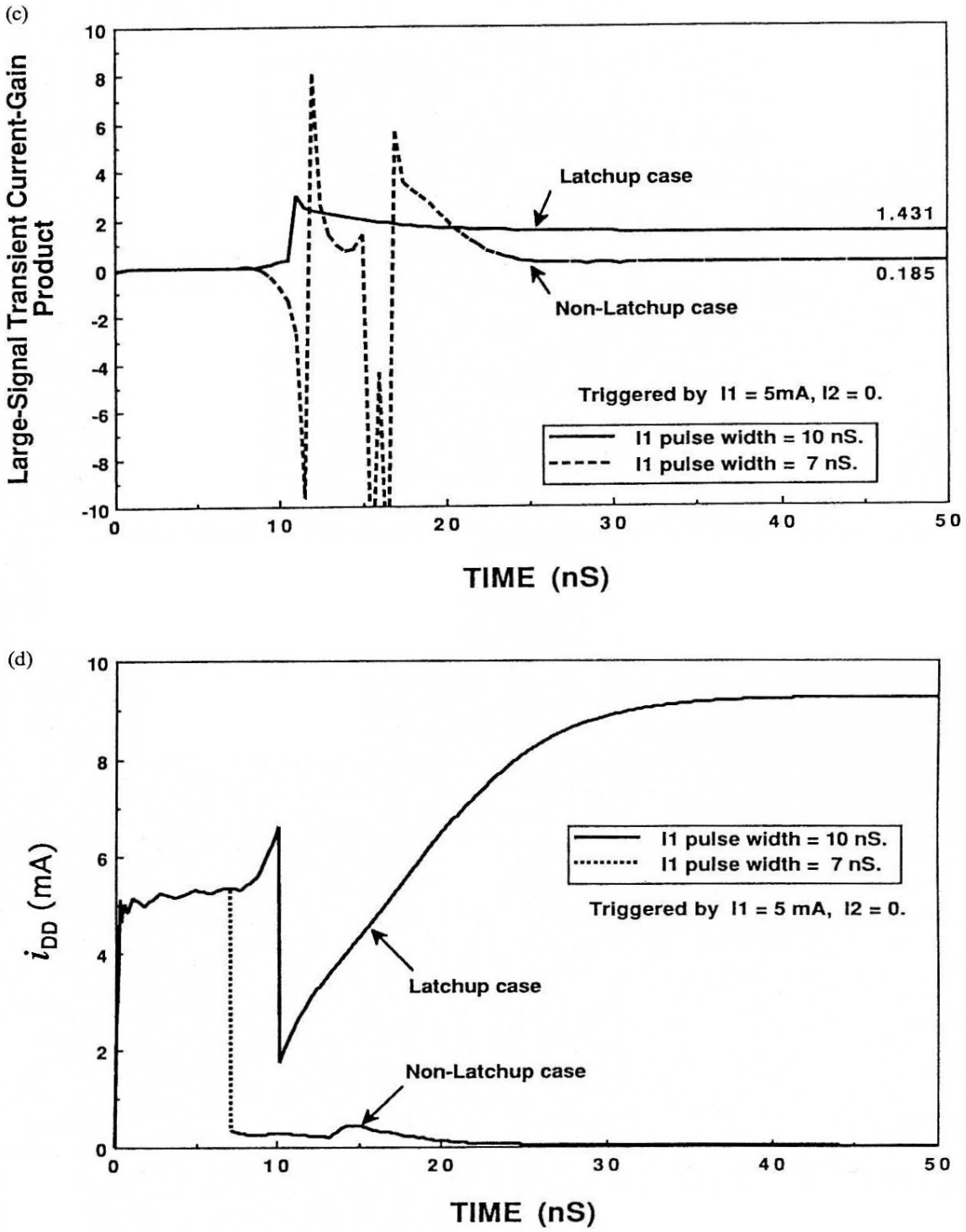

Fig. 2. (a) The typical SPICE simulated $v_{EB1}(t)$ and $v_{BE2}(t)$ waveforms of the p–n–p–n structure with $Rs = 800\,\Omega$ and $Rw = 5.6\,k\Omega$ in both latchup and non-latchup cases; (b) the product of the forward beta gains as a function of time in latchup (solid line) and non-latchup (dashed line) cases corresponding to the curves in (a); (c) the product of large-signal transient current gains as a function of time in latchup (solid line) and non-latchup (dashed line) cases as derived from the curves in (a); (d) the i_{DD} waveform as a function of time in latchup (solid line) and non-latchup (dashed line) cases corresponding to those in (a).

V_{BE2on}. The intrinsic base and collector currents are set to zero when the base–emitter voltages are less than their turn-on voltages.

3.1. *The four operating modes of a p–n–p–n structure*

Based upon the ON and OFF operations of the BJTs $Q1$ and $Q2$, there are four operating modes in the lumped equivalent circuit of a p–n–p–n structure during latchup transition. The BJTs $Q1$ and $Q2$ are initially in their OFF states before the external trigger sources are applied. When the external trigger sources which are the pulse-type current sources I_1 and I_2 are applied to the structure, the BJTs $Q1$ and $Q2$ first remain off and the junction capacitances are charged

Table 3. Device parameters of the parasitic BJTs in a p–n–p–n structure used in the theoretical calculations

Parameter	$Q_1(p$–n–$p)$ Lateral BJT	$Q_2(n$–p–$n)$ Vertical BJT
β_F	1.104	277.2
β_R	0.2	2.0
I_S(A)	2.833E − 16	8.112E − 16
I_{KF}(A)	6.909E − 5	4.867E − 4
I_{SE}(A)	4.250E − 14	1.217E − 13
τ_F(nS)	20	0.25
τ_R(nS)	10	2.0
C_{jc0}(pF)	2.0	0.6
C_{je0}(pF)	0.6	1.3

by the external trigger sources so that the base–emitter voltages arise as functions of time. When the base–emitter voltage $v_{EB1}(t)$ [or $v_{BE2}(t)$] raises up to be greater than its turn-on voltage, $Q1$ (or $Q2$) is driven into its ON state and the circuit operation is changed to the next mode. Due to the different turn-on speed of $Q1$ and $Q2$, the circuit has two different operation modes in which $Q1$ is first turned on with $Q2$ off or $Q2$ is first turned on with $Q1$ off. Finally, with the continuous and enough supply of external trigger sources, both $Q1$ and $Q2$ can be turned on and the circuit operation is changed to the last mode. In that mode, the above developed new criterion is used to judge the occurrence of latchup, and the required minimum pulse width (time) and magnitude of the pulse-type current source I_1 or I_2 can be easily calculated. If the p–n–p–n structure remains in its latchup state after the external trigger sources die out, the latchup changes from the transient type to the static type. On the other hand, if the p–n–p–n structure gradually turns off from the transient latchup state after the external trigger sources are removed, it was called the recoverable latchup[21].

In the following subsections, $v_{EB1}(t)$ and $v_{BE2}(t)$ will be solved in the four operating modes.

3.1.1. Mode 1: (Q1 and Q2 off). In this mode, the base and collector currents are zero since the BJTs $Q1$ and $Q2$ are in their OFF states. All the bias-dependent junction capacitances are estimated by their averaged values within the operating voltage ranges. With the initial condition, $v_{EB1}(0_-)=0$ and $v_{BE2}(0_-)=0$, the solutions of $v_{EB1}(t)$ and $v_{BE2}(t)$ in the Laplace form can be solved from (1)–(5) as:

$$V_{EB1}(S) = \frac{a_{10}\cdot S + (a_{10}\cdot b_{11} + b_{10}\cdot a_{12})}{S\cdot[S^2 + (a_{11}+b_{11})\cdot S + (a_{11}\cdot b_{11} - a_{12}\cdot b_{12})]} \tag{11}$$

$$V_{BE2}(S) = \frac{b_{10}\cdot S + (b_{10}\cdot a_{11} + a_{10}\cdot b_{12})}{S\cdot[S^2 + (a_{11}+b_{11})\cdot S + (a_{11}\cdot b_{11} - a_{12}\cdot b_{12})]}. \tag{12}$$

Then their time-domain solutions can be expressed as two-pole functions of time as:

$$v_{EB1}(t) = A_{10} + A_{11}\cdot e^{-(p_{11}\cdot t)} + A_{12}\cdot e^{-(p_{12}\cdot t)} \tag{13}$$

$$v_{BE2}(t) = B_{10} + B_{11}\cdot e^{-(p_{11}\cdot t)} + B_{12}\cdot e^{-(p_{12}\cdot t)}. \tag{14}$$

All the coefficients (a_{1j}, b_{1j}, A_{1j}, and B_{1j}) and the poles (p_{1j}) ($j=0, 1, 2$) in the above equations can be derived in terms of substrate and well resistances, junction capacitances, and the magnitudes of trigger sources (I_1 and I_2). The results are listed in Table 4. In this mode, the p–n–p–n structure has two negative real poles and the base–emitter voltages raise up as time increases. The transistor $Q1$ ($Q2$) will be turned on when its base–emitter voltage raises up to its turn-on voltage V_{EB1on} (V_{BE2on}) which can be calculated by using (B9) in Appendix B. The required time period t_{1a} (t_{1b}) to turn on the transistor $Q1$ ($Q2$) can be solved from (13) and (14) as:

$$A_{10} + A_{11}\cdot e^{-(p_{11}\cdot t_{1a})} + A_{12}\cdot e^{-(p_{12}\cdot t_{1a})} = V_{EB1on} \tag{15}$$

$$B_{10} + B_{11}\cdot e^{-(p_{11}\cdot t_{1b})} + B_{12}\cdot e^{-(p_{12}\cdot t_{1b})} = V_{BE2on}. \tag{16}$$

Note that the t_{1a} and t_{1b} can be easily solved from (15) and (16) without complicated numerical methods or steps.

The turn-on speed of $Q1$ and $Q2$ can be judged by the solved time variables t_{1a} and t_{1b}. If $t_{1a} < t_{1b}$, $Q1$ will turn on before $Q2$ and the circuit operation enters into the mode 2 when time increases to t_{1a}. On the contrary, $Q2$ will first turn on if $t_{1a} > t_{1b}$ and it enters into the mode 3 when time increases to t_{1b}. The base–emitter voltages in this mode at the time t_{1a} or t_{1b} are the initial conditions of the next mode and they can be calculated from (13) and (14) with the solved t_{1a} and t_{1b}. The initial conditions of the next mode can be summarized as:

$$v_{EB1}(t_{1a}) = V_{EB1on} \tag{17}$$

$$v_{BE2}(t_{1a}) = B_{10} + B_{11}\cdot e^{-(p_{11}\cdot t_{1a})} + B_{12}\cdot e^{-(p_{12}\cdot t_{1a})} \tag{18}$$

for the mode 2, and

$$v_{EB1}(t_{1b}) = A_{10} + A_{11}\cdot e^{-(p_{11}\cdot t_{1b})} + A_{12}\cdot e^{-(p_{12}\cdot t_{1b})} \tag{19}$$

$$v_{BE2}(t_{1b}) = V_{BE2on} \tag{20}$$

for the mode 3.

3.1.2. Mode 2: (Q1 on but Q2 off). In this mode, the base and collector currents of $Q2$ are still nearly zero, but those of $Q1$ are the linearized functions of its base–emitter voltage. The junction capacitances are averaged over their operating voltage ranges. With the initial conditions of base–emitter voltages in this mode given in (17) and (18), the solutions of $v_{EB1}(t)$ and $v_{BE2}(t)$ in the Laplace form are:

$$V_{EB1}(S) = \frac{S^2\cdot v_{EB1}(t_{1a}) + S\cdot[b_{21}\cdot v_{EB1}(t_{1a}) + a_{22}\cdot v_{BE2}(t_{1a}) + a_{20}] + (a_{20}\cdot b_{21} + a_{22}\cdot b_{20})}{S\cdot[S^2 + (a_{21}+b_{21})\cdot S + (a_{21}\cdot b_{21} - a_{22}\cdot b_{22})]} \tag{21}$$

$$V_{BE2}(S) = \frac{S^2\cdot v_{BE2}(t_{1a}) + S\cdot[a_{21}\cdot v_{BE2}(t_{1a}) + b_{22}\cdot v_{EB1}(t_{1a}) + b_{20}] + (b_{20}\cdot a_{21} + b_{22}\cdot a_{20})}{S\cdot[S^2 + (a_{21}+b_{21})\cdot S + (a_{21}\cdot b_{21} - a_{22}\cdot b_{22})]}. \tag{22}$$

Table 4. The coefficients in the four operation modes of the equivalent circuit in Fig. 1(b)

Mode 1:

$$p_{11}=\frac{(a_{11}+b_{11})-[(a_{11}-b_{11})^2+4\cdot a_{12}\cdot b_{12}]^{0.5}}{2}$$

$$p_{12}=\frac{(a_{11}+b_{11})+[(a_{11}-b_{11})^2+4\cdot a_{12}\cdot b_{12}]^{0.5}}{2}$$

and

$$A_{10}=\frac{a_{10}\cdot b_{11}+b_{10}\cdot a_{12}}{a_{11}\cdot b_{11}-a_{12}\cdot b_{12}}$$

$$A_{11}=\frac{a_{10}\cdot p_{11}-(a_{10}\cdot b_{11}+b_{10}\cdot a_{12})}{p_{11}\cdot(p_{12}-p_{11})}$$

$$A_{12}=\frac{a_{10}\cdot p_{12}-(a_{10}\cdot b_{11}+b_{10}\cdot a_{12})}{p_{12}\cdot(p_{11}-p_{12})}$$

$$B_{10}=\frac{b_{10}\cdot a_{11}+a_{10}\cdot b_{12}}{a_{11}\cdot b_{11}-a_{12}\cdot b_{12}}$$

$$B_{11}=\frac{b_{10}\cdot p_{11}-(b_{10}\cdot a_{11}+a_{10}\cdot b_{12})}{p_{11}\cdot(p_{12}-p_{11})}$$

$$B_{12}=\frac{b_{10}\cdot p_{12}-(b_{10}\cdot a_{11}+a_{10}\cdot b_{12})}{p_{12}\cdot(p_{11}-p_{12})}$$

where

$$a_{12}=\frac{Cc1+Cc2}{\Delta_C\cdot Rw}$$

$$a_{11}=\frac{Cc1+Cc2+Ce2}{\Delta_C\cdot Rs}$$

$$a_{10}=\frac{(Cc1+Cc2+Ce2)\cdot I_1-(Cc1+Cc2)\cdot I_2}{\Delta_C}$$

$$b_{12}=\frac{Cc1+Cc2}{\Delta_C\cdot Rs}$$

$$b_{11}=\frac{Cc1+Cc2+Ce1}{\Delta_C\cdot Rw}$$

$$b_{10}=\frac{(Cc1+Cc2+Ce1)\cdot I_2-(Cc1+Cc2)\cdot I_1}{\Delta_C}$$

Mode 2:

$$p_{21}=\frac{(a_{21}+b_{21})-[(a_{21}-b_{21})^2+4\cdot a_{22}\cdot b_{22}]^{0.5}}{2}$$

$$p_{22}=\frac{(a_{21}+b_{21})+[(a_{21}-b_{21})^2+4\cdot a_{22}\cdot b_{22}]^{0.5}}{2}$$

and

$$A_{20}=\frac{a_{20}\cdot b_{21}+b_{20}\cdot a_{22}}{a_{21}\cdot b_{21}-a_{22}\cdot b_{22}}$$

$$A_{21}=\frac{1}{p_{21}\cdot(p_{21}-p_{22})}\cdot\{(p_{21})^2\cdot v_{EB1}(t_{1a})-p_{21}\cdot[b_{21}\cdot v_{EB1}(t_{1a})+a_{22}\cdot v_{BE2}(t_{1a})+a_{20}]+(a_{20}\cdot b_{21}+b_{20}\cdot a_{22})\}$$

$$A_{22}=\frac{1}{p_{22}\cdot(p_{22}-p_{21})}\cdot\{(p_{22})^2\cdot v_{EB1}(t_{1a})-p_{22}\cdot[b_{21}\cdot v_{EB1}(t_{1a})+a_{22}\cdot v_{BE2}(t_{1a})+a_{20}]+(a_{20}\cdot b_{21}+b_{20}\cdot a_{22})\}$$

$$B_{20}=\frac{b_{20}\cdot a_{21}+a_{20}\cdot b_{22}}{a_{21}\cdot b_{21}-a_{22}\cdot b_{22}}$$

$$B_{21}=\frac{1}{p_{21}\cdot(p_{21}-p_{22})}\cdot\{(p_{21})^2\cdot v_{BE2}(t_{1a})-p_{21}\cdot[a_{21}\cdot v_{BE2}(t_{1a})+b_{22}\cdot v_{EB1}(t_{1a})+b_{20}]+(b_{20}\cdot a_{21}+a_{20}\cdot b_{22})\}$$

$$B_{22}=\frac{1}{p_{22}\cdot(p_{22}-p_{21})}\cdot\{(p_{22})^2\cdot v_{BE2}(t_{1a})-p_{22}\cdot[a_{21}\cdot v_{BE2}(t_{1a})+b_{22}\cdot v_{EB1}(t_{1a})+b_{20}]+(b_{20}\cdot a_{21}+a_{20}\cdot b_{22})\}$$

where

$$a_{22}=\frac{Cc1+Cc2}{\Delta_C\cdot Rw}$$

$$a_{21}=\frac{1}{\Delta_C}\cdot[(Cc1+Cc2+Ce2)\cdot(g_{B1}+1/Rs)+(Cc1+Cc2)\cdot g_{C1}]$$

$$a_{20}=\frac{1}{\Delta_C}\cdot[(Cc1+Cc2+Ce2)\cdot(I_1-I_{B10})-(Cc1+Cc2)\cdot(I_2+I_{C10})]$$

$$b_{22}=\frac{1}{\Delta_C}\cdot[(Cc1+Cc2+Ce1)\cdot g_{C1}+(Cc1+Cc2)\cdot(g_{B1}+1/Rs)]$$

$$b_{21}=\frac{Cc1+Cc2+Ce1}{\Delta_C\cdot Rw}$$

$$b_{20}=\frac{1}{\Delta_C}\cdot[(Cc1+Cc2+Ce1)\cdot(I_2+I_{C10})-(Cc1+Cc2)\cdot(I_1-I_{B10})]$$

continued

Table 4—*continued*

Mode 3:

$$p_{31}=\frac{(a_{31}+b_{31})-[(a_{31}-b_{31})^2+4\cdot a_{32}\cdot b_{32}]^{0.5}}{2}$$

$$p_{32}=\frac{(a_{31}+b_{31})+[(a_{31}-b_{31})^2+4\cdot a_{32}\cdot b_{32}]^{0.5}}{2}$$

and

$$A_{30}=\frac{a_{30}\cdot b_{31}+b_{30}\cdot a_{32}}{a_{31}\cdot b_{31}-a_{32}\cdot b_{32}}$$

$$A_{31}=\frac{1}{p_{31}\cdot(p_{31}-p_{32})}\cdot\{(p_{31})^2\cdot v_{EB1}(t_{1b})-p_{31}\cdot[b_{31}\cdot v_{EB1}(t_{1b})+a_{32}\cdot v_{BE2}(t_{1b})+a_{30}]+(a_{30}\cdot b_{31}+b_{30}\cdot a_{32})\}$$

$$A_{32}=\frac{1}{p_{32}\cdot(p_{32}-p_{31})}\cdot\{(p_{32})^2\cdot v_{EB1}(t_{1b})-p_{32}\cdot[b_{31}\cdot v_{EB1}(t_{1b})+a_{32}\cdot v_{BE2}(t_{1b})+a_{30}]+(a_{30}\cdot b_{31}+b_{30}\cdot a_{32})\}$$

$$B_{30}=\frac{b_{30}\cdot a_{31}+a_{30}\cdot b_{32}}{a_{31}\cdot b_{31}-a_{32}\cdot b_{32}}$$

$$B_{31}=\frac{1}{p_{31}\cdot(p_{31}-p_{32})}\cdot\{(p_{31})^2\cdot v_{BE2}(t_{1b})-p_{31}\cdot[a_{31}\cdot v_{BE2}(t_{1b})+b_{32}\cdot v_{EB1}(t_{1b})+b_{30}]+(b_{30}\cdot a_{31}+a_{30}\cdot b_{32})\}$$

$$B_{32}=\frac{1}{p_{32}\cdot(p_{32}-p_{31})}\cdot\{(p_{32})^2\cdot v_{BE2}(t_{1b})-p_{32}\cdot[a_{31}\cdot v_{BE2}(t_{1b})+b_{32}\cdot v_{EB1}(t_{1b})+b_{30}]+(b_{30}\cdot a_{31}+a_{30}\cdot b_{32})\}$$

where

$$a_{32}=\frac{1}{\Delta_C}\cdot[(Cc1+Cc2+Ce2)\cdot g_{C2}+(Cc1+Cc2)\cdot(g_{B2}+1/Rw)]$$

$$a_{31}=\frac{Cc1+Cc2+Ce2}{\Delta_C\cdot Rs}$$

$$a_{30}=\frac{1}{\Delta_C}\cdot[(Cc1+Cc2+Ce2)\cdot(I_1+I_{C20})-(Cc1+Cc2)\cdot(I_2-I_{B20})]$$

$$b_{32}=\frac{Cc1+Cc2}{\Delta_C\cdot Rs}$$

$$b_{31}=\frac{1}{\Delta_C}\cdot[(Cc1+Cc2+Ce1)\cdot(g_{B2}+1/Rw)+(Cc1+Cc2)\cdot g_{C2}]$$

$$b_{30}=\frac{1}{\Delta_C}\cdot[(Cc1+Cc2+Ce1)\cdot(I_2-I_{B20})-(Cc1+Cc2)\cdot(I_1+I_{C20})]$$

Mode 4:

$$p_{41}=\frac{(a_{41}+b_{41})-[(a_{41}-b_{41})^2+4\cdot a_{42}\cdot b_{42}]^{0.5}}{2}$$

$$p_{42}=\frac{(a_{41}+b_{41})+[(a_{41}-b_{41})^2+4\cdot a_{42}\cdot b_{42}]^{0.5}}{2}$$

and

$$A_{40}=\frac{a_{40}\cdot b_{41}+b_{40}\cdot a_{42}}{a_{41}\cdot b_{41}-a_{42}\cdot b_{42}}$$

$$A_{41}=\frac{1}{p_{41}\cdot(p_{41}-p_{42})}\cdot\{(p_{41})^2\cdot v_{EB1}(t_2)-p_{41}\cdot[b_{41}\cdot v_{EB1}(t_2)+a_{42}\cdot v_{BE2}(t_2)+a_{40}]+(a_{40}\cdot b_{41}+b_{40}\cdot a_{42})\}$$

$$A_{42}=\frac{1}{p_{42}\cdot(p_{42}-p_{41})}\cdot\{(p_{42})^2\cdot v_{EB1}(t_2)-p_{42}\cdot[b_{41}\cdot v_{EB1}(t_2)+a_{42}\cdot v_{BE2}(t_2)+a_{40}]+(a_{40}\cdot b_{41}+b_{40}\cdot a_{42})\}$$

$$B_{40}=\frac{b_{40}\cdot a_{41}+a_{40}\cdot b_{42}}{a_{41}\cdot b_{41}-a_{42}\cdot b_{42}}$$

$$B_{41}=\frac{1}{p_{41}\cdot(p_{41}-p_{42})}\cdot\{(p_{41})^2\cdot v_{BE2}(t_2)-p_{41}\cdot[a_{41}\cdot v_{BE2}(t_2)+b_{42}\cdot v_{EB1}(t_2)+b_{40}]+(b_{40}\cdot a_{41}+a_{40}\cdot b_{42})\}$$

$$B_{42}=\frac{1}{p_{42}\cdot(p_{42}-p_{41})}\cdot\{(p_{42})^2\cdot v_{BE2}(t_2)-p_{42}\cdot[a_{41}\cdot v_{BE2}(t_2)+b_{42}\cdot v_{EB1}(t_2)+b_{40}]+(b_{40}\cdot a_{41}+a_{40}\cdot b_{42})\}$$

where

$$a_{42}=\frac{1}{\Delta_C}\cdot[(Cc1+Cc2+Ce2)\cdot g_{C2}+(Cc1+Cc2)\cdot(g_{B2}+1/Rw)]$$

$$a_{41}=\frac{1}{\Delta_C}\cdot[(Cc1+Cc2+Ce2)\cdot(g_{B1}+1/Rs)+(Cc1+Cc2)\cdot g_{C1}]$$

$$a_{40}=\frac{1}{\Delta_C}\cdot[(Cc1+Cc2+Ce2)\cdot(I_1+I_{C20}-I_{B10})-(Cc1+Cc2)\cdot(I_2+I_{C10}-I_{B20})]$$

$$b_{42}=\frac{1}{\Delta_C}\cdot[(Cc1+Cc2+Ce1)\cdot g_{C1}+(Cc1+Cc2)\cdot(g_{B1}+1/Rs)]$$

$$b_{41}=\frac{1}{\Delta_C}\cdot[(Cc1+Cc2+Ce1)\cdot(g_{B2}+1/Rw)+(Cc1+Cc2)\cdot g_{C2}]$$

$$b_{40}=\frac{1}{\Delta_C}\cdot[(Cc1+Cc2+Ce1)\cdot(I_2+I_{C10}-I_{B20})-(Cc1+Cc2)\cdot(I_1+I_{C20}-I_{B10})]$$

The corresponding time-domain solutions are:

$$v_{EB1}(t) = A_{20} + A_{21} \cdot e^{-(p_{21} \cdot t)} + A_{22} \cdot e^{-(p_{22} \cdot t)} \quad (23)$$

$$v_{BE2}(t) = B_{20} + B_{21} \cdot e^{-(p_{21} \cdot t)} + B_{22} \cdot e^{-(p_{22} \cdot t)}. \quad (24)$$

The coefficients and the poles in (21)–(24) are also listed in Table 4. With the negative real poles $-p_{21}$ and $-p_{22}$, these base–emitter voltages also monotonically increase as time increases. The required time period t_{2b} to turn on $Q2$ can be easily obtained by solving the following equation:

$$B_{20} + B_{21} \cdot e^{-(p_{21} \cdot t_{2b})} + B_{22} \cdot e^{-(p_{22} \cdot t_{2b})} = V_{BE2on}. \quad (25)$$

When $Q2$ is turned on after $Q1$, the circuit operation enters into the mode 4. The base–emitter voltages in this mode at the time t_{2b} are the initial conditions of the mode 4 and they are:

$$v_{EB1}(t_{2b}) = A_{20} + A_{21} \cdot e^{-(p_{21} \cdot t_{2b})} + A_{22} \cdot e^{-(p_{22} \cdot t_{2b})} \quad (26)$$

$$v_{BE2}(t_{2b}) = V_{BE2on}. \quad (27)$$

3.1.3. Mode 3: (Q2 on but Q1 off). Similar to the mode 2, the base and collector currents of $Q1$ in this mode are still zero, but those of $Q2$ are the linearized functions of its base–emitter voltage. The $v_{EB1}(t)$ and $v_{BE2}(t)$ can be similarly solved with their coefficients and poles listed in Table 4. The required time period t_{2a} to turn on $Q1$ can be easily obtained. The initial conditions for the mode 4 can be determined similarly as those in the mode 2.

3.1.4. Mode 4: (Both Q1 and Q2 have been turned on). In this mode, the base and collector currents of $Q1$ and $Q2$ are the linearized functions of their base–emitter voltages. The junction capacitances are also averaged over their operating voltage ranges. To conveniently express the initial conditions, the notations $v_{EB1}(t_2)$ and $v_{BE2}(t_2)$ are used to generally represent these initial conditions from the modes 2 and 3. Then, the solutions of the base–emitter voltages in the Laplace form are:

$$V_{EB1}(S) = \frac{S^2 \cdot v_{EB1}(t_2) + S \cdot [b_{41} \cdot v_{EB1}(t_2) + a_{42} \cdot v_{BE2}(t_2) + a_{40}] + (a_{40} \cdot b_{41} + a_{42} \cdot b_{40})}{S \cdot [S^2 + (a_{41} + b_{41}) \cdot S + (a_{41} \cdot b_{41} - a_{42} \cdot b_{42})]} \quad (28)$$

$$V_{BE2}(S) = \frac{S^2 \cdot v_{BE2}(t_2) + S \cdot [a_{41} \cdot v_{BE2}(t_2) + b_{42} \cdot v_{EB1}(t_2) + b_{40}] + (b_{40} \cdot a_{41} + b_{42} \cdot a_{40})}{S \cdot [S^2 + (a_{41} + b_{41}) \cdot S + (a_{41} \cdot b_{41} - a_{42} \cdot b_{42})]}. \quad (29)$$

The corresponding time-domain solutions are:

$$v_{EB1}(t) = A_{40} + A_{41} \cdot e^{-(p_{41} \cdot t)} + A_{42} \cdot e^{-(p_{42} \cdot t)} \quad (30)$$

$$v_{BE2}(t) = B_{40} + B_{41} \cdot e^{-(p_{41} \cdot t)} + B_{42} \cdot e^{-(p_{42} \cdot t)}. \quad (31)$$

The coefficients and the poles in (28)–(31) are also listed in Table 4. The pole $-p_{42}$ is a negative real pole whereas $-p_{41}$ is a positive real pole due to the positive-feedback regeneration process in the p–n–p–n structure. It is interesting to note that only this mode of operation has a positive pole which leads to the rapid positive regeneration in both base and collector currents of $Q1$ and $Q2$, so that the p–n–p–n structure can be quickly triggered into its latchup state.

3.2. The required minimum time to initiate latchup

With the above solved $v_{EB1}(t)$ and $v_{BE2}(t)$ in each operation mode, all the node voltages and branch currents in the equivalent circuit shown in Fig. 1(b) can be calculated and the dynamic behaviors of a p–n–p–n structure as functions of time due to external currents triggering can be fully characterized. Then, the product $\beta_{1tr}(t) \cdot \beta_{2tr}(t)$ can be obtained and the physical criterion can be used to determine whether the transient latchup occurs in a p–n–p–n structure. Because either $Q1$ or $Q2$ is off in the piecewise-linearized operation modes 1–3, the latchup does not occur in these modes. The product of the large-signal transient current gains in the modes 1–3 may have a value due to the transient currents in the device capacitances but it is near zero as shown in Fig. 2(c) before the occurrence of latchup. When the circuit operation enters into the mode 4, the product of large-signal current gains arises from zero as time increases and the p–n–p–n structure becomes latchup when $\beta_{1tr}(t) \cdot \beta_{2tr}(t) = 1$. When $\beta_{1tr}(t) \cdot \beta_{2tr}(t) > 1$, the p–n–p–n structure has been in its latchup state.

Substituting the piecewisely linearized base and collector currents derived in Appendix B with the solved base–emitter voltages expressed in (30) and (31) into (8) and (9), the time equation of the product of the large-signal current gains can be obtained and the time period in the mode 4 corresponding to $\beta_{1tr}(t) \cdot \beta_{2tr}(t) = 1$ can be solved from the relation:

$$l_0 + l_1 \cdot e^{-(p_{41} \cdot t)} + l_2 \cdot e^{-(p_{42} \cdot t)} + l_3 \cdot e^{-[(p_{41} + p_{42}) \cdot t]} + l_4 \cdot e^{-(2 \cdot p_{41} \cdot t)} + l_5 \cdot e^{-(2 \cdot p_{42} \cdot t)} = 0. \quad (32)$$

The coefficients l_0–l_5 are derived in terms of device parameters of a p–n–p–n structure and the magnitudes of the external trigger current sources. The expression of l_0–l_5 are summarized in Table 5.

From the equations of the time periods in each mode, the minimum required pulse width to initiate transient latchup can be calculated. For example, if only I_1 is applied and $I_2 = 0$, the transistor $Q1$ is first turned on and then $Q2$ is turned on later. The corresponding circuit operation mode is from the mode 1, through the mode 2, and then to the mode 4. Therefore, the required minimum pulse width of I_1 to initiate latchup can be calculated as:

$$t_{min,I1} = t_{1a} + t_{2b} + t_{3a}, \quad (33)$$

Table 5. The coefficients of the equation (32)

$$l_0 = k_1 \cdot A_{40} + k_2 \cdot B_{40} + k_3 \cdot A_{40}^2 + k_4 \cdot B_{40}^2 + k_5 \cdot A_{40} \cdot B_{40}$$
$$l_1 = k_1 \cdot A_{41} + k_2 \cdot B_{41} + 2 \cdot k_3 \cdot A_{40} \cdot A_{41} + 2 \cdot k_4 \cdot B_{40} \cdot B_{41} + k_5 \cdot (A_{40} \cdot B_{41} + B_{40} \cdot A_{41})$$
$$l_2 = k_1 \cdot A_{42} + k_2 \cdot B_{42} + 2 \cdot k_3 \cdot A_{40} \cdot A_{42} + 2 \cdot k_4 \cdot B_{40} \cdot B_{42} + k_5 \cdot (A_{40} \cdot B_{42} + B_{40} \cdot A_{42})$$
$$l_3 = 2 \cdot k_3 \cdot A_{41} \cdot A_{42} + 2 \cdot k_4 \cdot B_{41} \cdot B_{42} + k_5 \cdot (A_{41} \cdot B_{42} + B_{41} \cdot A_{42})$$
$$l_4 = k_3 \cdot A_{41}^2 + k_4 \cdot B_{41}^2 + k_5 \cdot A_{41} \cdot B_{41}$$
$$l_5 = k_3 \cdot A_{42}^2 + k_4 \cdot B_{42}^2 + k_5 \cdot A_{42} \cdot B_{42}$$

where

$$k_1 = \frac{(\Delta_C - Cc1 \cdot Ce1) \cdot I_{C10} + Cc1 \cdot Ce1 \cdot I_{B20} + Cc1 \cdot Ce2 \cdot (I_{B10} - I_{C20})}{Rs}$$

$$k_2 = \frac{(\Delta_C - Cc2 \cdot Ce2) \cdot I_{C20} + Cc2 \cdot Ce2 \cdot I_{B10} + Cc2 \cdot Ce1 \cdot (I_{B20} - I_{C10})}{Rw}$$

$$k_3 = \frac{Cc1 \cdot Ce2}{Rs^2} + \frac{g_{C1} \cdot (\Delta_C - Cc1 \cdot Ce1) + g_{B1} \cdot Cc1 \cdot Ce2}{Rs}$$

$$k_4 = \frac{Cc2 \cdot Ce1}{Rw^2} + \frac{g_{C2} \cdot (\Delta_C - Cc2 \cdot Ce2) + g_{B2} \cdot Cc2 \cdot Ce1}{Rw}$$

$$k_5 = \frac{g_{B1} \cdot Cc2 \cdot Ce2 - g_{C1} \cdot Cc2 \cdot Ce1}{Rw} + \frac{g_{B2} \cdot Cc1 \cdot Ce1 - g_{C2} \cdot Cc1 \cdot Ce2}{Rs} - \frac{Cc1 \cdot Ce2 + Cc2 \cdot Ce1 + Ce1 \cdot Ce2}{Rs \cdot Rw}$$

where t_{3a} is the time period when the $\beta_{1tr}(t) \cdot \beta_{2tr}(t)$ product raises up to be equal to unity after the circuit operation enters the mode 4. The t_{3a} can be solved from (32). The time periods t_{1a} and t_{2b} have been solved in the modes 1 and 2, respectively. For I_2 triggering, similar relation of the minimum pulse width $t_{min,I2}$ as (33) to initiate latchup can be found with the circuit operation of mode 1→mode 3→mode 4.

Certainly, when both I_1 and I_2 are applied simultaneously, the required minimum pulse width to induce transient latchup can also be found similarly by using the proposed criterion and analytical timing model. Depending on the turn-on speed of each transistor, the sequence of the operation modes could be 1→2→4 or 1→3→4.

3.3. The minimum pulse height of trigger currents to induce latchup

If the applied external currents are not large enough, the p–n–p–n structure can not be turned on even though the trigger time is very long. Thus the structure can never be triggered into the latchup state. The minimum required pulse height of external trigger currents can also be found through the above described timing model.

For I_1 triggering ($I_2 = 0$), $Q2$ will be turned on after $Q1$ does and then the p–n–p–n structure could be triggered to transient latchup. If $Q2$ can not be turned on due to I_1 triggering, the latchup state will not occur. In the mode-2 operation where $Q1$ has been turned on but $Q2$ remains off, the base–emitter voltage of $Q2$ monotonically raises up to its final value with two negative poles as described in (24). If the final base–emitter voltage of $Q2$ in the mode 2 is smaller than its turn-on voltage, latchup never occurs. Thus a necessary condition for transient latchup initiation is that the final base–emitter voltage of $Q2$ in the mode 2 due to I_1 triggering must be greater than its turn-on voltage V_{BE2on}. The final base–emitter voltage of $Q2$ is the term B_{20} in (24) with I_1 triggering and $I_2 = 0$. Substituting the corresponding coefficients into B_{20}, this necessary condition can be written as:

$$B_{20} = \frac{I_{C10} \cdot (g_{B1} + 1/Rs) + g_{C1} \cdot (I_1 - I_{B10})}{(g_{B1} + 1/Rs) \cdot (1/Rw)} \geqslant V_{BE2on}. \quad (34)$$

From the above equation, the required minimum magnitude of I_1 to initiate transient latchup under $I_2 = 0$ can be written as:

$$I_{1min} = I_{B10} + \frac{(g_{B1} + 1/Rs)}{g_{C1}} \cdot \left[\frac{V_{BE2on}}{Rw} - I_{C10}\right]. \quad (35)$$

Similarly, the minimum pulse height of I_2 in the mode 3 to initiate latchup under $I_1 = 0$ can be written as:

$$I_{2min} = I_{B20} + \frac{(g_{B2} + 1/Rw)}{g_{C2}} \cdot \left[\frac{V_{EB1on}}{Rs} - I_{C20}\right]. \quad (36)$$

It can be seen from (35) and (36) that smaller Rs and Rw cause larger I_{1min} and I_{2min}. This means that a p–n–p–n structure with smaller substrate and well resistances has a higher transient latchup immunity against the substrate or well current triggering.

4. RESULTS OF MODEL CALCULATION AND DISCUSSION

4.1. Comparisons with SPICE simulation results

By using the developed new criterion and timing model, the required minimum pulse widths to initiate latchup with different pulse heights of trigger current

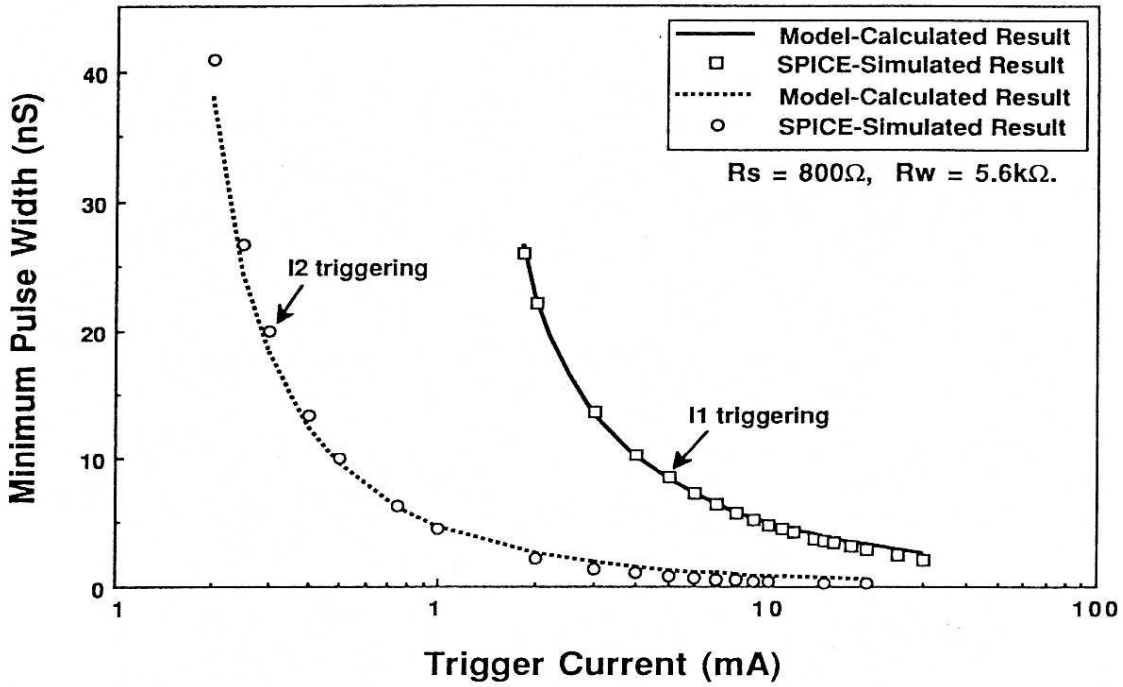

Fig. 3. The SPICE simulated and the model calculated results of the required minimum pulse width of the trigger currents to initiate latchup as functions of the pulse current heights.

I_1 and I_2 are calculated and compared to those obtained from SPICE simulations. The results are shown in Fig. 3 where the adopted device parameters of a p–n–p–n structure are listed in Table 3 with the piecewise-linearized currents in Appendix B and the averaged junction capacitances in Table 7. As can be seen from Fig. 3, good agreement is obtained between analytically calculated and SPICE simulated results. It is also found in Fig. 3 that a smaller trigger current requires a longer trigger time to induce latchup, and it never becomes latchup if the pulse width of a trigger current is smaller than the corresponding minimum values $t_{min,I1}$ (or $t_{min,I2}$) in (33).

Figure 4(a) and (b) show the variations of the minimum pulse widths $t_{min,I1}$ and $t_{min,I2}$ as functions of the substrate and the well resistances, respectively, for $I_1 = 5$ mA or $I_2 = 0.5$ mA triggering. It is noted that the decrease of the substrate or the well resistances increases the values of the required minimum pulse widths of I_1 and I_2 to initiate transient latchup so that the latchup immunity is enhanced. Good agreement is also obtained between analytically calculated and SPICE simulated results.

The effect of well-substrate junction capacitance on transient latchup is shown in Fig. 5. The minimum pulse widths of I_1 and I_2 are linearly proportional to the zero-biased well–substrate capacitance. This is also consistent with the previous results[8]. This result indicates that the larger well–substrate junction capacitance in a p–n–p–n structure leads to a higher transient latchup immunity against well and substrate currents triggering. The larger well–substrate junction capacitance can be achieved by a larger well region.

Figure 6(a) and (b) show the model calculated and SPICE simulated results of the minimum pulse widths as functions of the forward transit times τ_{F1} and τ_{F2} of the BJTs $Q1$ and $Q2$, respectively, with $I_1 = 5$ mA or $I_2 = 0.5$ mA triggering. As seen from the first equation in Table 7, the transit time has an important effect on the averaged base–emitter junction diffusion capacitance which is dominant in the total capacitance of the forward-biased base–emitter junction. A larger transit time which may be caused by a wider base width of the parasitic BJTs in a p–n–p–n structure leads to a larger minimum pulse width and thus a higher latchup immunity, as seen in Fig. 6(a,b).

The minimum pulse width as functions of the maximum forward beta gains, β_{F1} and β_{F2}, of $Q1$ and $Q2$ with $I_1 = 5$ mA or $I_2 = 0.5$ mA are shown in Fig. 7(a) and (b), respectively. As shown in these figures, the minimum pulse widths of well-triggering current I_2 and substrate-triggering current I_1 have a stronger dependence on the beta gains of $Q1$ and $Q2$ when the beta gains are smaller. But the dependence becomes less when the beta gains are large enough. Smaller beta gains increase the transient latchup immunity as expected.

From the above figures, it can be concluded that the transient latchup immunity can be effectively improved through the increase of the collector junction capacitances of the parasitic transistors. But the immunity can not be strictly improved if Rs (Rw) and β_{F1} (β_{F2}) are large enough or τ_{F1} (τ_{F2}) is small enough.

By using the proposed transient latchup criterion and the latchup timing model, the minimum magnitudes of I_1 and I_2 to induce latchup have been derived in (35) and (36), respectively. The model calculated and SPICE simulated results of I_{1min} and I_{2min} are shown in Fig. 8(a,b) with good agreements. As shown in Fig. 8(a,b), smaller substrate and well resistances

lead to larger $I_{1\min}$ and $I_{2\min}$. This means that a p–n–p–n structure with smaller substrate and well resistances has a higher transient latchup immunity as expected. The result of Fig. 8(b) also shows that the minimum magnitude of the well-triggering current I_2 applied to the base of the parasitic n–p–n BJT $Q2$ is more sensitive to well resistance (dashed line) than substrate resistance (solid line). This implies that decreasing the well resistance has a more significant efficiency on the enhancement of transient latchup immunity than decreasing the substrate resistance.

All the model calculated results with the different variations on device parameters of a p–n–p–n structure have shown good agreements to those of SPICE simulations in the above figures. These substantiate the validity of the proposed new transient latchup criterion and the timing model.

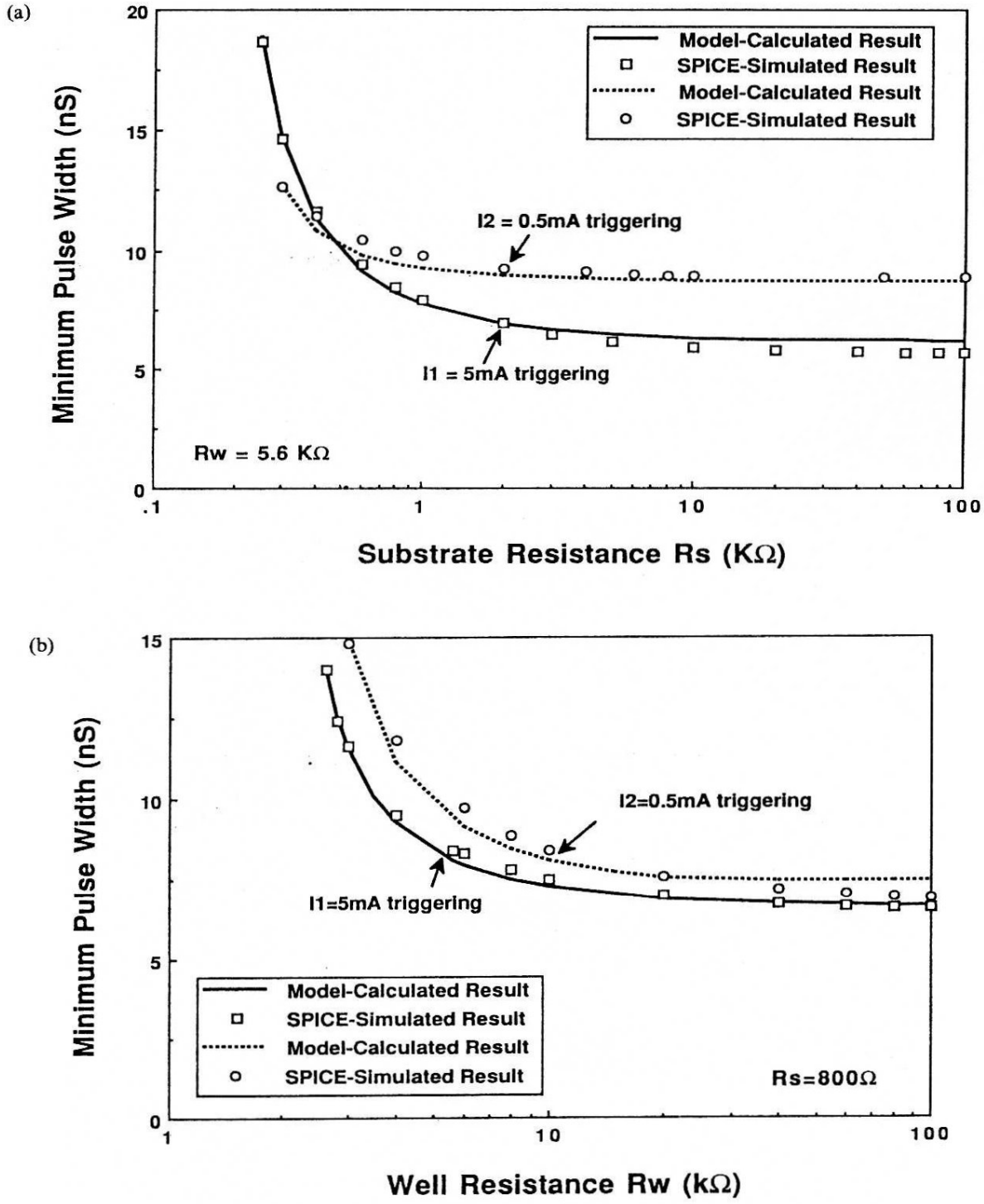

Fig. 4. The SPICE simulated and the model calculated results of the required minimum pulse widths with $I_1 = 5$ mA or $I_2 = 0.5$ mA triggering as functions of (a) the substrate resistance Rs with a fixed well resistance $Rw = 5.6$ kΩ; (b) the well resistance Rw with a fixed substrate resistance $Rs = 800\ \Omega$.

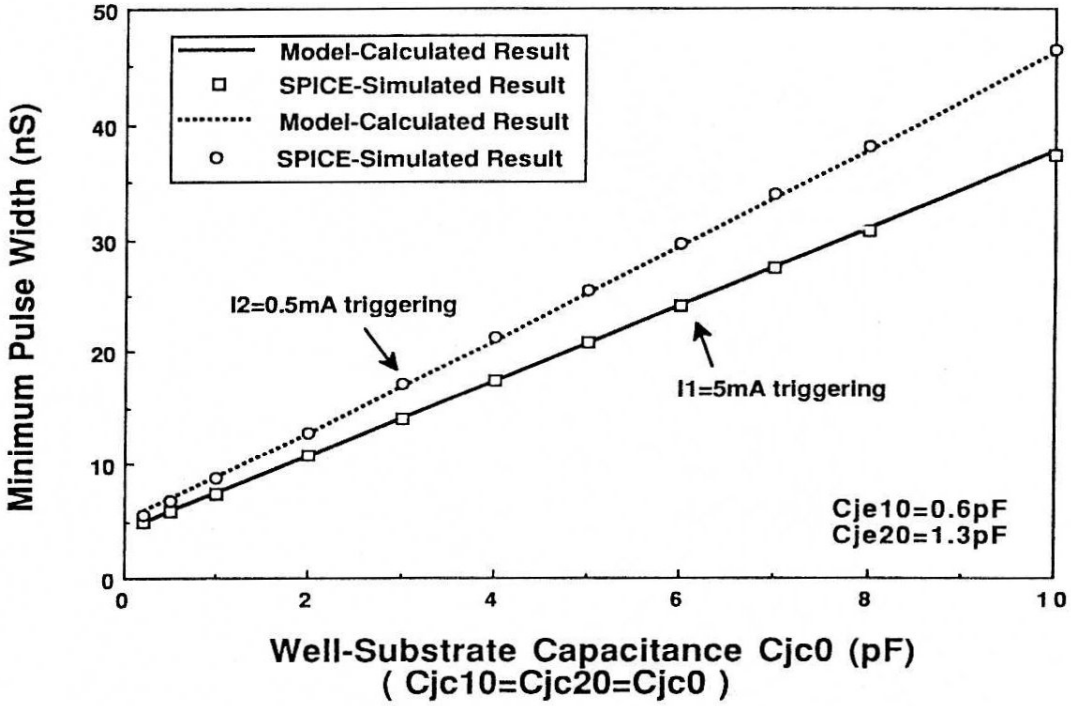

Fig. 5. The SPICE simulated and the model calculated results of the required minimum pulse widths as a function of the zero-biased well-substrate junction capacitance with $I_1 = 5$ mA or $I_2 = 0.5$ mA triggering.

4.2. *Comparisons with experimental results*

To experimentally investigate the dynamic triggering characteristics of transient latchup and verify the developed criterion and model, a p–n–p–n structure with the anode-to-cathode spacing of 35 μm has been fabricated by using a 0.8 μm twin-well n-substrate bulk CMOS technology and measured. The d.c. triggering voltage (current) of the fabricated p–n–p–n structure is 29.8 V (3.06 mA) and the holding voltage (current) is 1.2 V (4.54 mA). The device parameters of both parasitic lateral p–n–p and the vertical n–p–n BJTs in this experimental test structure has been extracted and listed in Table 6. Although the parasitic vertical n–p–n BJT $Q2$ has a β_{F2} as high as 322, its knee current I_{KF} for high-level injection[17–20] is only 0.226 mA which is much smaller than that of a normal BJT.

Figure 9 shows the model calculated and experimentally measured results of the minimum pulse

(a)

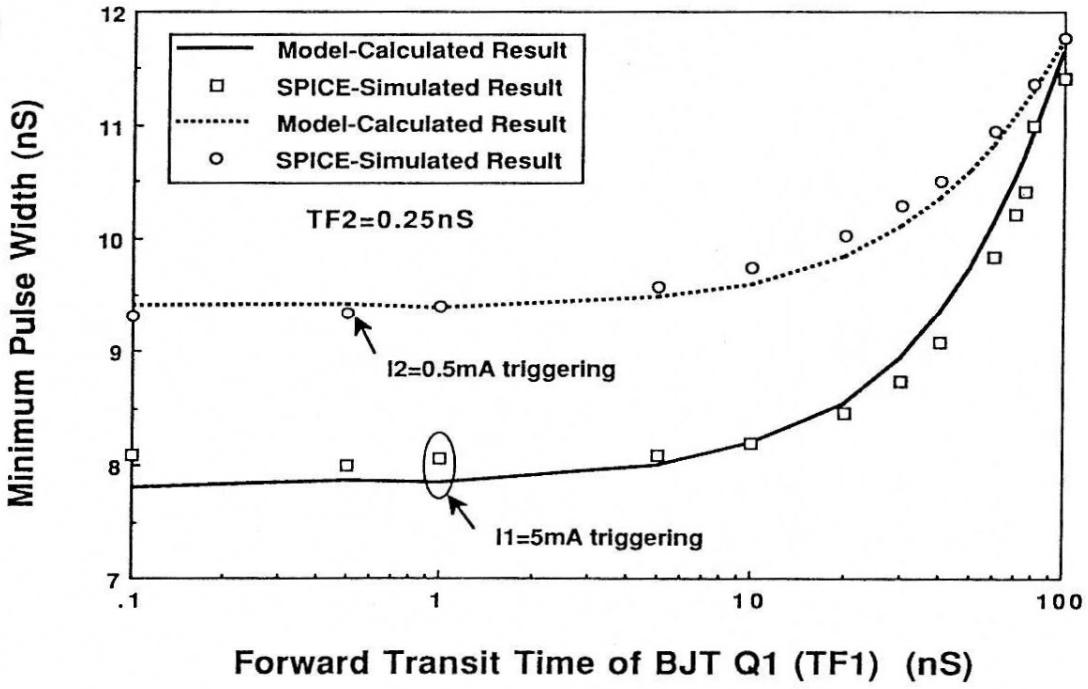

Fig. 6(a). *Caption on facing page.*

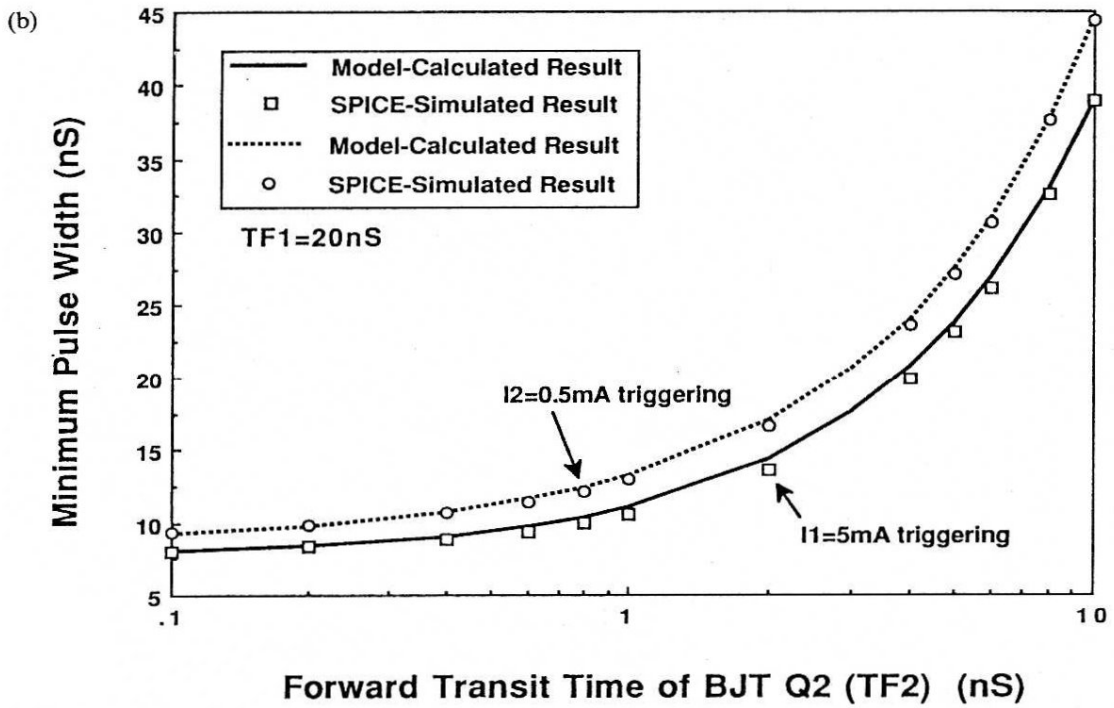

Fig. 6. The SPICE simulated and the model calculated results of the required minimum pulse widths with $I_1 = 5$ mA or $I_2 = 0.5$ mA triggering, $Rs = 800\ \Omega$, and $Rw = 5.6\ \text{k}\Omega$ as functions of (a) the forward transit time of the BJT $Q1$ with a fixed 0.25-nS forward transit time of the BJT $Q2$; (b) the forward transit time of the BJT $Q2$ with a fixed 20-nS forward transit time of the BJT $Q1$.

widths as functions of the pulse heights of I_1 and I_2. It is shown that good agreement is obtained between calculated and measured results. This also verifies the exactness of the proposed new physical transient latchup criterion and the timing model.

5. CONCLUSION

A new general and physical criterion for transient latchup has been developed. It is based upon the product of large-signal transient current gains of the parasitic lateral and vertical BJTs in the p–n–p–n

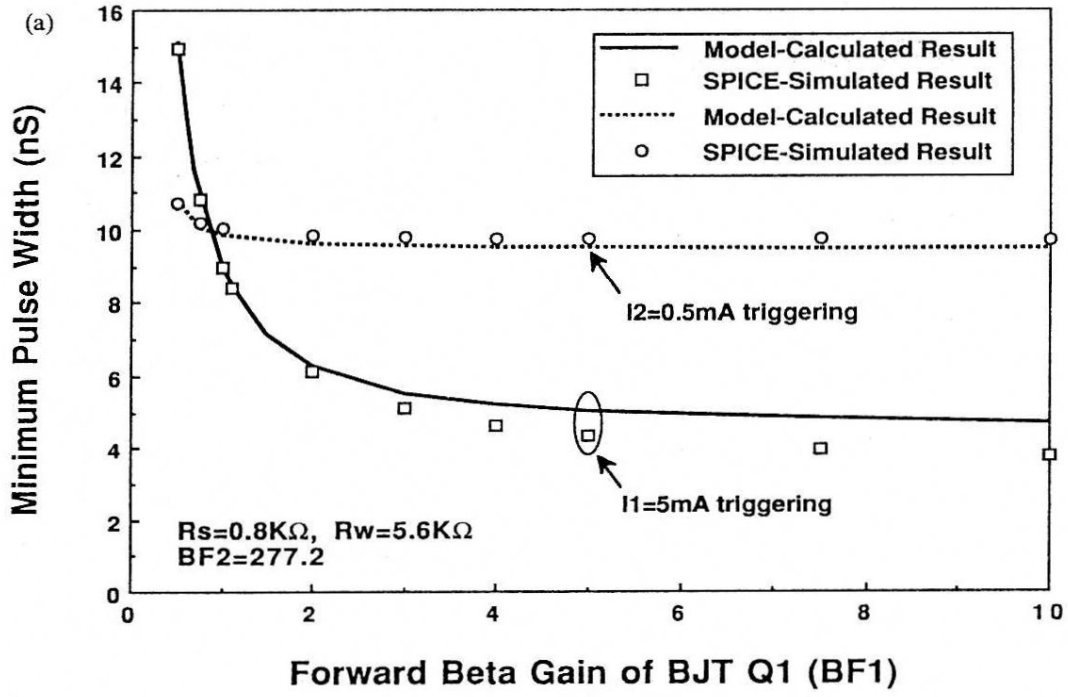

Fig. 7(a). *Caption overleaf.*

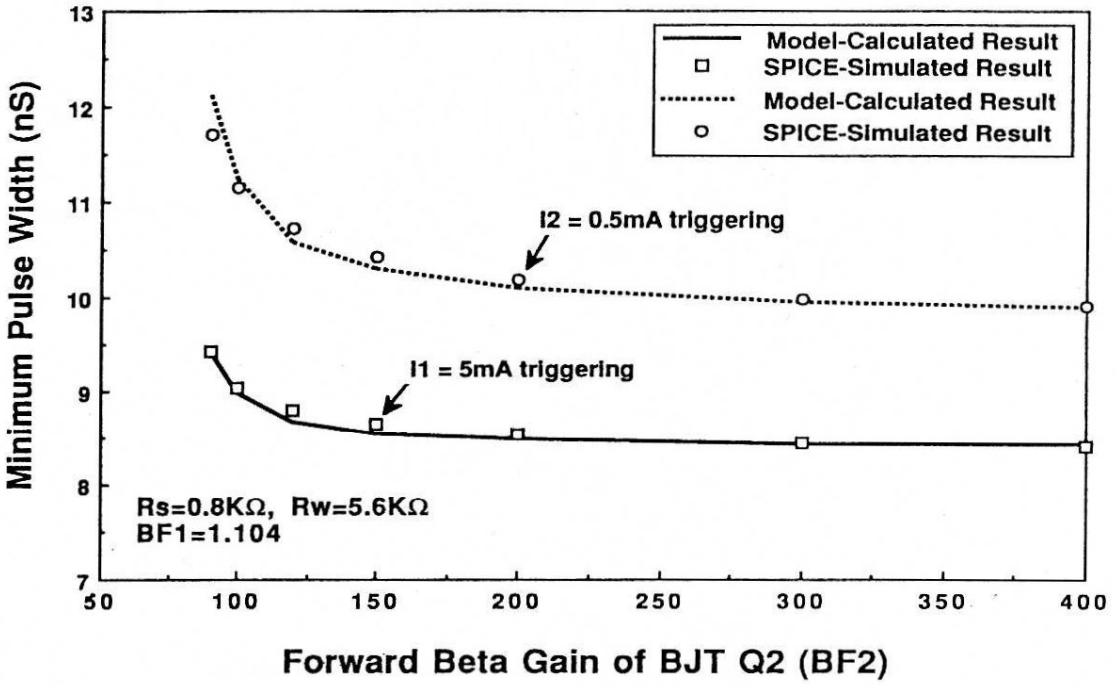

Fig. 7. The SPICE simulated and the model calculated results of the required minimum pulse widths with $I_1 = 5$ mA or $I_2 = 0.5$ mA triggering, $Rs = 800\ \Omega$, and $Rw = 5.6\ \text{k}\Omega$ as functions of (a) the forward beta gain of the BJT $Q1$ with a fixed $\beta_{F2} = 277.2$ forward beta gain of the BJT $Q2$; (b) the forward beta gain of the BJT $Q2$ with a fixed $\beta_{F1} = 1.104$ forward beta gain of the BJT $Q1$.

structure. The large-signal transient current gain is a new parameter which describes the transient current gain of a BJT, taking all the transient currents of the device capacitances into consideration. As the product of the large-signal transient current gains is equal to or greater than unity right after triggering, transient latchup occurs. Using the developed criterion and the derived analytical timing model with properly linearized equations, the required minimum pulse width for transient latchup as functions of the pulse heights of the well-triggering or the substrate-triggering currents can be calculated analytically.

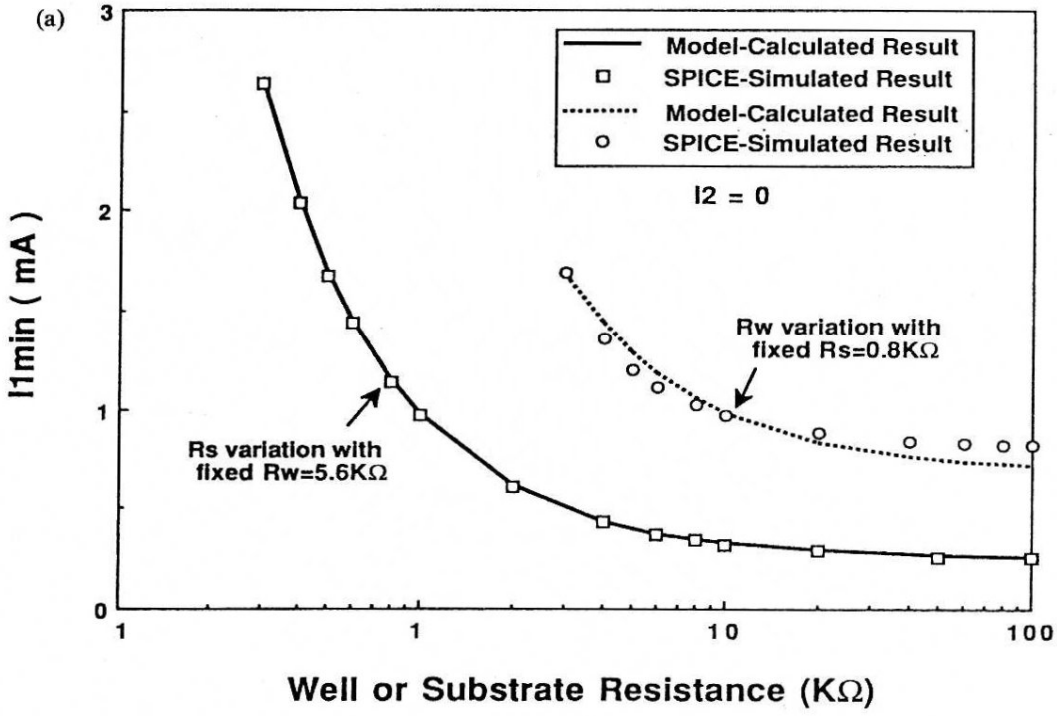

Fig. 8(a). *Caption on facing page.*

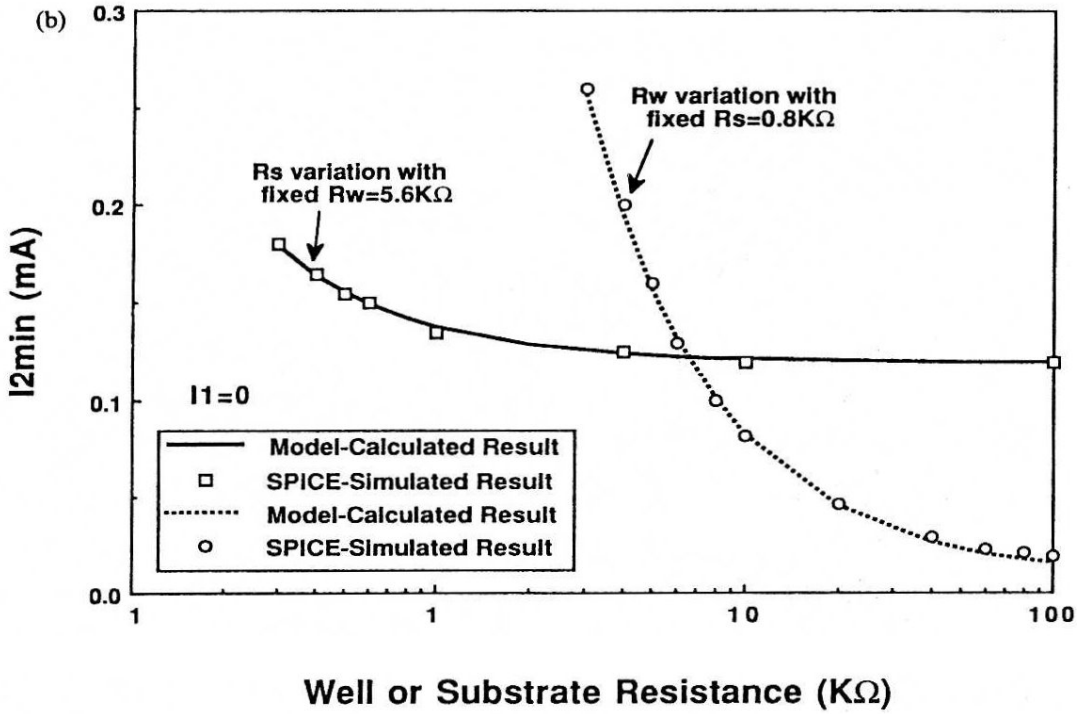

Fig. 8. The SPICE simulated and the model calculated results of the minimum trigger currents (a) $I_{1\min}$, or (b) $I_{2\min}$, to induce latchup as functions of the parasitic resistances *Rs* or *Rw*.

Both SPICE simulated and experimental results show good agreements to the model calculated results, which substantiate the validity of the proposed new criterion. It can be shown from the above results that larger forward transient times, larger well–substrate junction capacitance, smaller well and substrate resistances, smaller forward beta gains, and significant high-level injection effect of the parasitic BJTs lead to a higher transient latchup immunity in a *p–n–p–n* structure against well or substrate currents triggering.

The developed physical criterion and timing model for transient latchup are useful and convenient in

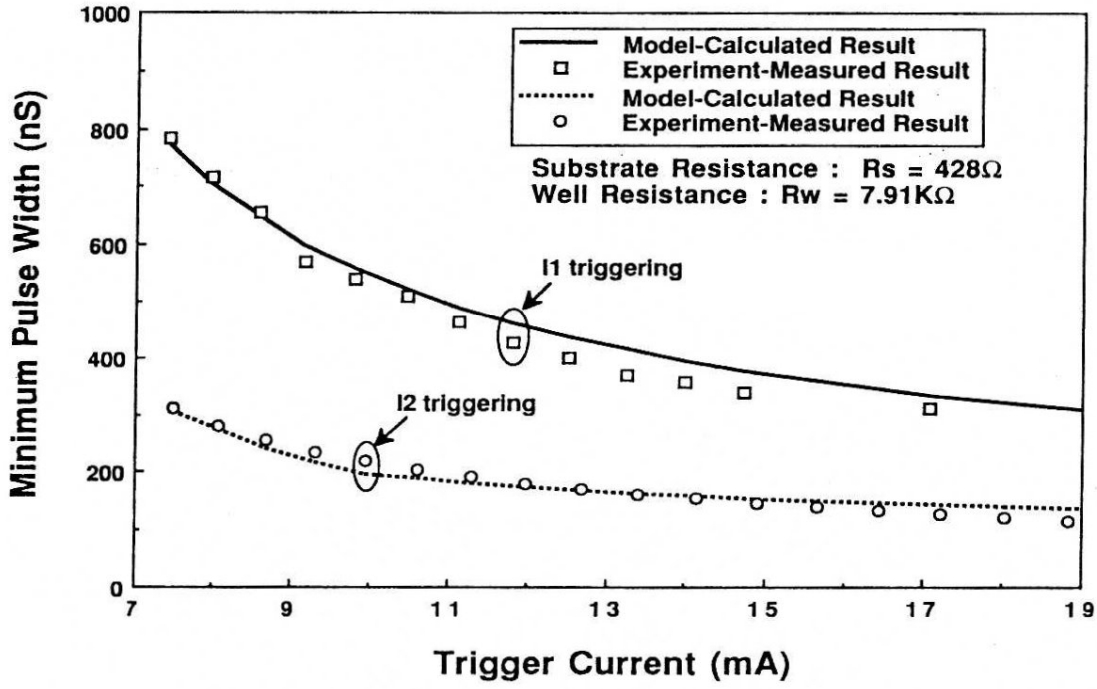

Fig. 9. The comparison of the measured and the model calculated results of the minimum pulse widths to initiate latchup as functions of the trigger currents with the substrate resistance 428 Ω and the well resistance 7.91 kΩ.

Table 6. Device parameters of the parasitic BJTs in the fabricated test structure

Parameter	$Q1(p-n-p)$ Lateral BJT	$Q2(n-p-n)$ Vertical BJT
β_F	0.623	322
β_R	0.104	6.5
I_S(A)	8.48E − 18	4.29E − 15
I_{KF}(A)	7.59E − 3	2.26E − 4
I_{SE}(A)	1.166E − 17	4.04E − 14
I_{SC}(A)	5.134E − 15	6.819E − 13
τ_F(S)	1.05E − 6	1.745E − 7
τ_R(S)	4.04E − 6	6.57E − 7
C_{je0}(F)	9E − 13	9E − 13
C_{je0}(F)	8.82E − 14	4.80E − 14
V_{AF}	40	8.6
V_{AR}	20	2
N_F	1.002	1.405
N_E	0.989	2.093
N_C	1.084	2.674
N_R	1.026	1.041
MJE	0.5	0.5
MJC	0.33	0.33

transient latchup analyses with any type of triggering. The developed physical criterion can also be applied to the numerical transient latchup analysis as well. Moreover, the developed criterion and model can be applied to the automatic latchup immunity checking, which are required in future CMOS VLSI design with submicron technologies.

Table 7. The piecewise-averaged junction capacitances of the parasitic BJTs in a $p-n-p-n$ structure

1. The averaged diffusion capacitance of a forward-biased base–emitter junction over its operating voltage range from v_{BEa} to v_{BEb} is:

$$\overline{C_{rbe}} = \frac{\tau_F \cdot I_S}{v_{BEb} - v_{BEa}} \cdot \left[\frac{e^{v_{BEb}/V_T \cdot N_F} - 1}{q_b(v_{BEb})} - \frac{e^{v_{BEa}/V_T \cdot N_F} - 1}{q_b(v_{BEa})} \right].$$

2. The averaged diffusion capacitance of a reverse-biased base–collector junction with its operating voltage range from v_{BCa} to v_{BCb} is:

$$\overline{C_{rbc}} = \frac{\tau_R \cdot I_S}{v_{BCb} - v_{BCa}} \cdot [e^{v_{BCb}/V_T \cdot N_R} - e^{v_{BCa}/V_T \cdot N_R}].$$

3. The averaged depletion capacitance of an abrupt base–emitter junction over its operating voltage range from v_{BEa} to v_{BEb} is:

$$\overline{C_{jbe}} = \frac{2 \cdot \phi_b \cdot C_{je0}}{v_{BEb} - v_{BEa}} \cdot \left[\left(1 - \frac{v_{BEa}}{\phi_b}\right)^{1/2} - \left(1 - \frac{v_{BEb}}{\phi_b}\right)^{1/2} \right]$$

when $v_{BEa} < v_{BEb} < \phi_b/2$,

$$\overline{C_{jbe}} = \frac{C_{je0}}{v_{BEb} - v_{BEa}} \cdot \left\{ 2 \cdot \phi_b \cdot \left[\left(1 - \frac{v_{BEa}}{\phi_b}\right)^{1/2} - \left(\frac{1}{2}\right)^{1/2} \right] + \frac{\left(v_{BEb} - \frac{\phi_b}{2}\right)}{4 \cdot (0.5)^{3/2}} \cdot \left[1 + \frac{\left(v_{BEb} + \frac{\phi_b}{2}\right)}{\phi_b} \right] \right\}$$

when $v_{BEa} < \phi_b/2 < v_{BEb}$,

$$\overline{C_{jbe}} = \frac{C_{je0}}{4 \cdot (0.5)^{3/2}} \cdot \left[1 + \frac{(v_{BEb} + v_{BEa})}{\phi_b} \right]$$

when $v_{BEb} > v_{BEa} > \phi_b/2$.

4. The averaged depletion capacitance of a reverse-biased grading base–collector junction over its operating voltage range from v_{BCa} to v_{BCb} is:

$$\overline{C_{jbc}} = \frac{\frac{3}{2} \cdot \phi_b \cdot C_{je0}}{v_{BCb} - v_{BCa}} \cdot \left[\left(1 - \frac{v_{BCa}}{\phi_b}\right)^{2/3} - \left(1 - \frac{v_{BCb}}{\phi_b}\right)^{2/3} \right]$$

when $v_{BCb} < v_{BCa} < 0$.

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APPENDIX A

Through the circuit connection in Fig. 1(b), the relations among the large-signal branch currents and node voltages are:

$$i_{C2}(t) + I_1(t) - i_{B1}(t) - \frac{v_{EB1}(t)}{Rs} = 0 \quad \text{(A1)}$$

$$i_{C1}(t) + I_2(t) - i_{B2}(t) - \frac{v_{BE2}(t)}{Rw} = 0 \quad \text{(A2)}$$

$$v_{CB1}(t) = v_{BC2}(t) = -[V_{DD} - v_{EB1}(t) - v_{BE2}(t)]. \quad \text{(A3)}$$

The V_{DD} power supply used in CMOS ICs is generally of 5 V. Taking the transient currents of junction depletion and diffusion capacitances into considerations and using the

modified Gummel–Poon model of BJT[17–19], the large-signal base and collector currents of BJTs $Q1$ and $Q2$ in Fig. 1(b) can be written as:

$$i_{B1}(t) = I_{B1} + \frac{\partial(Ce1 \cdot v_{EB1})}{\partial t} + \frac{\partial(Cc1 \cdot v_{CB1})}{\partial t} \quad \text{(A4)}$$

$$i_{C1}(t) = I_{C1} - \frac{\partial(Cc1 \cdot v_{CB1})}{\partial t} \quad \text{(A5)}$$

$$i_{B2}(t) = I_{B2} + \frac{\partial(Ce2 \cdot v_{BE2})}{\partial t} + \frac{\partial(Cc2 \cdot v_{BC2})}{\partial t} \quad \text{(A6)}$$

$$i_{C2}(t) = I_{C2} - \frac{\partial(Cc2 \cdot v_{BC2})}{\partial t}, \quad \text{(A7)}$$

where

$$Ce1 = C_{jbe1} + C_{tbe1} \quad \text{(A8)}$$

$$Cc1 = C_{jbc1} + C_{tbc1} \quad \text{(A9)}$$

$$Ce2 = C_{jbe2} + C_{tbe2} \quad \text{(A10)}$$

$$Cc2 = C_{jbc2} + C_{tbc2} \quad \text{(A11)}$$

In above equations, the $I_{B1(2)}$ and $I_{C1(2)}$ are the voltage-dependent intrinsic base and collector currents of $Q1(2)$. The $C_{jbe1(2)}$ and $C_{jbc1(2)}$ are the base–emitter and base–collector junction depletion capacitances of $Q1(2)$, whereas the $C_{tbe1(2)}$ and $C_{tbc1(2)}$ are the base–emitter and base–collector diffusion capacitances of $Q1(2)$. The equations of the intrinsic base and collector currents as well as the junction depletion and diffusion capacitances of a BJT device have been summarized in Tables 1 and 2, respectively[18].

The $\partial(C_j \cdot v_j)/\partial t$ terms in (A4)–(A7) can be further approximated as $C_j \cdot (\partial v_j/\partial t)$ because the value of the $\partial C_j/\partial t$ term is much smaller and can be negligible at each operating voltage range, where the C_j and v_j represent the junction capacitance and its voltage bias in each junction of a p–n–p–n structure. Substituting (A4)–(A7) into (A1) and (A2), and using the voltage relations in (A3), the dynamic behaviors of the base–emitter voltages $v_{EB1}(t)$ and $v_{BE2}(t)$ can be exactly obtained as expressed in (1)–(5).

APPENDIX B

Choosing two proper values of the base–emitter voltages for each of the BJTs $Q1$ and $Q2$, their base and collector currents can be approximated by using the piecewise linear models as:

$$I_{C1} = I_{C10} + g_{C1} \cdot v_{EB1} \quad \text{(B1)}$$

$$I_{B1} = I_{B10} + g_{B1} \cdot v_{EB1} \quad \text{(B2)}$$

for $Q1$, when $v_{EB1} \geqslant V_{EB1on}$;

and

$$I_{C2} = I_{C20} + g_{C2} \cdot v_{BE2} \quad \text{(B3)}$$

$$I_{B2} = I_{B20} + g_{B2} \cdot v_{BE2} \quad \text{(B4)}$$

for $Q2$, when $v_{BE2} \geqslant V_{BE2on}$.

If the base–emitter voltage is less than its corresponding turn-on voltage V_{EB1on} (V_{BE2on}), the base and collector currents of $Q1$ ($Q2$) are set to zeros to simplify model calculation.

In (B1) and (B2), the large-signal transconductances of the collector and the base currents with respect to the base–emitter voltage of $Q1$ BJT are defined as:

$$g_{C1} \equiv \frac{\Delta I_{C1}}{\Delta v_{EB1}} = \frac{I_{C1}(V_{EB1b}, V_{CB1b}) - I_{C1}(V_{EB1a}, V_{CB1a})}{V_{EB1b} - V_{EB1a}} \quad \text{(B5)}$$

$$g_{B1} \equiv \frac{\Delta I_{B1}}{\Delta v_{EB1}} = \frac{I_{B1}(V_{EB1b}, V_{CB1b}) - I_{B1}(V_{EB1a}, V_{CB1a})}{V_{EB1b} - V_{EB1a}}, \quad \text{(B6)}$$

and the zero-biased initial currents are

$$I_{C10} \equiv I_{C1}(V_{EB1b}, V_{CB1b}) - g_{C1} \cdot V_{EB1b} \quad \text{(B7)}$$

$$I_{B10} \equiv I_{B1}(V_{EB1b}, V_{CB1b}) - g_{B1} \cdot V_{EB1b}. \quad \text{(B8)}$$

With the above linearized relations, the approximated turn-on voltages of the BJT $Q1$ can be obtained as:

$$V_{EB1on} = -\frac{1}{2} \cdot \left(\frac{I_{C10}}{g_{C1}} + \frac{I_{B10}}{g_{B1}} \right). \quad \text{(B9)}$$

The two base–emitter voltages, V_{EB1a} and V_{EB1b}, used in the above linearized equations for $Q1$ are estimated at the fixed voltages of 0.68 and 0.78 V, respectively. The corresponding base–collector voltages can be found by (A3). Similar technique is also applied with the base–emitter voltages V_{BE2a}(0.65 V) and V_{BE2b}(0.75 V) of $Q2$ to determine the piecewise-linearized parameters of g_{C2}, g_{B2}, I_{C20}, I_{B20}, and V_{BE2on} in (B3) and (B4).