CMOS ON-CHIP ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT USING FOUR-SCR STRUCTURES WITH LOW ESD-TRIGGER VOLTAGE

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Abstract—A robust CMOS on-chip ESD protection circuit is proposed, which consists of four parasitic lateral SCR devices with low ESD trigger voltages to protect NMOS and PMOS devices of the internal circuits against the ESD pulses with both positive and negative polarities with respect to either VDD or VSS(GND) nodes. For each ESD stress with positive or negative polarity, there is an efficient and direct shunt path generated by the SCR low-impedance latching state to quickly bypass the ESD current. Thus, this four-SCR ESD protection circuit can perform very efficient protection in a small layout area. Since there is no diffusion or polysilicon resistor in the proposed ESD protection circuit, the RC delay between each I/O pad and its internal circuits is very low and high-speed applications are feasible. The experimental results show that this four-SCR protection circuit can successfully perform very effective protection against ESD damage. Moreover, the proposed ESD protection circuit is fully process-compatible with n-well or p-well CMOS and BiCMOS technologies.

1. INTRODUCTION

It is known that the electrostatic discharge (ESD) damage is one of the most insidious failure mechanisms of electronic devices and systems. MOS devices, in particular, because of their inherently high input impedance, are extremely susceptible to the ESD damage. The gate oxide thickness of the present submicron (0.5–0.8 μm) CMOS technologies is in the range of 100–200 Å, which could be ruptured by applying about 10–20 V across it if the dielectric breakdown strength of SiO_2 is around 10 MV/cm[1]. Therefore, it is necessary to provide an efficient on-chip ESD protection circuit in each I/O pad of CMOS ICs.

Generally, ESD voltages have different polarities to both VDD and VSS (ground) nodes and these ESD voltage pulses could damage both NMOS and PMOS devices in the input buffer or output driver of CMOS ICs. In the commonly used input ESD protection circuits, which are often made by the combination of thick-oxide NMOSFET, diffusion resistor/diode, and thin-oxide NMOSFET (sometimes called "Field Plate Diode")[2], the ESD protection circuit is only placed from each input pad to the VSS(GND) node. With such an arrangement, it can effectively provide a shunt path from input pad to VSS(GND) node if the ESD voltages have both positive and negative polarities to the VSS(GND) node. But it has no direct shunt path for the ESD pulses with positive or negative polarities to the VDD node. Thus, the PMOS device of the input stage is more susceptible to ESD damage so as to cause serious reliability

problems[3]. The other type of commonly used ESD input/output protection circuits is made by two diodes. The diodes become reversely biased and then break down to protect the internal circuits if the ESD voltage has a negative polarity to VDD when the VSS(GND) node is floating or a positive polarity to VSS(GND) when the VDD node is floating. This reverse condition may easily damage internal circuits because it could not quickly discharge the ESD currents[3]. In [3], it is shown that the drain diffusion of the PMOS device in the input inverter stage with $W/L = 3.0/1.5\,\mu$m, which is protected by the two-diode ESD protection circuit, is damaged by applying a 400 V Human-Body-Mode (HBM) ESD pulse with the positive polarity to the input pad where the VSS(GND) node is grounded and the VDD node is floating. The reason for this anomalous phenomenon is that the breakdown of the VSS(GND) protection diode is not sufficient to discharge the ESD current. At this time, the VDD protection diode is forward biased and diverts this ESD current to the VDD supply line. The diverted ESD voltage to the VDD node drops across the off-PMOS device in the first inverter stage because the series NMOS device of the inverter stage is turned on by the positive ESD voltage at its gate. This large ESD voltage stresses the PMOS device and damages it. Similar damage can also occur in the NMOS device of the first inverter stage under a negative ESD pulse at the I/O pad to the VDD node when the VSS(GND) node is floating.

Recently, the parasitic lateral SCR device has been used in CMOS on-chip ESD protection circuits[4–12]. Due to its high ESD failure threshold, the

parasitic lateral SCR device has been recognized as one of the most effective elements in on-chip ESD protection circuits of the advanced scaled-down CMOS technologies. However, the parasitic lateral SCR device is arranged between I/O pad and VSS(GND) node with its anode connected to I/O pad and its cathode connected to VSS(GND) node[6–10], since the SCR device has a single-polarity current conduction characteristics. With this arrangement, the SCR device can provide a shunt path from input pad to VSS(GND) node if the ESD voltage has positive polarity to VSS(GND) node. If the ESD voltage has a negative polarity to VSS(GND) node, the base–collector junction diode in the SCR device is forward biased to bypass the ESD stress. However, this arrangement of the lateral SCR device in the ESD protection circuits cannot provide an effective protection for the ESD stress from the I/O pad to the VDD node. If an ESD voltage occurs at the input pad with positive polarity to the VDD node whereas the VSS(GND) node is floating, the ESD current is first diverted to the floating VSS line through the SCR device. Then, this diverted ESD current flows from the VSS line to VDD node through the forward-biased parasitic well/substrate junction diode in the CMOS structure, which has its anode connected to VSS(GND) node but its cathode connected to VDD node. On the other hand, if the ESD voltage occurs at the input pad with negative polarity to the VDD node in the worst case of floating VSS node, the negative ESD voltage is diverted to the floating VSS line through the base–collector junction diode in the SCR device. This negative ESD voltage at the floating VSS line is hard to effectively discharge to the VDD node through the reverse-biased parasitic well/substrate junction diode. Thus, the PMOS device of internal circuits may be directly stressed by the ESD pulses with negative polarity from I/O pad to VDD node while the VSS(GND) node is floating.

In our previous work[11,12], the dual parasitic SCR structures were placed between the I/O pad and the VDD node so as to provide efficient ESD protection for both positive and negative ESD stresses. One SCR device is arranged to provide a discharge path for the ESD stress with positive polarity from I/O pad to VDD node. The other one provides a discharge path for the ESD stress with negative polarity from the I/O pad to VDD node. There is also a parasitic p-well/n-substrate junction diode between the VDD and VSS(GND) nodes in this CMOS structure. When the ESD stress has a negative polarity at the I/O pad with respect to the VSS(GND) node in the case of floating VDD node, the forward-biased parasitic p-well/n-substrate junction diode between VDD and VSS(GND) nodes can provide an ESD discharge path in cooperation with the SCR device. If the ESD stress has a positive polarity to VSS(GND) node in the worst case of floating VDD node, the ESD voltage at the I/O pad is first diverted through an SCR device to the VDD line and then discharges

through the reverse-biased parasitic p-well/n-substrate junction diode to VSS(GND) node. This discharge path is not effective to bypass the ESD stress in the internal circuits if there is no extra protection circuit between VDD and VSS(GND) nodes. Thus effective ESD protection circuit is required to provide a direct discharging path to quickly bypass each ESD stress with any polarities to both VDD and VSS(GND) nodes, especially in the much faster Machine-Mode (MM) and Charge-Device-Mode (CDM)[13,14] ESD transitions.

To overcome the above described problems in the previous reported ESD protection circuits, a novel four-SCR ESD protection circuit is proposed[15,16]. In the new protection circuit, four parasitic lateral SCR devices with low ESD trigger voltage are designed to directly discharge the ESD currents of the positive or negative ESD pulses at each I/O pad to both VDD and VSS(GND) nodes. The new structure can perform very efficient ESD protection within a small layout area. Since the new structure does not use series resistors between the I/O pad and its internal circuits, the resultant RC delay is very small. The configuration and arrangement of the four-SCR ESD protection circuit are presented in Section 2. The parasitic lateral SCR devices can be designed to achieve a very low ESD trigger voltage. The design methodology is described in Section 3. The proposed four-SCR ESD protection circuit has been successfully fabricated and tested. The experimental results are given in Section 4. Finally, the conclusion is drawn.

2. THE FOUR-SCR ESD PROTECTION CIRCUIT

The lumped equivalent circuit of the proposed CMOS on-chip four-SCR ESD protection circuit with four lateral SCR devices is shown in Fig. 1 and a demonstrated layout example is given in Fig. 2 with the corresponding cross-sectional view given in Fig. 3, where the n-substrate p-well CMOS process is used. In the p-well process, the n-substrate is biased at VDD. The ESD protection circuit in Fig. 1 consists of four lateral SCR devices (SCR_1, SCR_2, SCR_3 and SCR_4) which are in the identical layout structures but with different connections to their anodes and cathodes as shown in Fig. 2. The lateral SCR_1 and SCR_2 devices are arranged to protect against negative and positive ESD pulses at the I/O pad to the VDD node, respectively. Similarly, the lateral SCR_3 and SCR_4 devices are arranged to protect against negative and positive ESD pulses at the I/O pad to the VSS(GND) node, respectively.

Each one of the lateral SCR devices (SCR_1, SCR_2, SCR_3 or SCR_4) is formed by a parasitic lateral p–n–p bipolar transistor (Q_{1u}, Q_{3u}, Q_{1L} or Q_{3L}) and a parasitic vertical n–p–n bipolar transistor (Q_{2u}, Q_{4u}, Q_{2L} or Q_{4L}) in addition with a parasitic field-oxide NMOSFET (for SCR_1 and SCR_3) or PMOSFET (for SCR_2 and SCR_4) to further enhance its turn-on
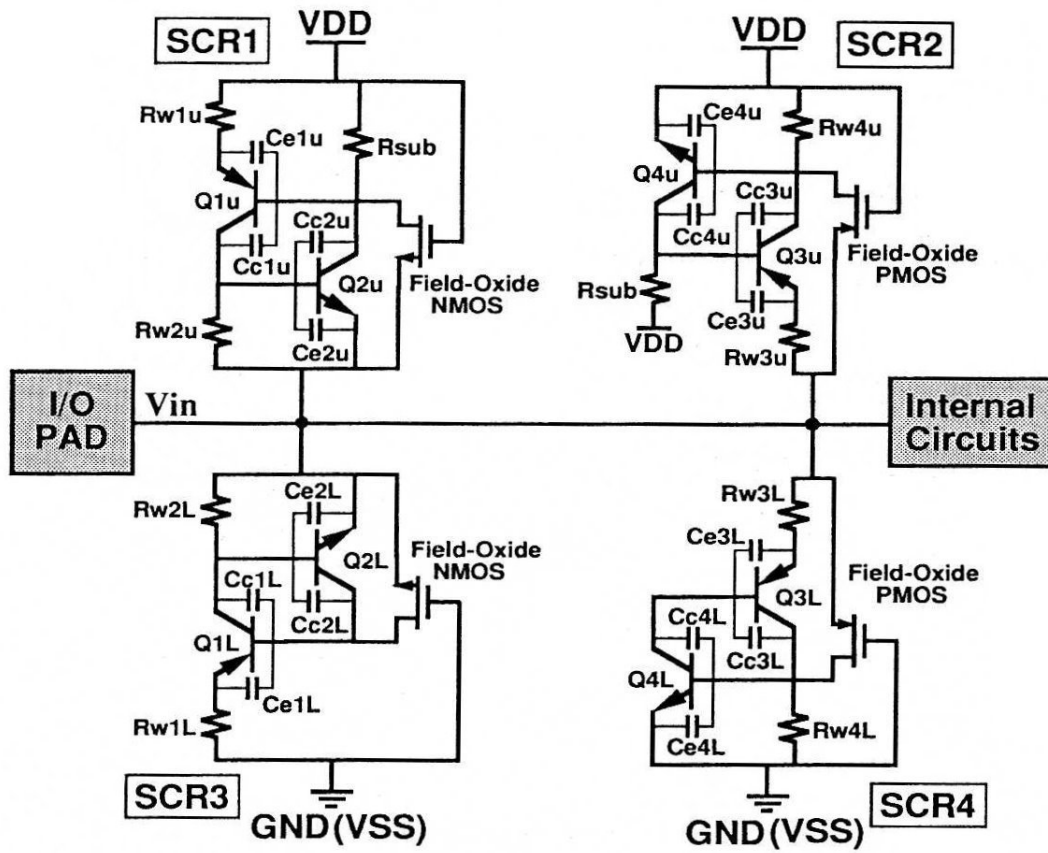
Fig. 1. The lumped equivalent circuit of the proposed CMOS on-chip four-SCR ESD protection circuit.
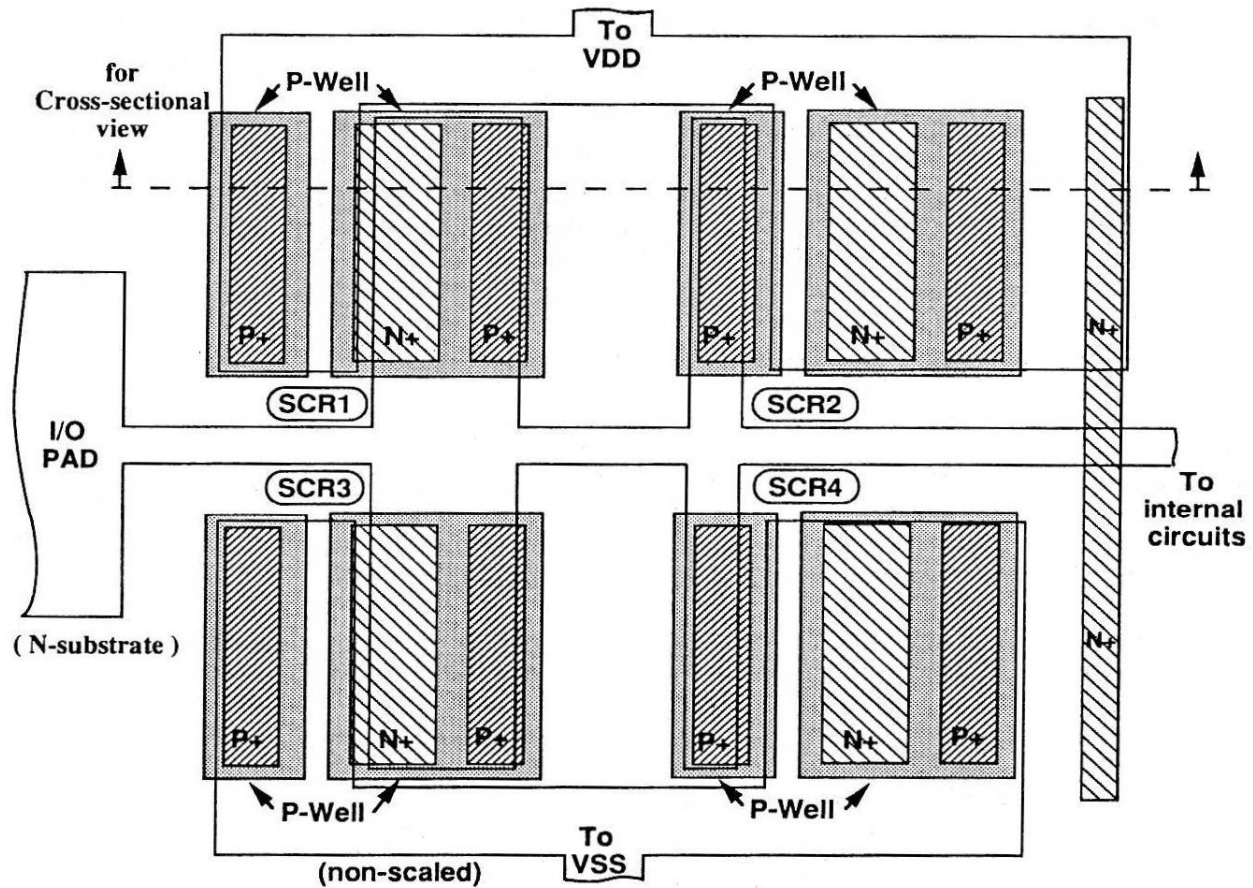

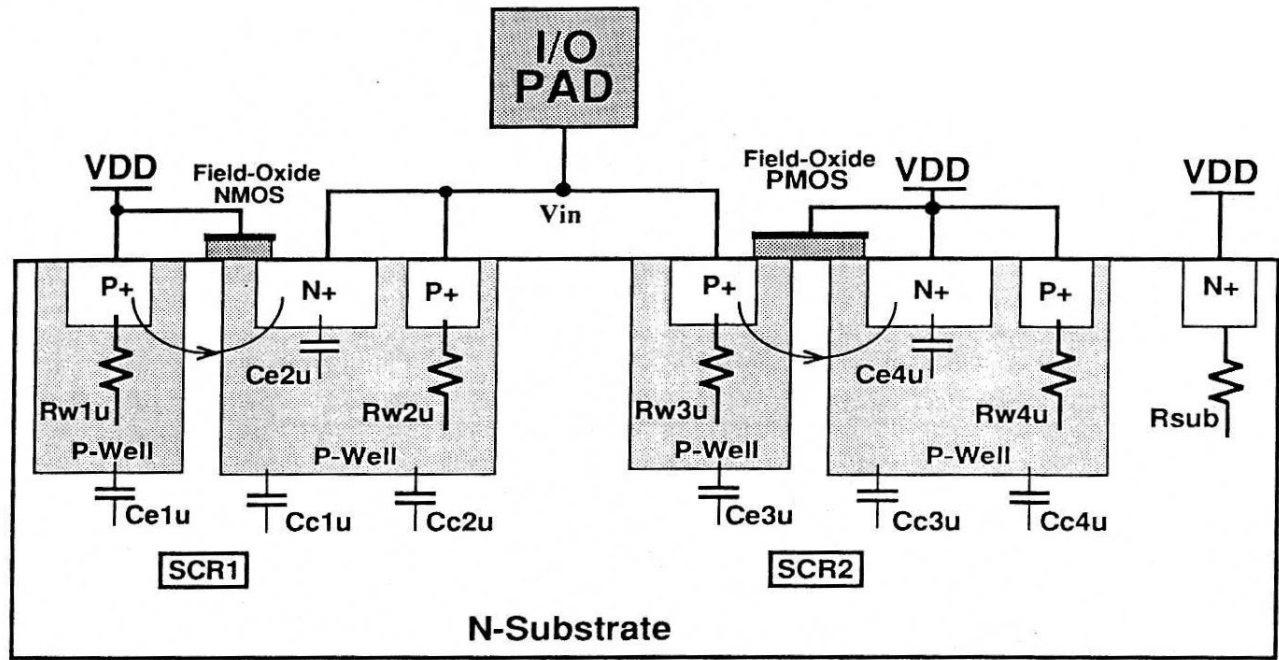Fig. 2. A layout example of the four-SCR ESD protection circuit.

Fig. 3. The cross-sectional view of the parasitic lateral SCR$_1$ and SCR$_2$ devices shown in Figs 1 and 2.

speed during the ESD transitions, respectively. The parasitic lateral p–n–p transistor (Q_{1u}, Q_{3u}, Q_{1L} or Q_{3L}) is formed by using a P^+ diffusion in the p-well as its emitter, the n-substrate as its base, and an adjacent p-well as its collector. Using the P^+ diffusion in a p-well rather than the P^+ diffusion only as the emitter of the lateral p–n–p transistor, the lateral SCR device has a larger and deeper anode structure. This deeper anode structure provides more current-flowing active area to its cathode, so that the proposed lateral SCR device can sustain higher ESD stresses. The smaller distance between p-well emitter and p-well collector can make a larger beta gain (β) of the lateral p–n–p transistor. This beta gain (β) can easily be made greater than one in CMOS technologies. The parasitic vertical n–p–n transistor (Q_{2u}, Q_{4u}, Q_{2L} or Q_{4L}) is composed of an N^+ diffusion in the p-well as its emitter, the p-well as its base, and the n-substrate as its collector. Although the beta gain (β) of such a vertical n–p–n transistor is dependent upon the process, the typical maximum forward beta gain (β_F) usually can be as high as 100. The positive feedback in each SCR device with the beta-gain product of the lateral and the vertical bipolar junction transistors (BJTs) much greater than one will lead to a very fast latching regeneration process to push the SCR device quickly into its low-impedance latchup state when an ESD event is occurring to trigger this SCR device. The parasitic field-oxide NMOSFET is formed by the N^+ diffusion/p-well/n-substrate structure as its source/bulk/drain, whereas the parasitic field-oxide PMOSFET is formed by the p-well/n-substrate/p-well structure. The gate is formed by the metal line on the field oxide. Because the parasitic field-oxide NMOSFET and PMOSFET can divert extra triggering currents to the base nodes

of the parasitic lateral p–n–p transistors (Q_{1u} and Q_{1L}) and the parasitic vertical n–p–n transistors (Q_{4u} and Q_{4L}), respectively, the trigger voltage of the associated lateral SCR device can be decreased and the turn-on speed can be enhanced.

There are some parasitic resistances and capacitances in the lumped equivalent ESD protection circuit as shown in Figs 1 and 3. The resistances (R_{w1u}, R_{w2u}, R_{w3u}, R_{w4u}, R_{w1L} R_{w2L}, R_{w3L} and R_{w4L}) are all the parasitic p-well resistances which essentially exist in the CMOS structures. The R_{sub} is the equivalent substrate resistance in the structures whereas the capacitances (C_{e1u}, C_{c1u}, ..., C_{e4L} and C_{c4L}) are all the parasitic p–n junction capacitances in the lateral SCR devices. These parasitic resistances and capacitances can be used to adjust the ESD trigger voltage of the lateral SCR devices.

The ESD protection circuit described above is based upon the p-well CMOS process. But, the principles are equally applicable and realizable in an n-well CMOS process if the realizations of the parasitic lateral SCR devices are modified accordingly. Thus, the fabrication process of the proposed ESD protection circuit is fully compatible with that of both p-well and n-well CMOS ICs. Moreover, the proposed four-SCR ESD protection circuit can be also implemented in the BiCMOS technology.

When a negative ESD pulse suddenly occurs at the I/O pad with respect to the VDD mode, the SCR$_1$ device is quickly triggered on by the transient currents generated by the well-substrate junction capacitances (C_{c1u} and C_{c2u}) in the transistors Q_{1u} and Q_{2u}. The transient turn-on behaviors of the lateral SCR device is analyzed in detail in next section. The field-oxide NMOSFET with its gate connected to VDD node also provides a triggering current to the

base of transistor Q_{1u}. This extra current makes the lateral SCR$_1$ device more quickly enter into its ON state. After turned on, a low-impedance path through the SCR$_1$ device is formed from the VDD node to the I/O pad and then the negative ESD pulse is quickly bypassed without damaging the internal circuits.

The operational principles of other lateral SCR devices (SCR$_2$, SCR$_3$ and SCR$_4$) are the same as that of the SCR$_1$ device. As a negative (positive) ESD pulse appears at the I/O pad to the VSS node with the worst case of VDD node floating, the SCR$_3$ (SCR$_4$) device is quickly triggered on by the transient displacement currents on the base–collector capacitances of C_{c1L} and C_{c2L} (C_{c3L} and C_{c4L}). In addition, the base of transistor Q_{3u} in the SCR$_2$ structure is connected to VDD node through the n-substrate resistance. If an ESD signal greater than about VDD + 0.6 V appears at the I/O pad with positive polarity to VDD node, the Q_{3u} is directly turned on and then causes a voltage drop in the resistance R_{w4u} to turn on transistor Q_{4u}. The SCR$_2$ device is quite quickly triggered on not only by the emitter-to-base current of Q_{3u} but also by the transient displacement currents on the capacitances of C_{C3u} and C_{c4u}. For any ESD stress with positive or negative polarities with respect to VDD or VSS(GND) nodes, there is an SCR device triggered on to bypass the ESD energy. Because the discharging path under the ESD stress with any polarity is through the similar SCR structure, the overall ESD protection capability is improved significantly.

It is known that an ESD protection circuit needs to consider the associated latchup problem. The VDD-to-VSS latchup problem can be overcome in the design of the proposed four-SCR ESD protection circuit. When a CMOS IC is in the normal operation, the VDD of 5 V must be applied to the IC. If the input signal has the unexpected noise greater than 5 V, it will be bypassed through the p-well n-substrate junction diode (the emitter–base junction of Q_{3u}) in the SCR$_2$ structure because the n-substrate is biased at 5 V. Even if the positive input signal can also turn on the SCR$_4$ device (SCR$_1$ and SCR$_3$ can not be turned on due to the unique current-conducting direction of the SCR devices), the current flows from input pad to VDD node through SCR$_2$ and from input pad to VSS node through SCR$_4$. The current does not flow from VDD to VSS node to cause the VDD-to-VSS latchup problem. So it has no VDD-to-VSS latchup problem in SCR$_2$ and SCR$_4$ devices due to an unexpected positive input signal at the input node. Similarly, even if the input signal with the unexpected noise is negative enough to turn on both SCR$_1$ and SCR$_3$ devices (SCR$_2$ and SCR$_4$ cannot be triggered on by a negative input signal), the current flows from the VDD node to input pad through SCR$_1$ and from VSS node to input pad through SCR$_3$. The current directions in SCR$_1$ and SCR$_3$ do not cause the latchup problem from VDD to VSS nodes.

The only VDD-to-VSS latchup path in the ESD protection circuit is from the P^+ diffusion (the emitter of the Q_{1u} transistor connected to VDD) in the SCR$_1$ structure, through the n-substrate, to the N^+ diffusion in p-well (the emitter of the Q_{4L} transistor connected to VSS) in the SCR$_4$ structure. This parasitic path can only be found in the whole layout of the ESD protection circuit as shown in Fig. 2. The VDD-to-VSS latchup path can be blocked by separating the P^+ emitter of SCR$_1$ and the N^+ emitter of SCR$_4$ devices by the bonding pad and by adding the latchup guard-rings to the SCR devices. Thus the latchup immunity can be improved much significantly. Generally, a farther spacing from the VDD-connected P^+ diffusion in N-substrate to the VSS-connected N^+ diffusion in p-well and wider guard-rings have higher latchup immunity.

3. THE METHOD TO LOWER THE ESD TRIGGER VOLTAGE

To lower the ESD trigger voltage of the lateral SCR devices so that the ESD protection becomes more effective, the a.c./capacitance method is adopted[11,12]. According to the analysis results of CMOS latchup[17,18], a parasitic lateral SCR device generally has a much lower a.c. trigger voltage than a d.c. one. Because an ESD voltage is of the transition type, the ESD turn-on behavior of the lateral SCR device in the proposed ESD protection circuit is related to the a.c./pulse-type trigger voltage rather than the d.c. one. The a.c./pulse-type trigger voltage can be recognized as the ESD trigger voltage if the a.c./pulse-type trigger voltage has a rise time the same as that of an ESD transition waveform. The rise time of the Human-Body-Mode(HBM) ESD waveform is in the range about 5–15 ns. In this section, the relations between the characteristics of the ESD trigger voltage and the device parameters of the parasitic lateral SCR$_1$ device in the proposed four-SCR ESD protection circuit are analyzed in detail to explore the capability of the a.c./capacitance method in lowering the ESD trigger voltage. Other SCR devices (SCR$_2$, SCR$_3$ and SCR$_4$) have the similar characteristics and capability as that of the SCR$_1$ device.

The lateral SCR$_1$ device is simply modeled as the lumped equivalent circuit shown in Fig. 1, where C_{e1u} (C_{e2u}) is the base–emitter p-well/n-substrate (N^+ diffusion/p-well) capacitance and C_{c1u} (C_{c2u}) is the base–collector p-well/n-substrate capacitance of the parasitic BJT Q_{1u} (Q_{2u}). These capacitances can easily be changed by only changing their layout area. R_{sub} (R_{w2u}) in the SCR$_1$ device is the equivalent parasitic substrate (p-well) resistance from the base of the parasitic BJT Q_{1u} (Q_{2u}) to the N^+ (P^+) diffusion of the n-substrate (p-well) contact. Both R_{sub} and R_{w2u} can be adjusted by changing the spacing of the N^+ and P^+ diffusions to the bases of the parasitic BJTs Q_{1u} and Q_{2u}, respectively. They can also be adjusted by adding or reducing the contact number in the N^+ and P^+ diffusions of the n-substrate and p-well
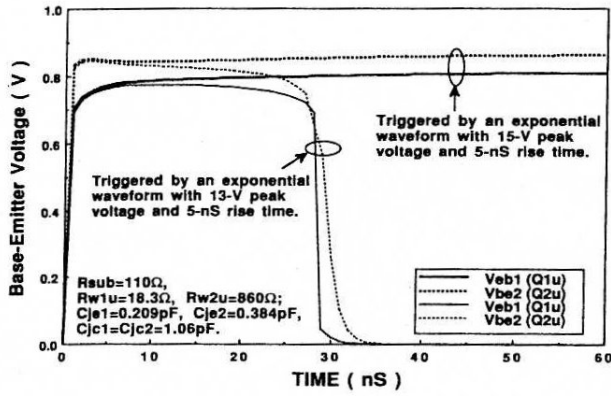
Fig. 4. The SPICE simulated base–emitter voltage waveforms vary as functions of time due to the triggering of the single-pole exponential voltage waveforms with the same rise time of 5 ns but different peak voltages of 13 and 15 V. The V_{eb1} (V_{be2}) is the base–emitter voltage of the parasitic lateral (vertical) BJT Q_{1u} (Q_{2u}) in the lateral SCR$_1$ device.

contacts. The R_{w1u} is the parasitic p-well emitter resistance of the parasitic lateral BJT Q_{1u}. In order to perform a more efficient ESD protection with a lower turn-on impedance, R_{w1u} is designed to have its minimum value of resistance by using the maximum p-well contact number with each contact in its minimum size permitted by the design rules of the CMOS technology.

A single-pole exponential voltage waveform with a fixed rise time of 5 ns but an adjustable peak voltage is used to simulate the quickly rising transition of the HBM ESD waveforms. This single-pole exponential voltage waveform is applied across the anode to cathode of the lateral SCR$_1$ device to find its ESD trigger voltage through the SPICE simulation[19]. The turn-on behavior of the lateral SCR$_1$ device can be characterized by observing the base–emitter voltage waveforms of the parasitic lateral and vertical BJTs Q_{1u} and Q_{2u} in the SCR$_1$ device. The typical base–emitter voltage waveforms under different peak voltages triggering with the same rise time of 5 ns are shown in Fig. 4 in both the latching and non-latching cases of the lateral SCR$_1$ device. The parasitic resistances and capacitances of the lateral SCR$_1$ device in

the SPICE simulation are also listed in Fig. 4, where the C_{je1} (C_{je2}) and C_{jc1} (C_{jc2}) are the zero-biased base–emitter and base–collector junction capacitances of the parasitic lateral (vertical) BJT Q_{1u} (Q_{2u}). If the base–emitter voltage waveforms, V_{eb1} (for BJT Q_{1u}) and V_{be2} (for BJT Q_{2u}), remain at about 0.75–0.85 V under the triggering of the simulated HBM ESD rise-transition voltage, the lateral SCR$_1$ device is triggered on. If the base–emitter voltage waveforms drop to 0 V after the ESD rise-transition triggering, the lateral SCR$_1$ device is OFF. This means that the lateral SCR$_1$ device can not be triggered on by the simulated HBM ESD rise-transition voltage with a 5 ns rise time if the peak voltage is below a certain voltage level. It is clearly shown in Fig. 4 that the lateral SCR$_1$ device can be triggered on by a single-pole exponential voltage waveform with its peak voltage of 15 V, but it can not be triggered on by the same waveform with a 13 V peak voltage. If the peak voltage raises from 13 to 15 V, there is a minimum value in the peak voltage of the single-pole exponential voltage waveform with a fixed 5 ns rise time to initiate the latching behavior of the lateral SCR$_1$ device. This minimum value of the peak voltage can be recognized as the "simulated ESD trigger voltage" of the lateral SCR$_1$ device. It is also found in Fig. 4 that the turn-on speed of the typical lateral SCR device under the HBM ESD rise-transition triggering is quite quick, being within 1 ns. Under the much shorter rise time of Machine-Mode(MM) and Charge-Device-Mode (CDM) ESD events, the SCR device is triggered on more quickly due to the larger transient displacement current ($i = C \cdot dV/dt$) in the base–collector capacitances of the SCR device. This implies that the four-SCR ESD protection circuit is also very efficient in the protection against the faster rising transition of Machine-Mode and Charge-Device-Mode ESD stresses.

Through the simulated ESD trigger voltages, the effect of the substrate resistance R_{sub} on the ESD trigger voltage can be quantitatively analyzed as shown in Fig. 5. The effect of the p-well resistance R_{w2u} on the ESD trigger voltage is also simulated and shown in Fig. 6. Similar to the CMOS latchup
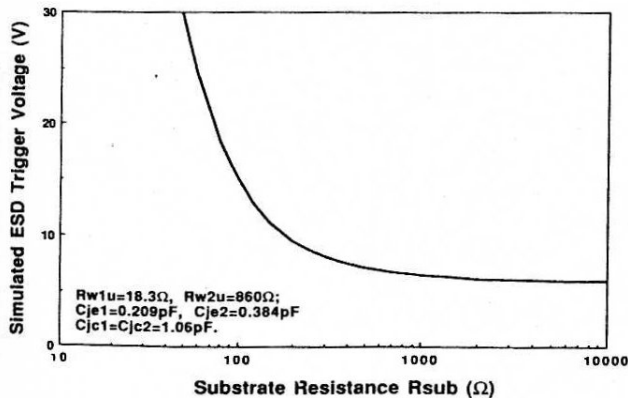

Fig. 5. The influence of the substrate resistance R_{sub} on the simulated ESD trigger voltage under the triggering condition of 5 ns rise time.
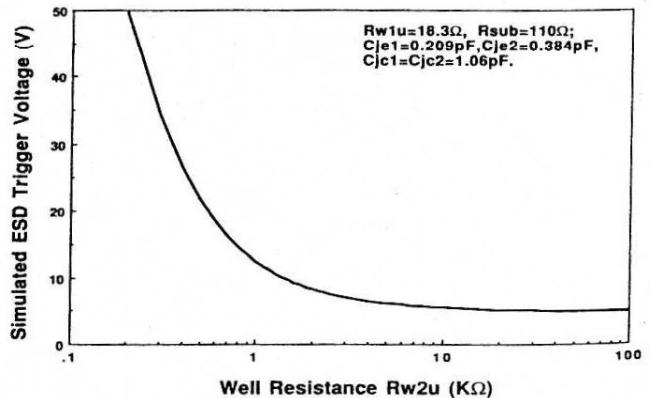

Fig. 6. The influence of the p-well resistance R_{w2u} on the simulated ESD trigger voltage.
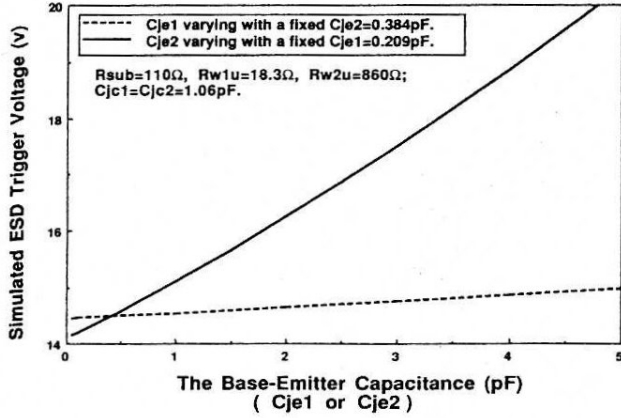
Fig. 7. The influence of the base–emitter junction capacitance on the simulated ESD trigger voltage. The C_{je1} (C_{je2}) is the zero-biased base–emitter junction capacitance of the lateral (vertical) BJT Q_{1u} (Q_{2u}) in the lateral SCR$_1$ device.

characteristics[17,18], larger R_{sub} and R_{w2u} lead to a lower simulated ESD trigger voltage, but too large R_{sub} and R_{w2u} resistances have a saturation effect in reducing the simulated ESD trigger voltage. The effects of the base–emitter capacitances, C_{e1u} and C_{e2u}, on the simulated ESD trigger voltage are shown in Fig. 7 whereas the influence due to the total base–collector capacitances, $C_{e1u} + C_{c2u}$, in the lateral SCR$_1$ device is shown in Fig. 8. It is indicated that the ESD trigger voltage has a nearly linear-increasing relation with the base–emitter capacitances of the parasitic lateral and vertical BJTs in the lateral SCR device. Especially, the base–emitter capacitance of the vertical BJT has a much stronger effect in increasing the ESD trigger voltage than that of the lateral BJT. In Fig. 7, the simulated ESD trigger voltage only increases a little from 14.44 to 14.97 V as the base–emitter capacitance C_{je1} varies from 0.05 to 5 pF with a fixed $C_{je2} = 0.384$ pF, where the C_{je1} (C_{je2}) is the zero-biased junction capacitance of the p-well (N^+ diffusion) emitter in the parasitic lateral (vertical) BJT Q_{1u} (Q_{2u}). As described in Section 2, a larger and deeper p-well is used instead of a P^+ diffusion in the n-substrate as the emitter of the lateral BJT Q_{1u} in the

SCR$_1$ device to increase its ESD protection capability. The larger and deeper p-well emitter generally leads to a larger base–emitter junction capacitance C_{e1u}, but it has only quite a little increase in the ESD trigger voltage of the lateral SCR$_1$ device as the dashed line shown in Fig. 7. Thus, it can be realized from the above descriptions that a lateral SCR device can sustain high ESD stresses but with a low ESD trigger voltage. Besides, if the base–collector capacitances of the parasitic BJTs Q_{1u} and Q_{2u} decrease, the simulated ESD trigger voltage increases much greater. This implies that the larger base–collector p-well/n-substrate junction capacitance leads to a lower ESD trigger voltage of the lateral SCR device.

The influences of the maximum forward beta gains (β_{F1} and β_{F2}) of both lateral and vertical BJTs Q_{1u} and Q_{2u} in the lateral SCR$_1$ device on the ESD trigger voltage are also simulated and the results are shown in Fig. 9(a) and (b), respectively. They show that higher beta gains of the parasitic lateral and vertical BJTs in a lateral SCR device cause a lower ESD trigger voltage.

If the trigger signal of the single-pole exponential voltage waveform has different rise times, the ESD trigger voltage under each different rise time with the

(a)

(b)
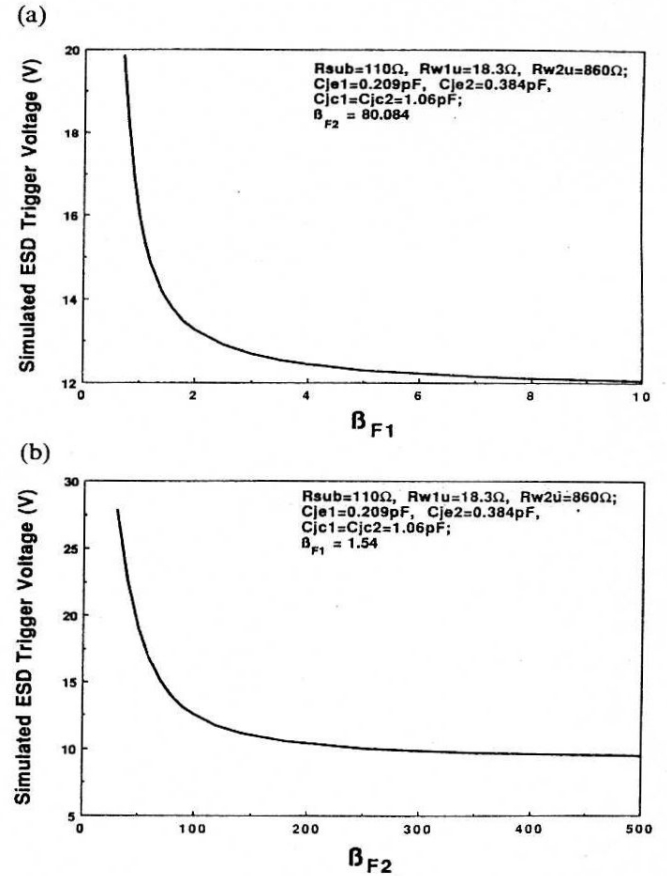
Fig. 9. The influences of the beta gains in the lateral and vertical BJTs on the ESD trigger voltage of the lateral SCR device. (a) The relation between the simulated ESD trigger voltage and the maximum forward beta gain (β_{F1}) of the lateral BJT Q_{1u} in the lateral SCR$_1$ device. (b) The relation between the simulated ESD trigger voltage and the maximum forward beta gain (β_{F2}) of the vertical BJT Q_{2u} in the lateral SCR$_1$ device.
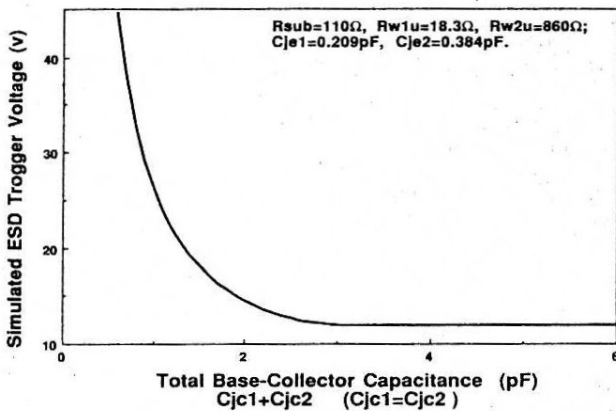

Fig. 8. The influence of the base–collector junction capacitance on the simulated ESD trigger voltage. The C_{jc1} (C_{jc2}) is the zero-biased base–collector junction capacitance of the lateral (vertical) BJT Q_{1u} (Q_{2u}) in the lateral SCR$_1$ device.
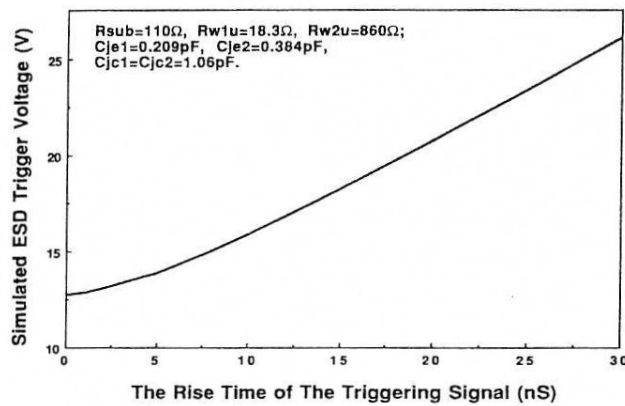
Fig. 10. The relation between the rise time of the single-pole exponential triggering signal and the simulated ESD trigger voltage.

same device parameters of the lateral SCR_1 device can be also simulated. The results are shown in Fig. 10 and indicate that the ESD triggering signal with a longer rise time requires a higher ESD trigger voltage to turn on the lateral SCR device. This implies that the ESD trigger voltage of the lateral SCR device under the MM or the CDM ESD stresses has a smaller value than that under the HBM ESD stress, because the rising transition of both MM and CDM ESD is faster than that of the HBM ESD. All the device parameters of the parasitic lateral and vertical BJTs used in the above SPICE simulations are listed in Table 1, which are measured from the really fabricated lateral SCR device in the proposed four-SCR ESD protection circuit.

From the above SPICE simulation results on the trigger-on behaviors of the lateral SCR_1 device, it is found that the ESD trigger voltage of the lateral SCR device can be adjusted through the design of the ratio between C_{e1u}, C_{e2u}, C_{c1u} and C_{c2u} with the appropriate substrate and well resistance R_{sub} and R_{w2u}. The larger the well-substrate junction capacitances (C_{c1u} and C_{c2u}), the larger transient current is generated to trigger on the lateral SCR device during the occurrence of ESD transitions. The low ESD trigger voltage of the lateral SCR device can be achieved by the a.c./capacitance method without involving any device or junction breakdown. Thus, the protection

capability and performance does not degrade after numerous ESD transitions and the robustness of the ESD protection circuit can be improved significantly. The layout of the proposed four-SCR ESD protection circuit can be accomplished to meet the above requirements on device resistances and capacitances. Although a lower ESD trigger voltage is expected to provide a more effective protection for the internal circuits against ESD damages, it can not be too low in order to guarantee that the ESD protection circuit can not be triggered on by the normal input and output signals of the CMOS ICs.

4. EXPERIMENTAL RESULTS

One set of the four-SCR ESD protection circuits with different layout dimensions has been implemented by using 0.8 μm twin-well bulk CMOS process with LDD structure and silicide[20]. The chip photomicrograph of one fabricated four-SCR ESD protection circuit is shown in Fig. 11. The SCR_1 and SCR_2 devices are laid between I/O pad and VDD line whereas the SCR_3 and SCR_4 devices are laid between I/O pad and VSS(GND) line. The main reason for the SCR_1 and SCR_2 devices separated from the SCR_3 and SCR_4 devices by the I/O pad is to obtain a better VDD-to-VSS(GND) latchup immunity. For higher latchup immunity specification, the extra guard-rings are required to surround the whole ESD protection circuit to prevent the VDD-to-VSS(GND) latchup problems.

The testing results of ESD failure thresholds in HBM and MM ESD stresses for the fabricated four-SCR ESD protection circuits with different layout dimensions of the lateral SCR devices are listed in Table 2. The ESD failure thresholds are found by the testing methods of HBM and MM which are the MIL-STD-883C method 3015.7[21] and EIAJ-IC-121 method 20[22], respectively. The experimental results show that the ESD failure threshold of the fabricated four-SCR ESD protection circuit can be greater than $+/-$ 1000 V and $+/-$ 10 kV in MM and HBM

Table 1. The device parameters of the parasitic lateral and vertical BJTs in a lateral SCR device fabricated by a 0.8 μm CMOS process

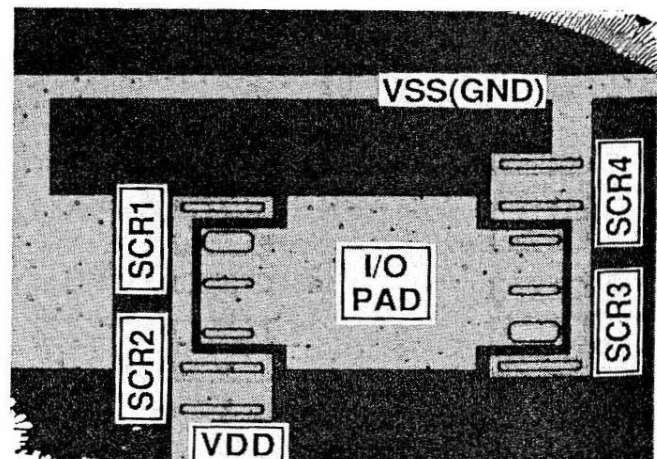| Parameter	Lateral p–n–p BJT	Vertical n–p–n BJT
β_F	1.54	80.084
β_R	0.655	0.843
$I_S(A)$	1.037E-16	1.609E-16
$I_{KF}(A)$	5.89E-4	3.016E-3
$I_{SE}(A)$	8.415E-17	4.415E-17
$I_{SC}(A)$	2.958E-16	3.613E-16
$\tau_F(S)$	28.78E-9	3.52E-10
$\tau_R(S)$	32.55E-9	1.24E-9
$V_{AF}(V)$	36.18	51.71
$V_{AR}(V)$	31.415	19.133
N_F	0.966	0.965
N_E	0.977	1.164
N_C	1.0	0.996
N_R	0.978	0.969

Fig. 11. A photomicrograph of the fabricated four-SCR ESD protection circuit.

Table 2. The experimental results of the four-SCR ESD protection circuit

	The layout area of each lateral SCR device in the fabricated four-SCR ESD protection circuit (width × length, unit: μm × μm)				
	42 × 25	42 × 50	42 × 75	43 × 50	92 × 50
ESD failure threshold voltage					
Machine-mode (+/−)	500 V	>1000 V[a]	>1000 V[a]	>1000 V[a]	>1000 V[a]
Human-body-mode (+/−)	8000 V	>10 kV[a]	>10 kV[a]	>10 kV[a]	>10 kV[a]
Trigger voltage					
D.c. condition	32.60 V	33.70 V	34.70 V	34.75 V	35.20 V
Pulse-type condition (rise time = 5 nS)	5.54 V	8.92 V	10.48 V	8.74 V	11.30 V
The anode to cathode space	5 μm	5 μm	5 μm	6 μm	5 μm
$V_{\mathrm{on}(1\,\mu A)}$[b]	30.30 V	30.40 V	30.35 V	30.45 V	30.35 V
Turn-on resistance[c] (Ω)	13.2	8.9	6.5	8.7	9.5

[a]Limited by the ESD testing equipment.
[b]The d.c. turn-on voltage measured at the 1 μA initially conducting current.
[c]Measured the slope of I–V curves between $I = 10$ and 20 mA.

testing with the +/− polarities respect to both VDD and VSS(GND) nodes, respectively, for each lateral SCR device with a layout area as small as $42 \times 50\ \mu\mathrm{m}^2$. The ESD failure threshold is defined as the ESD voltage that causes the $V_{\mathrm{on}(1\,\mu A)}$ of the device under test shifting 50% from its original value which is measured before any ESD testing. The $V_{\mathrm{on}(1\,\mu A)}$ is the d.c. turn-on voltage measured at the 1 μA initial conducting current. The $V_{\mathrm{on}(1\,\mu A)}$ of the fabricated lateral SCR devices with different layout dimensions are listed in Table 2.

Some of the measured d.c. I–V characteristics of the lateral SCR device in the fabricated four-SCR ESD protection circuit are also listed in Table 2. The d.c. trigger voltage of the lateral SCR device is around 32.6–35.2 V with the different layout dimensions, and its $V_{\mathrm{on}(1\,\mu A)}$ is about 30.3–30.45 V. The turn-on resistance of the lateral SCR device measured by the I–V slope between $I = 10$ and 20 mA is in the range of 6.5–13.2 Ω. A photograph of the measured

d.c. I–V characteristics of the SCR$_3$ and SCR$_4$ devices seen from the input pad to the VSS(GND) node is shown in Fig. 12. Due to the same layout structure of each lateral SCR device in this protection circuit, the I–V characteristic of the SCR$_3$ device is symmetrical to that of the SCR$_4$ device as shown in Fig. 12. Therefore, the proposed ESD protection circuit has the same excellent ESD robustness against both positive and negative ESD stresses.

The ESD trigger voltage of the fabricated lateral SCR device is measured by directly applying a pulse-type voltage waveform with a fixed 5 ns rise time and a tunable pulse height across the anode to the cathode of the fabricated lateral SCR device as shown in Fig. 13. An oscilloscope is used to monitor the turn-on occurrence of the lateral SCR device under each pulse triggering with different peak voltages. If the applied voltage pulse can not trigger on the lateral SCR device, the voltage waveform of the applied pulse at the anode of the lateral SCR device does not degrade due to the high impedance in the OFF state of a lateral SCR device. On the contrary, the voltage waveform will be seriously degraded at the anode due to the low impedance in the latching state of the lateral SCR device if the applied voltage pulse triggers on the lateral SCR device. Using this direct method, the pulse-type ESD trigger voltage is
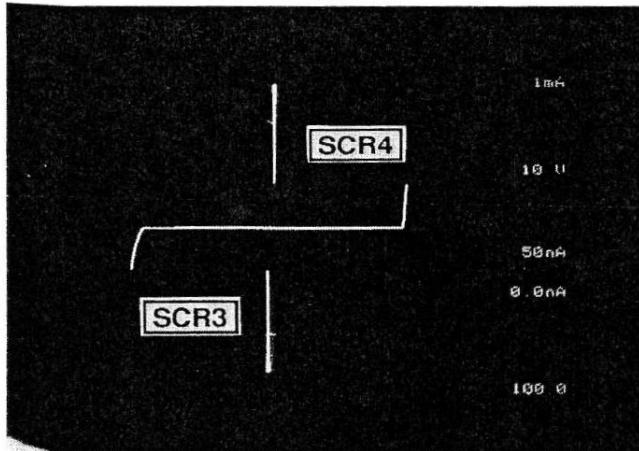

Fig. 12. A photograph of the measured d.c. I–V characteristics of the lateral SCR$_3$ and SCR$_4$ devices in the fabricated four-SCR ESD protection circuit, which is seen from the input pad to the VSS(GND) node. (Vertical scale: 1 mA/div.; horizontal scale: 10 V/div.)
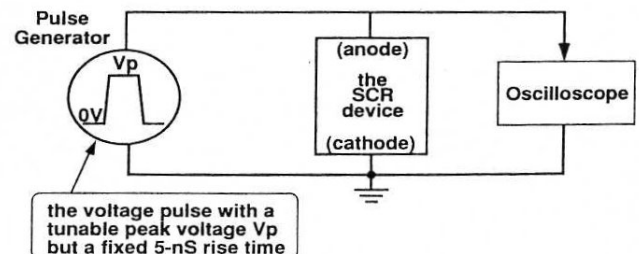

Fig. 13. The experimental set-up used to measure the trigger voltage of the fabricated lateral SCR device by directly applying a pulse-type voltage waveform with a fixed 5 ns rise time to the device under test.

measured and also listed in Table 2. It is found that the pulse-type ESD trigger voltages are from 5.54 to 11.3 V under the triggering condition of 5 ns rise time, depending on the different capacitance ratio in the fabricated lateral SCR device with different layout dimensions. With such a low ESD trigger voltage, the four-SCR ESD protection circuit can provide very efficient ESD protection not only against the HBM ESD stress but also against both MM and CDM ESD stresses.

As shown in Table 2, the pulse-type ESD trigger voltage of the lateral SCR device is much lower than its d.c.-type one. This verifies the effectiveness of the proposed design methodology to lower the ESD trigger voltage of a lateral SCR device. Generally, the appropriate trigger voltage of an ESD protection circuit must be less than the gate-oxide (drain) breakdown voltage of the internal circuits for input (output) protection but greater than the maximum voltage level of the normal input (output) signals.

5. CONCLUSION

A novel CMOS on-chip four-SCR ESD protection circuit with four parasitic lateral SCR devices has been successfully designed, fabricated, and tested. The test results of the fabricated protection circuits show that it can effectively perform excellent ESD protection within a smaller layout area than those of the conventional protection circuits. Through the proper design of device capacitances and resistances in the lateral SCR devices, the low ESD trigger voltage can be obtained without involving any device or junction breakdown. The ESD trigger voltage can also be adjusted to satisfy special design requirements. Without changing or adding any process step, this four-SCR ESD protection circuit is fully process compatible to the conventional or advanced CMOS and BiCMOS technologies in both the n-well and p-well processes. Moreover, the proposed ESD protection circuit can perform efficient ESD protection without the diffusion or polysilicon resistors so that the signal delay between I/O pad and internal circuits can be minimized. In view of these advantageous features, the proposed four-SCR ESD protection circuit is very suitable for high-speed and high-density sub-micron CMOS ICs.

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