Optimization of Guard Ring Structures to Improve Latchup Immunity in an 18 V DDDMOS Process

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***Abstract*— The optimization of guard ring structures to improve latchup immunity in an 18 V double-diffused drain MOS (DDDMOS) process with the DDDMOS transistors has together been investigated in a silicon test chip. The layout parameters including the anode-to-cathode spacing and the guard ring width are also studied to seek their impacts on latchup immunity. The measurement results demonstrated that the test devices isolated with the specific guard ring structure of n-buried layer can highly improve the latchup immunity. The suggested guard ring structures can be applied to the high-voltage circuits in this 18 V DDDMOS process to meet the new Joint Electron Device Engineering Council standard (JESD78D) with the trigger current of over ±200 mA.**

***Index Terms*— Double-diffused drain (DDD), latchup, n-buried layer (NBL).**

I. Introduction

SMART power technology, which can integrate both low-voltage (LV) and high-voltage (HV) devices in a single silicon chip, provides a cost-effective solution for high-voltage and high-current capabilities while increasing performance and reliability. When HV devices are used in HV CMOS ICs, the possible occurrence of latchup induced by external glitches or inductive load was difficult to eliminate [1], [2]. Latchup in CMOS ICs is formed by the parasitic p-n-p-n structure between V_{DD} and V_{SS} in CMOS circuits. Such a parasitic structure is inherent in the bulk CMOS technology. Fig. 1 shows the device cross-sectional view and equivalent circuit scheme of a latchup path between nMOS and pMOS transistors in a CMOS technology. The latchup structure is composed of a p-n-p BJT (Q_{pnp}) and a n-p-n BJT (Q_{npn}), and the positive feedback regeneration will start when one of the BJTs is turned ON [3]. Due to the high circuit operating voltage and structure complexity in HV CMOS ICs, latchup in the HV structure usually suffers worse situation in comparison with that in LV CMOS ICs. When latchup is triggered, HV CMOS ICs are often seriously damaged by the latchup-generated high power. Therefore, improving the latchup immunity is one of major reliability issues in HV CMOS ICs.

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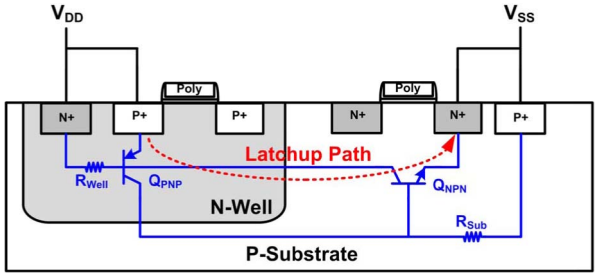

Fig. 1. Device cross-sectional view of the latchup path between nMOS and pMOS transistors in a CMOS technology.

TABLE I
TRIGGER CHARACTERIZATION IN LATCHUP CURRENT TEST [4]

Latchup I-test	Stress Range	Force Current
Positive I-Test	I	< 50 mA
	II	50 to < 100 mA
	III	100 to < 150 mA
	IV	150 to < 200 mA
	V	>= 200 mA
Negative I-Test	I	> -50 mA
	II	-50 mA to > -100 mA
	III	-100 to > -150 mA
	IV	-150 to > -200 mA
	V	< -200 mA

The methods and test procedures to investigate the latchup immunity of integrated circuits with a latchup trigger current test (I-test) had been defined in the Joint Electron Device Engineering Council (JEDEC) standards [4]. The trigger characterization for the latchup I-test in the up-to-dated standard (JESD78D) is listed in Table I, where the highest latchup I-test level has been specified to be of greater than 200 mA. Accordingly, nowadays many IC design houses develop their IC products with a latchup immunity of over ±200-mA current trigger as their desired specification.

To suppress the occurrence of latchup event, many techniques had been reported using process optimization [5], [6], layout structure [7]–[10], or even active guard ring design [11]. Among the previous studies, inserting the double guard rings with grounded p-well ring and V_{DD}-connected n-well ring inside the latchup path to absorb minority carriers is one of the most effective designs. However, there were a few studies to investigate the influence of guard ring structures of the double-diffused drain MOS (DDDMOS) device and their layout parameters on latchup immunity in the HV DDDMOS technology. This HV DDDMOS technology features multiple voltage levels with various types of devices such as CMOS,

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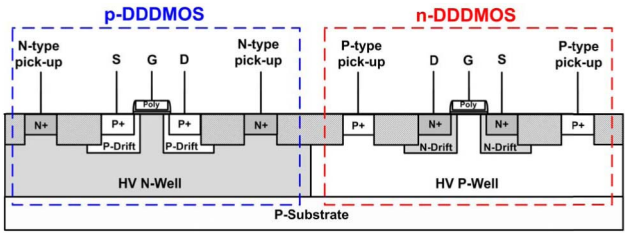

Fig. 2. Device structures of p-type and n-type DDDMOS transistors in an 18 V DDDMOS technology.

DDDMOS, and BJT devices. The n-type and p-type well structures with different doping levels and junction depths in this process would greatly influence the latchup occurrence.

In this paper, the latchup characteristics of DDDMOS transistors with the different guard ring structures under JEDEC latchup current test are investigated in silicon. In addition, layout parameters such as the anode-to-cathode spacing and the guard ring width (GW) are also studied to find their impacts on latchup immunity. In order to verify the holding voltage of HV latchup test structures, the dc curve tracer (Tek370B) is also used. It is demonstrated that the test devices isolated with the specific guard ring structure of n-buried layer (NBL) and double-diffused layer can highly improve the latchup immunity.

II. Test Device Structures

The devices studied in this paper are implemented in an 18 V DDDMOS technology. The device structures of p-type and n-type DDDMOS transistors are shown in Fig. 2, where the drift regions under both drain and source sides of each device are used to increase the junction breakdown voltage to sustain high operating voltage. In HV ICs, the latchup path in I/O cells was often triggered by external overshooting or undershooting voltage/current glitches. In this paper, the optimization of layout rules and guard ring structures is investigated to improve latchup immunity in an inverter output buffer. The proposed test structures are drawn with the p-type and n-type DDDMOS transistors, as illustrated in Fig. 3, where the latchup path exists from the V_{DD}-connected source of the pDDDMOS, through the HV n-well and HV p-well, to the V_{SS}-connected source of the nDDDMOS. The channels of both DDDMOS devices are kept in OFF state by connecting its gate to its source for studying the influence of layout structure on latchup.

Fig. 4(a)–(d) shows the cross-sectional view of different guard-ring test structures of types A, B, C, and D, respectively. To get better latchup immunity, all the test transistors are surrounded by guard rings. Test structure A consists of a pair of pDDDMOS and nDDDMOS. Each transistor is surrounded by only one guard ring, which is the base guard ring of each transistor. This structure is used as a reference structure for comparing with other test structures. Test structure B consists of the transistor pair that each transistor is surrounded by double guard rings. The second guard ring, which encircles the first guard ring of each transistor, is used to collect the minority carriers in the p-substrate. Test structure C consists of the transistor pair surrounded by double guard rings, but an

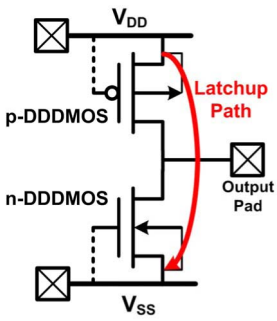

Fig. 3. Circuit scheme of the proposed test structure with p-type and n-type DDDMOS transistors, which is used to simulate an inverter output buffer in the I/O cell. For latchup test, both transistors are kept OFF.

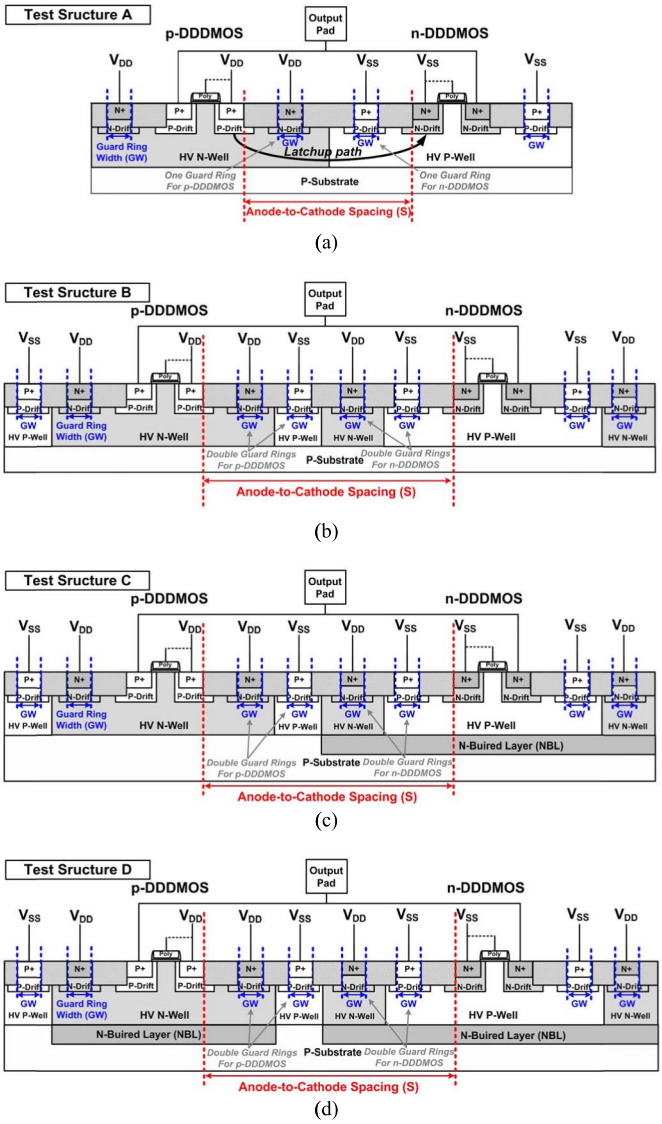

Fig. 4. Device cross-sectional views of the proposed latchup test structures (a) A, (b) B, (c) C, and (d) D, with a pair of pDDDMOS and nDDDMOS transistors in each test structure.

NBL is added under nDDDMOS. Test structure D consists of the transistor pair surrounded by double guard rings with two NBL layers added under the pDDDMOS and the n-DDDMOS, respectively.

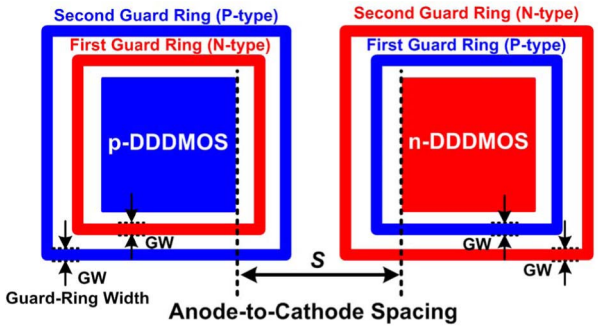

Fig. 5. Simplified layout top view of latchup test unit for test structures A–D.

Compared with test structures A and B, the nDDDMOS in test structures C and D is totally isolated from the p-substrate. The NBL structure is used to further improve the guard ring efficiency. In addition, some layout parameters such as the anode-to-cathode spacing (S) and the GW are investigated. The improvement obtained by adding double-diffused regions (n-drift or p-drift layers) under the guard rings are also studied. The simplified layout top views of latchup test unit for test structures A, B, C, and D are shown in Fig. 5, indicating the related layout parameters.

III. Experimental Results

A. Latchup I–V Characteristics

To investigate the latchup characteristics of the proposed test structures, the latchup dc I–V curves are measured by a Tek370B curve tracer. All the test results are measured at a room temperature of 25 °C. If the holding voltage of these test structures is greater than V_{DD}, the latchup occurrence can be avoided. The I–V characteristics traced from V_{DD} to V_{SS} of the test structures with a minimum anode-to-cathode spacing of 13.4 μm and a guard ring width of 1 μm are shown in Fig. 6(a), where the holding voltage of all those test structures is below 5 V. It implies that the latchup paths in test structures C and D will be still induced even with the NBL to isolate the devices. As shown in Fig. 6(b), when the anode-to-cathode spacing is increased to 20 μm, the trigger voltage and holding voltage of all test structures are increased slightly. As shown in Fig. 6(c), when the anode-to-cathode spacing is increased to 30 μm, the trigger voltage and holding voltage of all test structures are moderately increased, but the holding voltage is still lower than the operating voltage V_{DD} of 18 V in the given process. Even extending the GW to 3 μm, the holding voltage of all test structures is still lower than the operating voltage of 18 V.

Among the test structures, test structure D has the highest dc trigger (the switching point) current and test structure A has the lowest one. A higher trigger current means better latchup immunity, which can be further verified in the JEDEC latchup trigger current test.

B. Latchup Trigger Current Test

Because the holding voltage of test structures is all smaller than the operating voltage V_{DD} of 18 V in the given process,

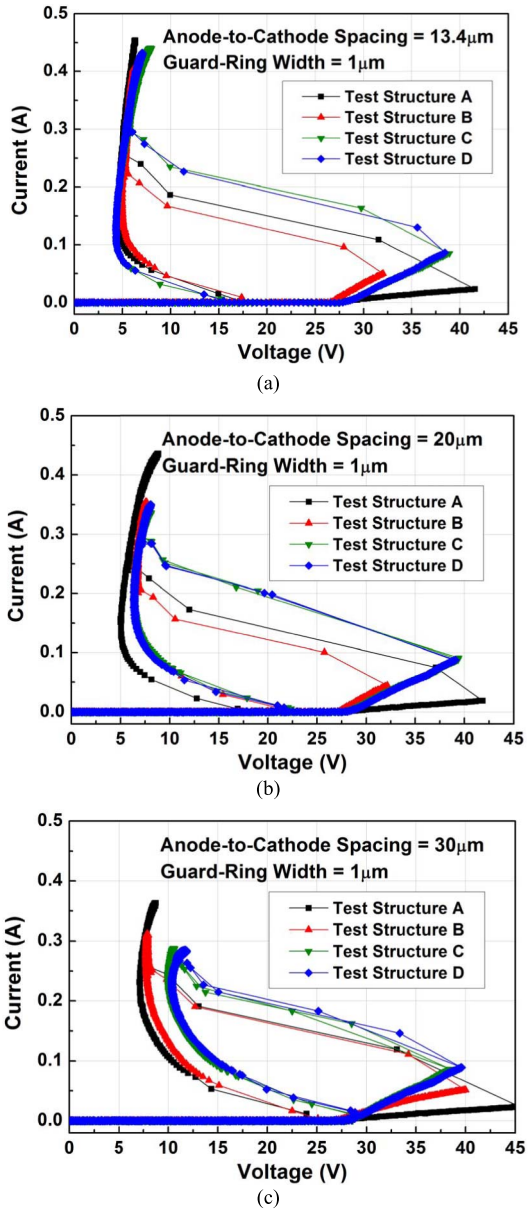

Fig. 6. Latchup I–V characteristics of different test structures from V_{DD} to V_{SS} with different anode-to-cathode spacings of (a) 13.4, (b) 20, and (c) 30 μm, respectively, under the same guard ring width of 1 μm.

another way to verify their latchup immunity is using the latchup trigger current test as that specified in the JEDEC standard (JESD78D). The measurement setup of JEDEC latchup trigger current test applied to the output buffer is exploited in Fig. 7, with an 18 V supply at V_{DD} pin, a current pulse generator applied to the output pin, and an oscilloscope to monitor the waveforms of the V_{DD} pin voltage and the injected current. The positive or negative trigger current pulse from the pulse generator is injected into the output pin of the test structure to investigate whether the latchup is triggered ON or not. If the test structure is triggered into latchup, a decrease on the voltage waveform of V_{DD} pin can be found to judge the occurrence of latchup.

The measured waveforms of test structure A with the anode-to-cathode spacing of 13.4 μm and the guard ring

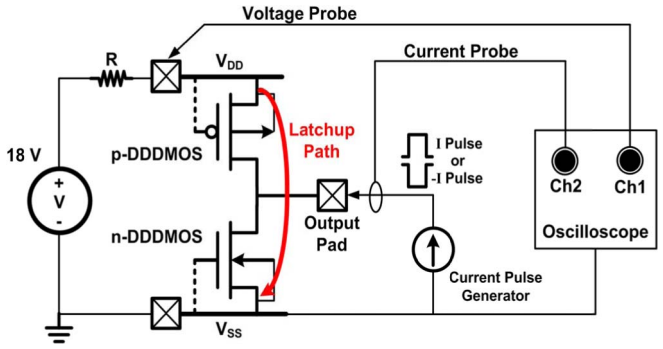

Fig. 7. Latchup test for test structures with the positive or negative latchup trigger current at each output pad.

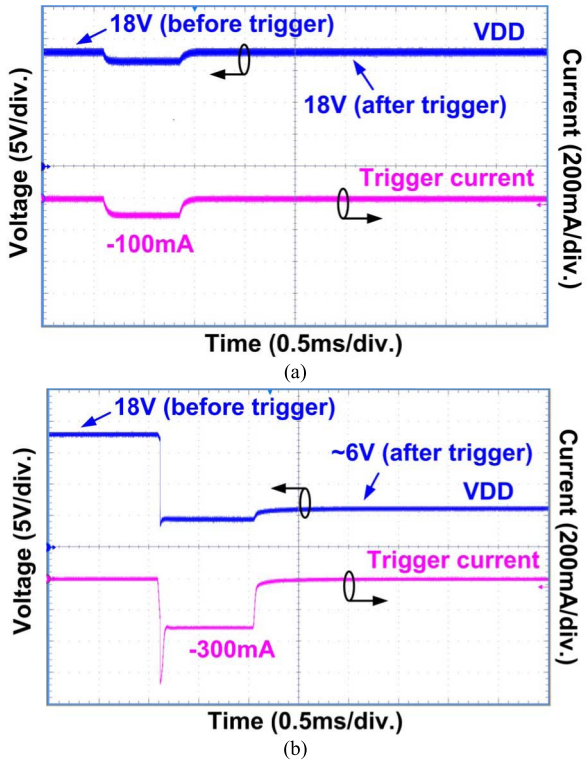

Fig. 8. Measured waveforms of test structure A under negative latchup trigger current test with the trigger currents of (a) −100 mA and (b) −300 mA, injected into the output pad.

width of 1 μm, under the negative trigger current test with trigger current pulses of −100 and −300 mA, are shown in Fig. 8(a) and (b), respectively. To avoid electrical overstress events and to successfully detect the fired latchup state of the test structure, the pulse width is chosen as 1 ms, and the pulse step is 100 mA.

The voltage at V_{DD} pin is kept at 18 V if the applied trigger current at the output pad did not fire on the latchup path of the test structure, as shown in Fig. 8(a). However, the voltage at V_{DD} pin is dropped down to ∼6 V while the latchup path is triggered ON, as that shown in Fig. 8(b). The initial undershooting glitch in the negative trigger current waveform is caused by the current compensation in the current pulse generator, which can be ignored. Thus, by adjusting the trigger current level with repeated experimental procedures,

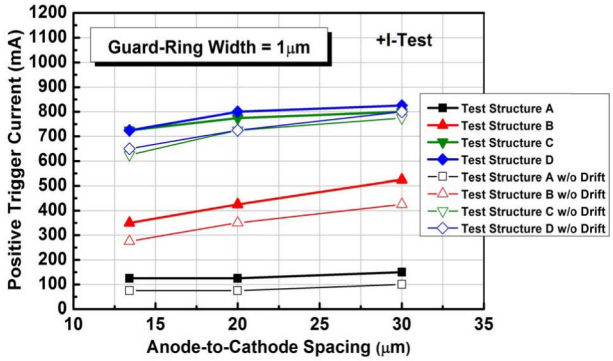

Fig. 9. Relations between the positive latchup trigger current on output pad and the anode-to-cathode spacings of 13.4, 20, and 30 μm for different test structures, test structures A, B, C, and D, under the same guard ring width of 1 μm.

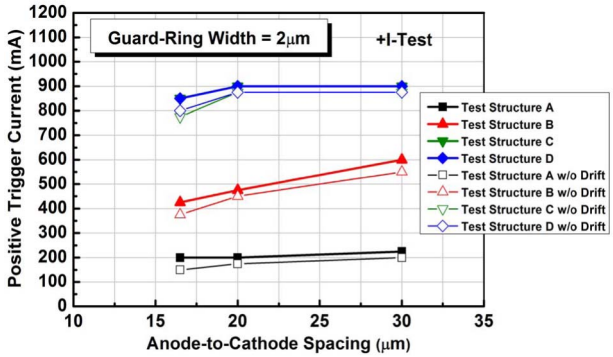

Fig. 10. Relations between the positive latchup trigger current on output pad and the anode-to-cathode spacings of 16.5, 20, and 30 μm for different test structures, test structures A, B, C, and D, under the same GW of 2 μm.

the threshold level of trigger current to initiate a latchup occurrence can be found.

Furthermore, more detailed examinations to verify the latchup immunity are measured using a latchup test machine, Thermo Scientific MK.1, with a 10-ms pulse width and a 25-mA pulse step. Fig. 9 shows the measured relations between the positive latchup trigger current and the different anode-to-cathode spacings of 13.4, 20, and 30 μm for different test structures but with the same GW of 1 μm. In Fig. 9, the test structure without drift means that the drift layers are not added under the guard rings in the test structure. The latchup trigger currents of all test structures are moderately increased by the increase in anode-to-cathode spacing. Among the test results of different test structures with the same anode-to-cathode spacing, test structure A has the lowest latchup trigger current below 150 mA, because the devices in structure A are surrounded only by the base guard rings. Test structure B has a higher latchup trigger current than that of test structure A due to the use of the double guard rings. Using the double guard rings as well as the NBL to isolate the devices, test structures C and D have almost the same latchup trigger current of above 600 mA and exhibit the highest current level among the test structures. In addition, the drift layers under the guard rings can increase the latchup trigger current by at

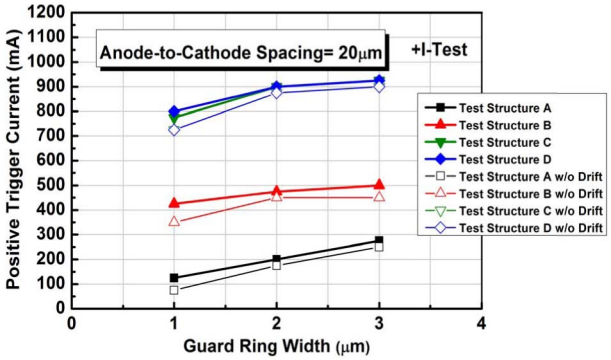

Fig. 11. Relations between the positive latchup trigger current on output pad and the guard ring widths of 1, 2, and 3 μm for different test structures, test structures A, B, C, and D, under the same anode-to-cathode spacing of 20 μm.

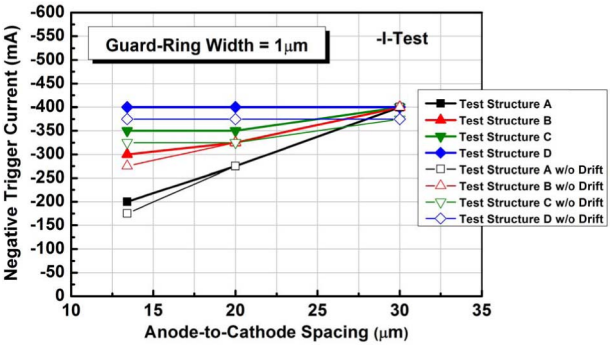

Fig. 12. Relations between the negative latchup trigger current on output pad and the anode-to-cathode spacings of 13.4, 20, and 30 μm for different test structures, test structures A, B, C, and D, under the same GW of 1 μm.

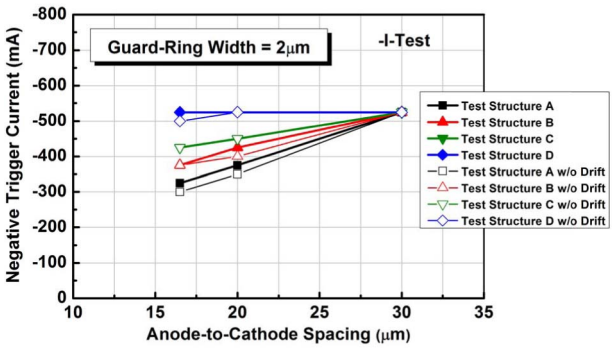

Fig. 13. Relations between the negative latchup trigger current on output pad and the anode-to-cathode spacings of 16.5, 20, and 30 μm for different test structures, test structures A, B, C, and D, under the same guard ring width of 2 μm.

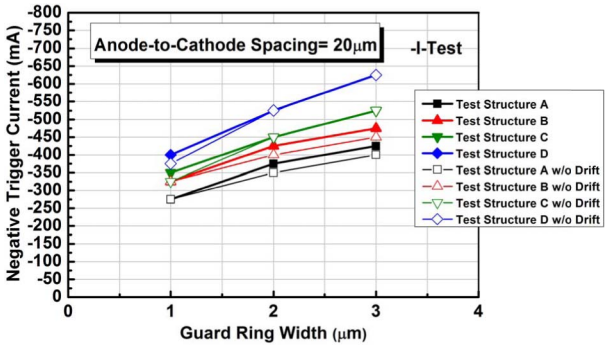

Fig. 14. Relations between the negative latchup trigger current on output pad and the GWs of 1, 2, and 3 μm for different test structures, test structures A, B, C, and D, under the same anode-to-cathode spacing of 20 μm.

least 25 mA, compared with the results of those structures without drift layers. As for the measured results in Fig. 9, test structure D can sustain the positive latchup trigger current of over 800 mA, when its anode-to-cathode spacing is 30 μm.

Fig. 10 shows the measured relations of different test structures between the positive latchup trigger current and the different anode-to-cathode spacings of 16.5, 20, and 30 μm under the same GW of 2 μm. The positive latchup trigger currents of all test structures are moderately increased by the increase in the anode-to-cathode spacing. Fig. 11 shows the measured relations of different test structures between the positive latchup trigger current and the different guard ring widths of 1, 2, and 3 μm under the same anode-to-cathode spacing of 20 μm. For test structure A, the increased guard ring width can improve the positive current level greatly. However, for test structures B, C, and D, the current level can only be improved slightly by the increased GW. From the comparison of test results between test structures B and C, the guard ring efficiency in nDDDMOS can be greatly improved using the NBL layer. That is, adding NBL under the n-type device can greatly improve the latchup immunity in the positive latchup trigger current test. As for the measured results in Fig. 11, test structure D with a guard ring width of 3 μm and the anode-to-cathode spacing of 20 μm can sustain the positive latchup trigger current of up to 900 mA.

Similarly, the latchup immunity under negative latchup trigger current test can be also observed. Figs. 12 and 13 show the measured relations between the negative latchup trigger current and the different test structures under the different guard ring widths of 1 and 2 μm, respectively. Fig. 14 shows the measured relations of different test structures between the negative latchup trigger current and the different GWs under the same anode-to-cathode spacing of 20 μm. The latchup trigger current of all test structures can be increased by an increased guard ring width and the added drift layers, as the measured results in the positive trigger current test. For test structures A–C, the negative latchup trigger current can be greatly increased by the increase in the anode-to-cathode spacing. Nevertheless, for test structure D, although it has the highest current level, increasing the anode-to-cathode spacing has no improvement on latchup immunity under negative latchup trigger test. It was suspected that the latchup path in test structure D from the V_{DD}-connected source of pDDDMOS to the V_{SS}-connected source of nDDDMOS was not fired. This phenomenon can be further investigated by failure analysis.

Compared with test structure C, test structure D has much higher negative latchup trigger current (over -600 mA, as shown in Fig. 14). The guard ring efficiency in pDDDMOS can be greatly improved using the NBL. Adding the NBL under the p-type device can greatly improve the latchup robustness in the negative latchup trigger current test.

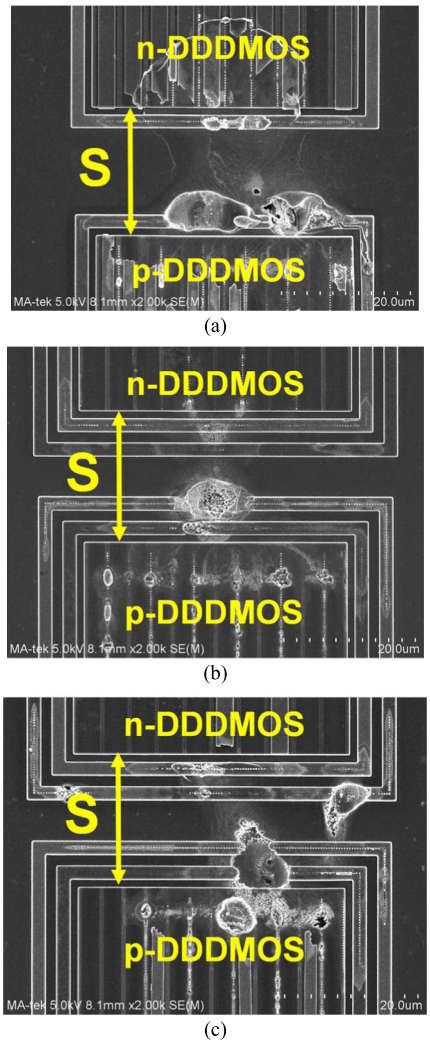

Fig. 15. SEM photographs of (a) test structure A, (b) test structure B, and (c) test structure D, to show the latchup-induced damage after the injection of negative latchup trigger current, under the same GW of 2 μm and anode-to-cathode spacing (S) of 20 μm.

C. Failure Analysis

Fig. 15(a)–(c) shows the SEM photographs of test structures A, B, and D, respectively, with the latchup-induced damage after the injection of negative latchup trigger current under the same layout parameters. It is obviously found that test structure D got damaged in the both regions of pDDDMOS and nDDDMOS with the burn-out traces between these two devices, as shown in the results of test structures A and B. Accordingly, the failure analysis verified that the latchup path indeed occurred in test structure D to induce damage.

IV. Conclusion

The characteristics of HV latchup have been investigated in an 18 V DDDMOS process. Four test structures are used to evaluate the latchup immunity of HV device structures. Among the test structures, test structure D can exhibit the highest latchup immunity against the negative and positive latchup trigger current because of the highest guard ring efficiency. Using the NBL-based isolation structure can not only gain good latchup immunity but also save the layout area of HV output buffers without extending the distance between the p-type and n-type MOS devices. Furthermore, the drift layers can be also applied to optimize the guard ring structure for better latchup prevention in HV CMOS ICs.

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References

[1] S. H. Voldman, *Latchup*. Hoboken, NJ, USA: Wiley, 2007.
[2] M.-D. Ker and S.-F. Hsu, *Transient-Induced Latchup in CMOS Integrated Circuits*. New York, NY, USA: Wiley, 2009.
[3] M.-D. Ker and C.-Y. Wu, "Modeling the positive-feedback regenerative process of CMOS latchup by a positive transient pole method—Part I: Theoretical derivation," *IEEE Trans. Electron Devices*, vol. 42, no. 6, pp. 1141–1148, Jun. 1995.
[4] *IC Latch-Up Test*, JEDEC Solid State Technology Association, JEDEC Standard JESD78D, 2011.
[5] S. Voldman *et al.*, "The influence of a silicon dioxide-filled trench isolation structure and implanted sub-collector on latchup robustness," in *Proc. 43rd IRPS*, 2005, pp. 112–120.
[6] S. H. Voldman, "The influence of a novel contacted polysilicon-filled deep trench (DT) biased structure and its voltage bias state on CMOS latchup," in *Proc. 44th IRPS*, 2006, pp. 151–158.
[7] S. Gupta, J. C. Beckman, and S. L. Kosier, "Improved latch-up immunity in junction-isolated smart power ICs with unbiased guard ring," *IEEE Electron Device Lett.*, vol. 22, no. 12, pp. 600–602, Dec. 2001.
[8] M.-D. Ker and W.-Y. Lo, "Methodology on extracting compact layout rules for latchup prevention in deep-submicron bulk CMOS technology," *IEEE Trans. Semicond. Manuf.*, vol. 16, no. 2, pp. 319–334, May 2003.
[9] S.-F. Hsu and M.-D. Ker, "Dependence of device structures on latchup immunity in a high-voltage 40-V CMOS process with drain-extended MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 4, pp. 840–851, Apr. 2007.
[10] J.-W. Lee, Y.-F. Chang, C.-W. Hsu, T.-C. Tsai, W.-Y. Lin, and M. H. Song, "Novel isolation ring structure for latch-up and power efficiency improvement of smart power IC's," in *Proc. 35th EOS/ESD Symp.*, 2013, pp. 1–5.
[11] H.-W. Tsai and M.-D. Ker, "Active guard ring to improve latch-up immunity," *IEEE Trans. Electron Devices*, vol. 61, no. 12, pp. 4145–4152, Dec. 2014.

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