# Investigation of Unexpected Latchup Path Between HV-LDMOS and LV-CMOS in a 0.25-$\mu$m 60-V/5-V BCD Technology

Chia-Tsen Dai and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*— The latchup path which may potentially exist at the interface between high-voltage (HV) and low-voltage (LV) circuits in a HV bipolar-CMOS-DMOS (BCD) technology is investigated in this brief. Owing to multiple well structures used to realize the HV device in the BCD process, the expected latchup path in the test structure was hardly triggered. However, a parasitic silicon-controlled rectifier path featuring a very low holding voltage is found in the experimental silicon chip. Such a parasitic path is first reported in the literature. It may influence the electrostatic discharge robustness of CMOS IC products with the HV and LV circuits integrated together. Thus, the layout rules at the HV and LV interface should be carefully defined to avoid the occurrence of an unexpected parasitic path.**

***Index Terms*— Electrostatic discharge (ESD), latchup, silicon-controlled rectifier (SCR).**

## I. Introduction

WHEN high-voltage (HV) transistors are widely used in HV ICs or power ICs, the possible occurrence of latchup induced by the external glitches or inductive load is difficult to eliminate [1], [2]. Latchup in CMOS ICs is formed by the parasitic silicon-controlled rectifier (SCR) structure between $V_{DD}$ and $V_{SS}$ in CMOS circuits. Such a parasitic structure is inherent in the bulk CMOS technology. Due to the high circuit-operating voltage and structure complexity of HV devices, HV CMOS ICs would be seriously damaged by the latchup-generated high power if latchup was triggered. Therefore, improving the latchup immunity is one of the major reliability issues in HV CMOS ICs. Adding well pickups and inserting double guard rings in the latchup path are the most traditional solutions. In addition, latchup prevention had been reported by using process modification, layout optimization, or even circuit of active guard ring [3]–[8]. The methods and test procedures to investigate the latchup immunity of integrated circuits with a current-trigger latchup test had been defined in the Joint Electron Device Engineering Council (JEDEC) standards [9]. The specification of latchup immunity level for the current-trigger latchup test in the up-to-date standard (JESD78E) has been specified to be greater than 100 mA.

With the integration of both HV and low-voltage (LV) devices in the same chip, the voltage levels of the HV domain are often significantly above the voltage levels of the LV domain. There have been some related studies on the latchup failures between different power domains [10], [11]. Therefore, solutions are strongly needed to avoid latchup risk at the HV and LV interface in CMOS IC products. In this brief, the characteristic of a potential latchup path between HV lateral double-diffused MOS (LDMOS) and LV CMOS transistors is investigated in a HV bipolar-CMOS-DMOS (BCD) technology. In order to verify the holding voltage ($V_h$) of the latchup path, the dc curve tracer (Tek370B) is used [12]. A parasitic SCR path is found in the experimental silicon chip that was fabricated by the 60-V BCD technology. The current-trigger latchup test is further used to investigate the characteristics of the parasitic paths between these HV and LV devices.

Manuscript received June 2, 2017; accepted June 18, 2017. Date of publication July 3, 2017; date of current version July 21, 2017. This work was supported by the Ministry of Science and Technology (MOST), Taiwan, under Contract MOST 105-2221-E-009-166 and Contract MOST 106-2622-8-009-007-TE1. The review of this brief was arranged by Editor F. Udrea. *(Corresponding author: Ming-Dou Ker.)*

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Digital Object Identifier 10.1109/TED.2017.2717970

## II. Test Structures

The test structure studied in this paper is implemented in a 0.25-$\mu$m 5-V/60-V BCD technology. The device structures of 60-V p-type lateral double-diffused MOS (pLDMOS) and 5-V pMOS transistors are shown in Fig. 1. A potential latchup path is expected from the $V_{DDH}$-connected source of pLDMOS, through HV n-body, HV p-well, HV n-well, and p-substrate, to the $V_{DDL}$-connected n-well pickup of LV-pMOS. The simplified circuit scheme of the test structure is illustrated in Fig. 2. For studying the influence of layout structure on latchup, the channels of both devices are kept in OFF-state by connecting each device's gate to its own source. The distance of the expected latchup path is 30 $\mu$m in the silicon chip. Both devices are drawn with a channel width of 50 $\mu$m. $V_{Trigger}$ pin will be used in the current-trigger latchup test.

## III. Experimental Results

### A. DC I–V Characteristics

To investigate the latchup characteristics of the test structure, the latchup dc $I$–$V$ curves are measured by Tek370B

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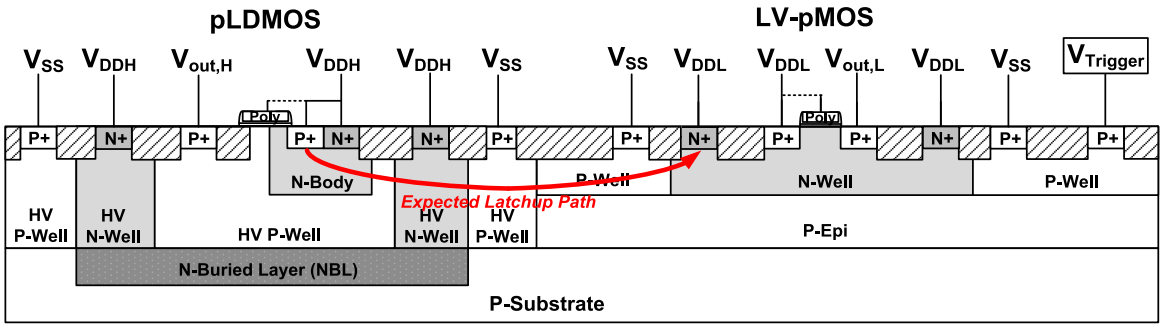


Fig. 1. Device structures of 60-V pLDMOS and 5-V LV-pMOS in the HV BCD technology. The expected potential latchup path is designated.

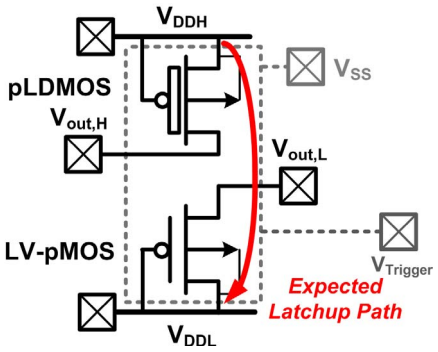


Fig. 2. Circuit scheme to show the possible latchup path in the test structure with 60-V pLDMOS and 5-V LV-pMOS.

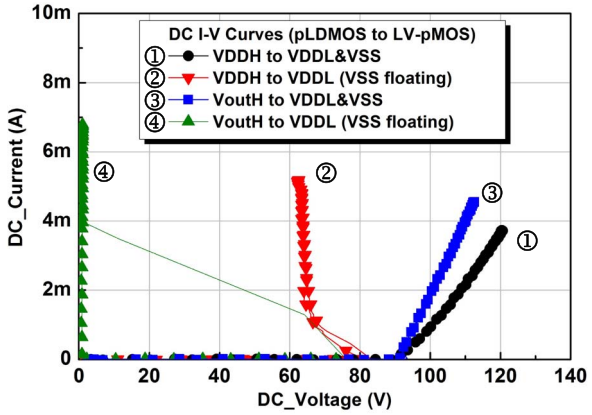


Fig. 3. *I–V* characteristics of the proposed test structure measured by a dc curve tracer.

curve tracer under a room temperature of 25 °C. Fig. 3 shows the dc $I$–$V$ characteristics traced between pLDMOS and LV-pMOS under different parasitic paths. Curve 1 is traced from $V_{DDH}$ to $V_{DDL}$ with $V_{SS}$ grounded. The trigger voltage ($V_{t1}$) is up to 80 V, but no snapback phenomenon is found. To further study the characteristic of this path, curve 2 is traced from $V_{DDH}$ to $V_{DDL}$ while $V_{SS}$ is floating. As shown in Fig. 3, a snapback curve can be detected with a $V_h$ of ~60 V. On the other hand, a parasitic path, which is from the $V_{OUT,H}$ of pLDMOS, through HV n-well and p-substrate, to the $V_{DDL}$-connected n-well pickup of LV-pMOS, is also measured. Curve 3 is traced from $V_{OUT,H}$ to $V_{DDL}$ with $V_{SS}$ grounded. The $V_{t1}$ of this path is also up to 80 V with no snapback phenomenon. However, when $V_{SS}$ is floating, different from the result of curve 3, curve 4 shows a strong snapback behavior with $V_h$ of only ~1 V.

In the test results of curves 1 and 2, the path from $V_{DDH}$ to $V_{DDL}$ is formed with a six-layer p-n-p-n-p-n path due to the multiple well structures in pLDMOS. Thus, it will lead this path to have a high $V_h$. In the test results of curves 3 and 4, the path from $V_{OUT,H}$ to $V_{DDL}$ is formed with a traditional four-layer p-n-p-n SCR path, so a strong snapback curve is distinctly found. In addition, the test results with $V_{SS}$ grounded are different from the ones without $V_{SS}$ grounded. The reason is that $V_{SS}$ node can collect holes in p-substrate and hence restrict the conduction of n-p-n bipolar junction transistor (BJT) in the parasitic SCR path.

## B. Current-Trigger Latchup Test

To verify the latchup immunity, the current-trigger latchup test specified in the JEDEC standard (JESD78E) is used. The measurement setup of JEDEC latchup test applied to the test structure is shown in Fig. 4(a), with a 60-V dc supply at $V_{DDH}$ pin, $V_{DDL}$ pin grounded, a current pulse generator applied to the $V_{Trigger}$ pin, and an oscilloscope to monitor the waveforms of the $V_{DDH}$ pin voltage and the injected current pulse. The trigger current pulse with a pulsewidth of 10 ms injected into $V_{Trigger}$ pin is to simulate a transient noise penetrating into the p-substrate within HV and LV devices to induce latchup. If the test structure is triggered into latchup, a decrease on the voltage waveform of $V_{DDH}$ pin can be found to judge the occurrence of latchup. After the transient triggering, no clamped voltage roll-off and no latchup state can be detected even with $V_{SS}$ floating. It is due to the high $V_h$ measured by the dc curve tracer in the expected latchup path. To verify the $V_h$ of this path, the latchup trigger measurement is tested again with the dc supply voltage raised to 70 V. Fig. 4(b) shows the measured time-domain waveforms after the transient triggering of 10-mA current pulse injection. This path clamped the supply voltage to ~60 V, which is the same value of $V_h$ under dc curve tracer measurement. A higher $V_h$ means a better latchup immunity. It implies that the latchup issue at the HV and LV interface can barely happen if HV device features such complex well structures.

Furthermore, the parasitic SCR path from the $V_{OUT,H}$ pin of the 60-V pLDMOS to the $V_{DDL}$ pin of 5-V LV-pMOS is also

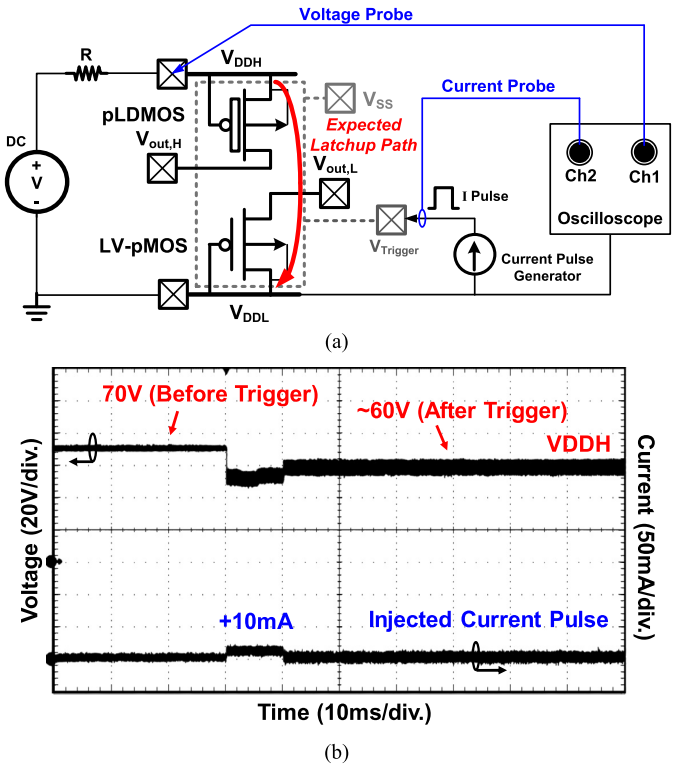


Fig. 4. (a) Latchup measurement on the expected latchup path of the test structure with the positive 10-mA current pulse applied to the $V_{Trigger}$ pad. (b) Measured time-domain voltage and current waveforms on the test structure.

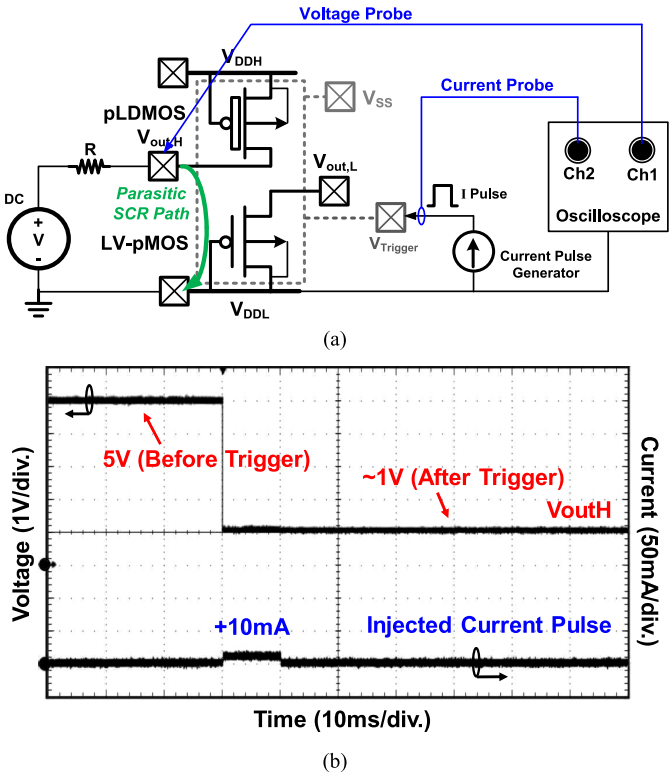


Fig. 5. (a) Transient triggering measurement on the parasitic SCR path of the test structure with the positive 10-mA current pulse applied to the $V_{Trigger}$ pad. (b) Measured time-domain voltage and current waveforms on the test structure.

measured by the current-trigger latchup test. The measurement setup is shown in Fig. 5(a), with a 5-V dc supply at $V_{OUT,H}$ pin, $V_{DDL}$ pin grounded, $V_{SS}$ pin floating, and a current pulse injection into $V_{Trigger}$ pin. From the measured voltage waveform in Fig. 5(b), this path clamped the supply voltage to ~1 V, which is the same value of $V_h$ under dc curve tracer measurement. In consequence, the transient triggering test has verified that this parasitic SCR path can be successfully induced into snapback state.

### C. Impact on ESD Protection

This parasitic SCR path may cause the unexpected electrostatic discharge (ESD) current discharging path across the HV/LV interface of the ICs to degrade the ESD robustness of IC products. A typical on-chip ESD protection design with HV and LV power rail ESD clamp circuits in a CMOS IC with different power domains is depicted in Fig. 6. If an ESD stress zaps from the output pin of the HV domain to the $V_{DDL}$ pin of the LV domain, the conduction path of ESD current ($I_{ESD}$) is generally designed to discharge through the body diode of pLDMOS to the floating $V_{DDH}$ line, then through the HV power-rail ESD clamp circuit to the floating $V_{SS}$ lines, and then through the parasitic diode inherent in the LV power-rail ESD clamp circuit to the grounded $V_{DDL}$ line, as the blue line indicates in Fig. 6. The sum of the different voltage drops along this conduction path can be approximately expressed as

$$V_{IESD} \cong V_{Diode,\,pLDMOS} + V_{HV\_Clamp} + V_{Diode,VSS} + V_{LV\_Clamp} \quad (1)$$

where $V_{Diode,pLDMOS}$ and $V_{Diode,VSS}$ are the voltage drops of the body diode of pLDMOS and the bidirectional diodes between $V_{SSH}$ and $V_{SSL}$ ground lines, and $V_{HV\_Clamp}$ and $V_{LV\_Clamp}$ are the conduction voltage drops of HV and LV power-rail ESD clamp circuits.

However, if the layout spacing between HV and LV p-type devices is too close, the $V_h$ of the parasitic SCR path (shown by the green dashed line in Fig. 6) can be lower than the voltage drop of the conduction path in (1), and hence it will divert the ESD current when triggered ON. An unexpected failure might happen to degrade the ESD robustness, if the device dimension of this parasitic SCR between the HV and LV p-type devices was not large enough to sustain the desired ESD level.

There are two recommended ways to prevent the unexpected failure between different power domains. The first way is to simply extend the layout spacing between HV and LV devices to increase the $V_h$ of the parasitic path, and even insert double guard rings within the parasitic path for reducing the current gains of the parasitic BJTs, as depicted in Fig. 7.

On the contrary, the second way is to utilize the parasitic path to improve the ESD robustness. The device dimensions of the adjacent HV and LV p-type devices can be appropriately enlarged to ensure the ESD robustness of this parasitic path. The transmission-line-pulsing (TLP) system is used to

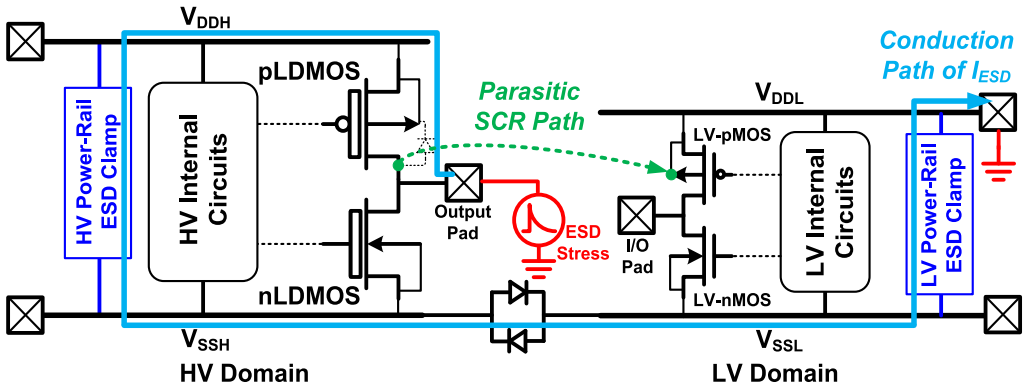


Fig. 6. ESD protection design with HV and LV power-rail ESD clamp circuits in a CMOS IC with different power domains.

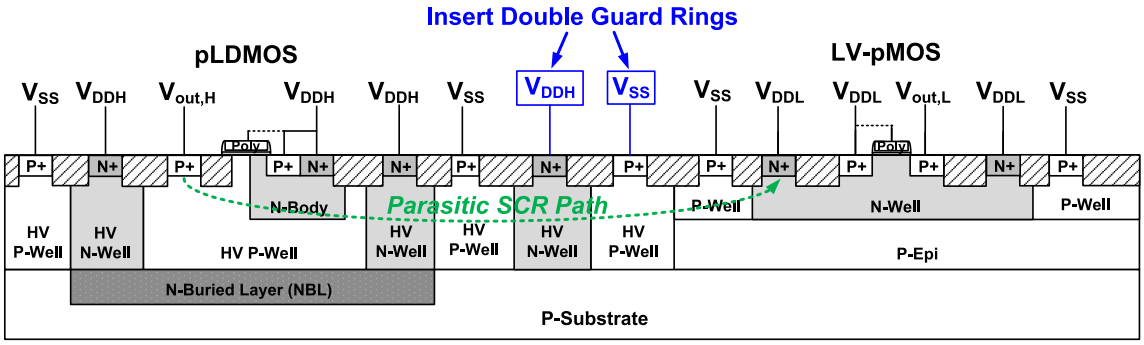


Fig. 7. Parasitic SCR path between HV and LV p-type devices in a HV BCD technology with inserted double guard rings.

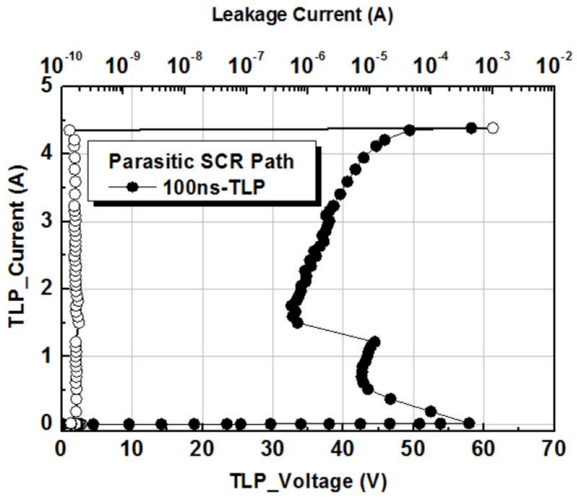


Fig. 8. TLP-measured $I$–$V$ curve of the parasitic SCR path between 60-V pLDMOS and 5-V pMOS devices. (Channel widths for both 60-V pLDMOS and 5-V pMOS devices are 50 $\mu$m.)

investigate the characteristic of the parasitic SCR path in this test structure.

The TLP-measured $I$–$V$ curve of this parasitic SCR path is shown in Fig. 8. The TLP-measured $V_h$ is ~30 V, which is much higher than that in the dc-measured result. Such voltage difference is due to the increased current gain induced by the Joule heating effect in the dc measurement [12]. In addition, the TLP-measured failure current ($I_{t2}$) of this parasitic SCR path is ~4.4 A. With a channel width of 50 $\mu$m for both 60-V pLDMOS and 5-V pMOS devices fabricated in this test structure, the $I_{t2}$ per width is calculated as ~0.088 A/$\mu$m. It can be applied to predict the ESD robustness of this parasitic SCR path.

## IV. Conclusion

The characteristics of the parasitic paths between the HV and LV devices in the test structure have been investigated in a HV BCD technology. It is found that the $V_h$ of the expected latchup path measured by a curve tracer is greater than 60 V. Through experimental verification by using the current-trigger latchup test, this expected latchup path is hardly induced. However, an unexpected parasitic SCR path has been found in the silicon chip. Transient triggering measurement has further verified that the parasitic SCR path can be easily triggered. It would cause a negative impact on the ESD robustness of IC products due to the ESD current diverting through the unexpected discharging path. Accordingly, layout rules between HV pLDMOS and LV-pMOS devices should be carefully defined to prevent the occurrence of unexpected parasitic path in such a 0.25-$\mu$m 60-V/5-V BCD technology.

## Acknowledgment

The authors would like to thank Dr. G.-L. Lin and Dr. Y.-N. Jou of Vanguard International Semiconductor Corporation for their valuable technical support and chip fabrication.

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