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PAPER

A 8 Phases 192 MHz Crystal-Less Clock Generator with PVT Calibration

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SUMMARY A multi-phase crystal-less clock generator (MPCLCG) with a process-voltage-temperature (PVT) calibration circuit is proposed. It operates at 192 MHz with 8 phases outputs, and is implemented as a 0.18 μm CMOS process for digital power management systems. A temperature calibrated circuit is proposed to align operational frequency under process and supply voltage variations. It occupies an area of 65 μm × 75 μm and consumes 1.1 mW with the power supply of 1.8 V. Temperature coefficient (TC) is 69.5 ppm/°C from 0 to 100°C, and 2-point calibration is applied to calibrate PVT variation. The measured period jitter is a 4.58-ps RMS jitter and a 34.55-ps peak-to-peak jitter (P2P jitter) at 192 MHz within 12.67k-hits. At 192 MHz, it shows a 1-MHz-offset phase noise of −102 dBc/Hz. Phase to phase errors and duty cycle errors are less than 5.5% and 4.3%, respectively.

key words: *crystal-less clock generator, multi-phase output, digital power application, process, voltage and temperature (PVT) calibration*

1. Introduction

In the evolution of electrical products, portable devices with more multi-functions and smaller size increase market competitiveness. The necessity has promoted an explosive growth of wafer fabrication and system on chip (SoC). The clock reference circuit is an essential component in digital, analog, and radio frequency (RF) applications [1]. However, power consumption and frequency variation are the most important factors to be overcome in a clock generator. Currently, crystal oscillators (XOs), micro electro mechanical systems (MEMS) oscillators and complementary metal-oxide-semiconductor (CMOS)-based oscillators are three main ways used to generate the reference clock signal. XOs provide highly precise and nearly temperature independent reference clock [2], [3]. However, the crystal (XTAL) is an off-chip component with high power consumption. MEMS oscillators provide higher Q and better signal characteristic than CMOS-based oscillators, whereas need additional micro electro mechanical process to be integrated with traditional CMOS process [4].

Recently, there has been three kinds of CMOS-based oscillators. The inductance-capacitor (LC) oscillators operate at high frequency [5]. The structure has high Q and low phase noise. It mostly targets at RF frequency synthesis. Relaxation oscillators repeatedly alternate between two states with a period that depend on the charging of a capacitor [6]–[10]. All digital CMOS-based oscillators are implemented for applications such as the internal control and the high-speed interface [11]–[13]. The low voltage, power and small area features of all digital CMOS-based oscillators bring enormous benefits.

The CMOS-based oscillators should achieve sufficiently high frequency stability and accuracy over variation in process, voltage, and temperature (PVT) [14]. Switching capacitor and different types of resistors are well-known PVT calibration circuits of oscillators. Multi-phase clock applications, such as high speed data transmission likes clock and data recovery (CDR) or clock synthesis for frequency multiplication, are widely applied in digital and RF circuits [15], [16]. The proposed 8 phases crystal-less clock generator with PVT calibration is fabricated in 0.18 μm CMOS technology. The whole circuit consumes 1.1 mW with the power supply of 1.8 V and the core dimension is 65 μm × 75 μm.

2. Architecture and Circuit Implementation

Figure 1 shows the structure of the proposed multi-phase PVT calibrated CLCG. It includes a ring oscillator, a phase error corrector (PEC), a level shifter and a bias circuit. The bias circuit consists of current source and a PVT calibrated circuit.

2.1 Voltage Controlled Oscillator and Phase Error Correct Circuit

The schematic of the applied voltage controlled oscillator (VCO) is illustrated in Fig. 2. The VCO adopts 4 stages differential cell with 8 phases outputs.

Figure 3 illustrates the circuit of VCO with a phase error correct (PEC) circuit. The phase error mainly occurs at the mismatch of each phase. The circuit routing of the ring oscillator and process variation are the major reasons. The

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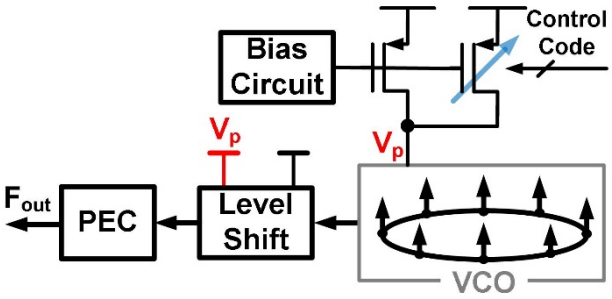


Fig. 1 Block diagram of the proposed CLCG.

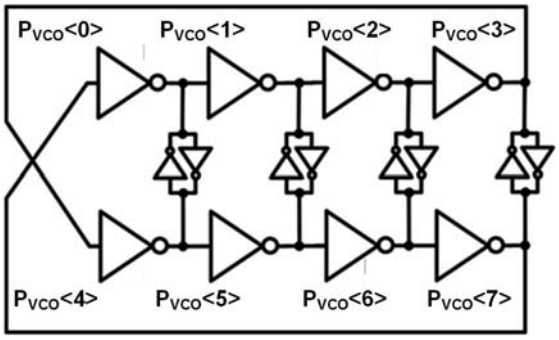
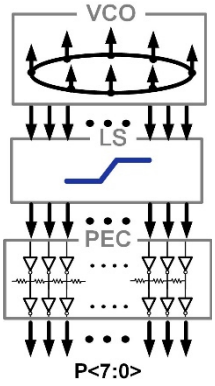
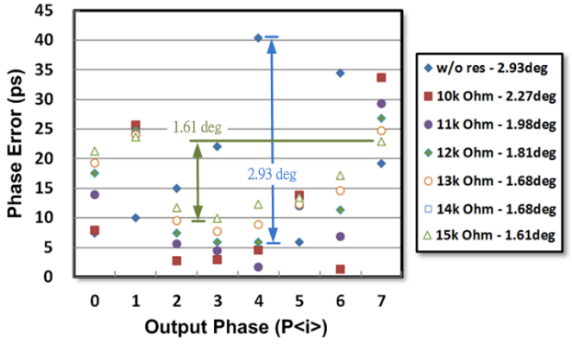


Fig. 2 Schematic of the 8 phase differential ring oscillator.



(a)



(b)

Fig. 3 Block diagram of the VCO, LS, and PEC, and (b) simulated result between output phase and phase error.

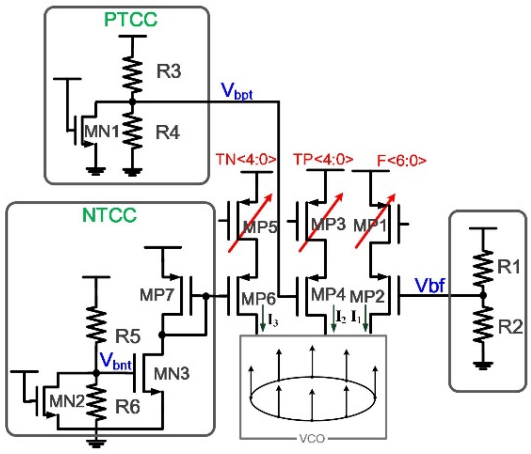


Fig. 4 Block diagram of the PVT calibrated circuit.

PEC circuit applies resistors between each phase to balance the mismatch. Figure 3(b) shows the relationship between output phase and phase error. The phase error without PEC circuit is 40.5 ps (2.93°) at P<4>. The PEC circuit adopts 15k Ohm to achieve the minimum phase error which is 1.61°. Thus, the PEC can reduce 45% of the phase error [17].

2.2 PVT Calibrated Circuit

The modified PVT calibrated CLCG architecture is demonstrated in Fig. 4. The calibrated circuits calibrate the variation by a digital controlling bias circuit. There are three PVT calibrated mechanisms for CLCG. The digital code, F<6:0>, can calibrate the process and frequency variations. The digital code, TP<4:0>, can calibrate the positive temperature variation and the digital code, TN<4:0>, modifies the negative temperature variation. The frequency calibration consists of MP1, MP2, R1, and R2. F<6:0> can control the current I_1 which can modify the VCO frequency. R1, R2, and MP2 are the bias circuit. The bias voltage V_{bf} is as follows.

$$V_{bf} = V_{DD} - (V_{SD(MP1)} + V_{SG(MP2)}) = \frac{R_2}{R_1 + R_2} V_{DD} \quad (1)$$

where $V_{SD(MP1)}$ and $V_{SG(MP2)}$ are the source-to-drain voltage of MP1 and the source-to-gate voltage of MP2, respectively. The voltage division of resistance has to keep MP2 operating at the saturation region.

Simulated frequency versus temperature for the CLCG without temperature calibrations is shown in Fig. 5. Temperature coefficients (TC) are −350, −505, and −901 ppm/°C of slow-slow (SS), typical-typical (TT) and fast-fast (FF) corners, respectively. TC of CLCG are all negative temperature coefficients; therefore, we propose the negative temperature coefficient calibration (NTCC) circuit calibrates negative TC. MP5, MP6, MP7, MN2, MN3, R5, and R6 constitute of the NTCC. TN<4:0> can control the current I_3 which can modify the VCO frequency, and MP6 and MP7 can transfer the calibrated current to I_3.

The simulated results of the temperature calibration part

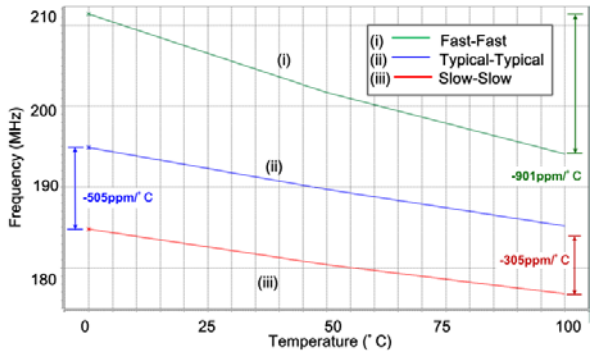


Fig. 5 Simulated frequency versus temperature for the proposed DCO without temperature calibration.

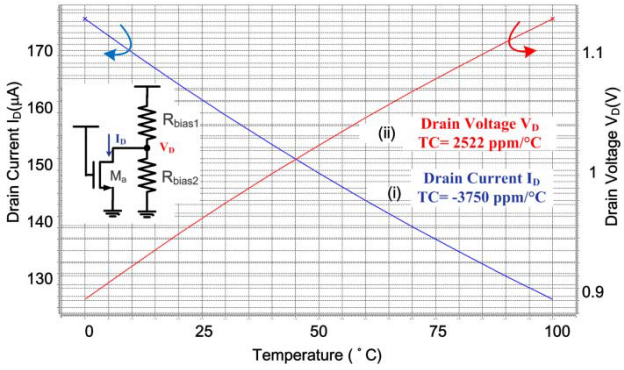


Fig. 6 Simulated frequency versus temperature for the temperature calibration part.

are shown in Fig. 6. The temperature calibration circuit consists one transistor M_a and two bias resistors R_{bias1} and R_{bias2}. The MOSFET drain current I_D is expressed as

$$I_D \propto \mu(T)\,(V_{DD} - V_{TH}(T))^{\alpha} \tag{2}$$

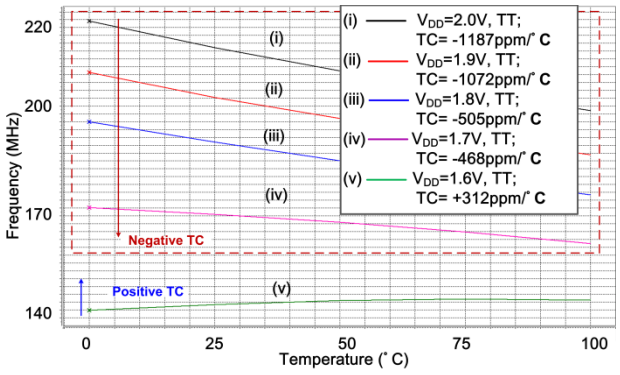
The threshold voltage $V_{TH}(T)$ and mobility μ(T) have temperature dependence [18], [19] as follows.

$$V_{TH}(T) = V_{TH}\,(T_0) - k\,(T - T_0) \tag{3}$$

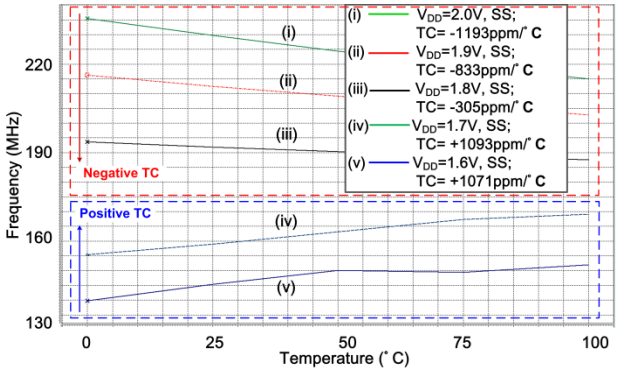
$$\mu(T) = \mu\,(T_0)\left(\frac{T}{T_0}\right)^{-m} \tag{4}$$

where T is the present temperature and T_0 is the room temperature (T_0 = 300 K). α is typically to be 2. k is the threshold voltage temperature coefficient whose typical value is 2.5 mV/K. m is mobility temperature exponent whose typical value is about 1.5~2. Both μ and V_{TH} are negative temperature coefficients. The effect of drain current by μ is much higher than that by V_{TH} as V_{DD} and V_{TH}(T) are relatively large, such as V_{DD} = 1.8 V and V_{TH} = 0.7 V [20]. Figure 6 shows the same trend of drain current versus temperature where drain current is negative TC = −3750 ppm/°C. On the contrary, the effect of drain current by V_{TH} is higher than that by μ as V_{DD} and V_{TH}(T) are relatively small, such as V_{DD} < 1 V and V_{TH} = 0.7 V.

The NTCC circuit consists of the temperature calibration part and a pair of current mirror. The temperature



(a)



(b)

Fig. 7 Simulated frequency versus temperature for the proposed VCO under (a) typical-typical and (b) slow-slow corner with supply voltage variation.

part includes R5, R6, and MN2. It produces the positive TC bias voltage V_{bnt} which controls the drain current of MN3, $I_{D(MN3)}$. As V_{bnt} increases with temperature, so does $I_{D(MN3)}$. In analogy to the mechanism in a current mirror, I_3 is approximately proportional to absolute temperature (PTAT). Therefore, the output frequency can be pulled up with temperature by bias current I_3. The PTAT current modifies a negative temperature coefficient via digital code, TN<4:0>.

Figure 7(a) shown the simulation results of the frequency accuracy of CLCG under TT corner with supply voltage variation. TC are 312, −468, −505, −1072, and −1187 ppm/°C of V_{DD} = 1.6 V, 1.7 V, 1.8 V, 1.9 V, and 2.0 V, respectively. However, TC turns out to be a positive temperature coefficient as supply voltage is reduced to 1.6 V from 1.8 V. As a MOS device has a large current, the CLCG can obtain a negative temperature coefficient easily.

With variations of process corner and supply voltage (SS corner and low supply voltage), the CLCG becomes a positive temperature coefficient. For example, Fig. 7(b) shows the simulation results of the frequency accuracy of CLCG under SS corner. The TCs with V_{DD} = 1.6 V and V_{DD} = 1.7 V become positive temperature coefficients which fails the implementation of a negative temperature calibrated circuit under low voltage supplies. The main reason is that

the additional bias circuit reduces the head room of the VCO. Applying long channel length devices of the oscillator keeps TC staying in a negative temperature coefficient. Besides, an adoption of the positive temperature calibrated circuit (PTCC) is a low cost and low power consumption way.

MP3, MP4, MN1, R3, and R4 constitute of the positive temperature calibration which is the same as the circuit of right hand side in Fig. 6. TP<4:0> is able to control the current I_2 which can modify the frequency. As V_{bpt} increases with temperature, $I_2 = I_{D(mp4)}$ decreases. Therefore, I_2 is complementary to absolute temperature (CTAT). The CTAT current modifies the positive temperature variation by digital code, TP<4:0>.

Figure 8 shows the simulation result after temperature calibration. Temperature coefficients (TC) are 83, 62.5, and 46.9 ppm/°C of SS, TT and FF corners, respectively. TC at V_{DD} = 1.6 V is 119 ppm/°C of TT corner. The compensated curve of negative TC is concave, while the one of positive TC is convex. The frequency resolution of F<6:0> is $\frac{\text{Tuning Range}}{2^N} = \frac{128\,\text{MHz}}{2^7} = 1\,\text{MHz}$, where N is the number of digital code. Besides, the frequency resolution of TP<4:0> is $\frac{\text{Tuning Range}}{2^N} = \frac{16\,\text{MHz}}{2^5} = 500\,\text{kHz}$. Tuning step of TP<4:0> is 32.5 ppm/°C. The frequency resolution of TN<4:0> and TP<4:0> are 500 kHz.

2.3 Level Shifter

Buffers are widely applied to amplify the digital signals. As the operating voltage increases, the output signal couldn't be properly amplified to full swing or even turn off to zero. The schematic of level shifter is shown in Fig. 9. The level shifter amplifies the output swing to guaranteed full swing outputs. The output signal of VCO provides low voltage supply (V_{DDL}) input signal (P_{VCO}<i>) to level shifter. Two NMOS devices with gate connection to P_{VCO}<i> and $\overline{P_{VCO}}$<i> speed up the transition. The input signal which is low voltage level ensures that the CLCG could produce high voltage level output signal P_{LS}<i> under a low voltage supply. Furthermore, the power consumption of level shifter is lower than traditional buffers [21].

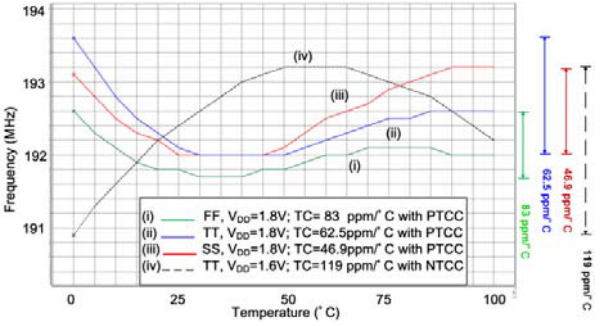


Fig. 8 Simulation results of frequency versus temperature for the proposed CLCG after calibration.

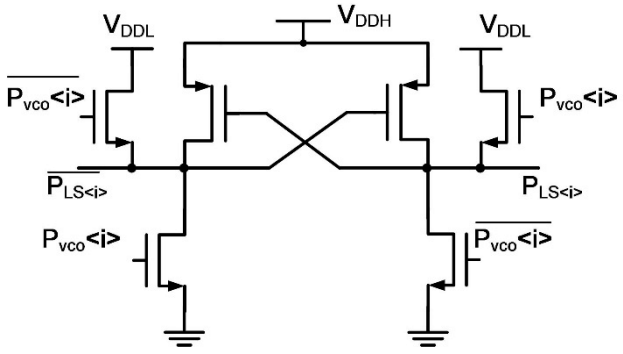


Fig. 9 Schematic of a level shifter.

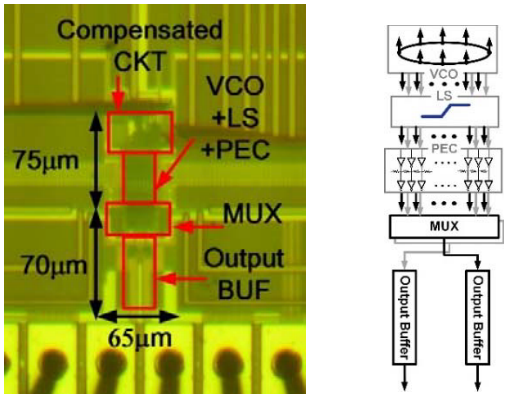
3. Experimental Results

The proposed clock generator has been fabricated in a 0.18 μm GP (general purpose) CMOS process without specialized analog process options. Die photograph is shown in Fig. 10(a). The core dimension which includes multiplier (MUX) and output buffers is 65 μm × 145 μm. The MUX and output buffers are used to measure the information of each phase output signal. Therefore, the CLCG core area is 65 μm × 75 μm.

In Fig. 10(b), the block of output stage for measuring phase to phase errors and duty cycle errors is illustrated. The output stage includes MUX and output buffers. The MUX is applied to select phases and phase to phase errors can be measured by selecting two adjacent phases. The MUX is also capable to produce additional jitter each output phase. The output buffer includes tap buffers and resistances. The total power consumption is 1.1 mW at 1.8 V.

3.1 Process Voltage Temperature Calibration

Figure 11 shows the measurement environment. Temperature measurements were performed in a programmable thermal chamber. Frequency drift was measured with a real-time oscilloscope (Agilent 81204B). The PVT calibration setup can be theoretically considered as the following operations:



(a) (b)

Fig. 10 (a) Die photograph of the proposed circuit, and (b) block of output stage.

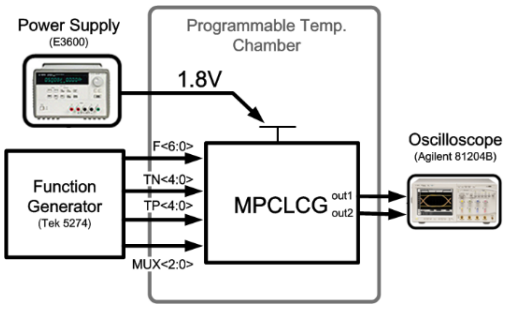


Fig. 11 Measurement setup.

First of all, we determine the offset and slope by temperature measurement. After setting all the digital code, F<6:0>, TP<4:0> and TN<4:0> to zero, we put the device under test (DUT) into a programmable temperature chamber and measure the frequency at 20°C and 80°C respectively. Therefore, the offset (ΔF) which denotes the difference between measured frequency and targeted frequency could be found. And the temperature offset, ΔT, is equal to 60°C, that is 80°C − 20°C. $slope = \frac{\Delta F80°C - \Delta F20°C}{\Delta T}$.

Secondly, we select the temperature calibration circuit by the trend of the temperature dependence. The measured frequency to temperature curve is used to spot the temperature calibration circuit. If the slope is negative, the negative calibration circuit is applied. Otherwise, the positive calibration circuit is adopted for a positive TC.

Finally, the calibrated circuits calibrate the frequency variation automatically. From Fig. 8, one optimal compensated point is obtained under one temperature and voltage setting. These simulated optimal compensated points are then plotted in Fig. 12. The vertical axis refers to digital code in both Fig. 12(a) and (b) while the horizontal axis denotes an offset and a slope respectively in Fig. 12(a) and Fig. 12(b). We plotted fitting lines by linear regression analysis. Then we could get any desired digital code by substituting measured offset and slope into fitting lines in Fig 12(a) and (b).

Measured results after calibration are shown in Fig. 12(c). After calibration mechanism, PVT calibration which calibrates the initial frequency to 192 MHz at 20°C has been applied. The total temperature coefficient is measured in the external 1.8-V unregulated power supply under a temperature range from 0 to 100°C. TC without any calibration is ±2.375% or 475 ppm/°C and turns out to be ±0.342% or 69.5 ppm/°C after calibration. Figure 12(c) also shows the measured results under various supply voltage. The blue line, representing V_{DD} = 1.6 V, is the only one with positive temperature calibration and the unique concave curve, which conforms to theoretical simulation.

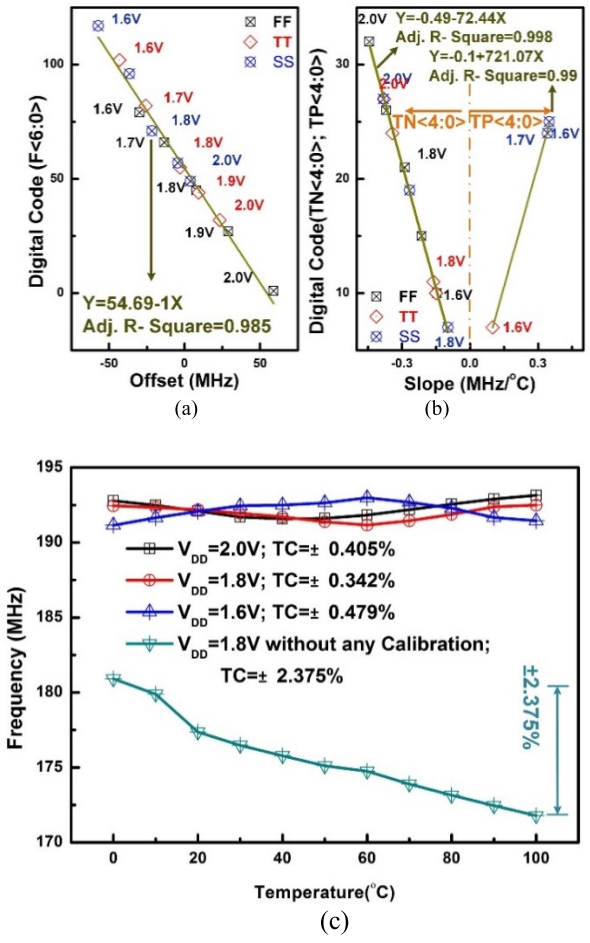


Fig. 12 (a) Relationship between digital code and (a) offset, (b) slope, and (c) measurement result after temperature calibration with V_{DD} variation.

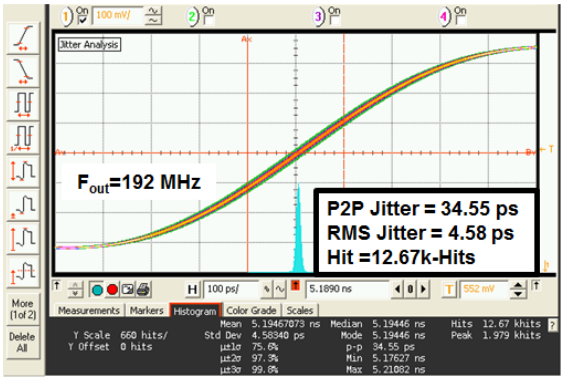


Fig. 13 Jitter performance where RMS=4.58 ps and P2P=34.55 ps of 192 MHz output at 1.8 V.

3.2 Jitter and Phase Noise

Figure 13 represents the operating frequencies of CLCG at 20°C and the jitter histogram at 1.8 V. The CLCG output demonstrates a 4.58-ps RMS jitter and a 34.55-ps peak-to-peak jitter (P2P jitter) at 192 MHz within 12.67k hits. The RMS and P2P period jitters are less than 0.088% and 0.665%, respectively. Fig. 14 shows the output spectrum of the VCO with a supply voltage of 1.8 V, and the phase noise of output signal. As shown in Fig. 14, the phase noise is −102.03 dBc/Hz @ 1 MHz offset and −124.24 dBc/Hz @ 10 MHz.

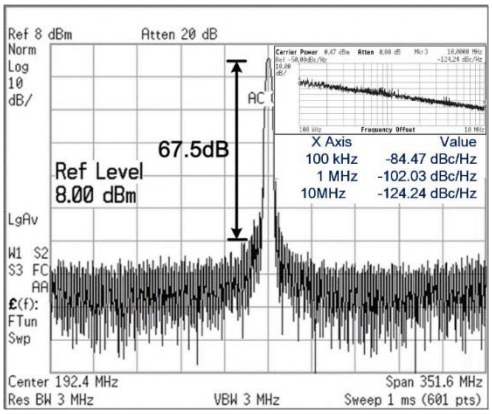


Fig. 14 Measured output spectrum and phase noise of 192 MHz output of the VCO with a supply voltage of 1.8 V.

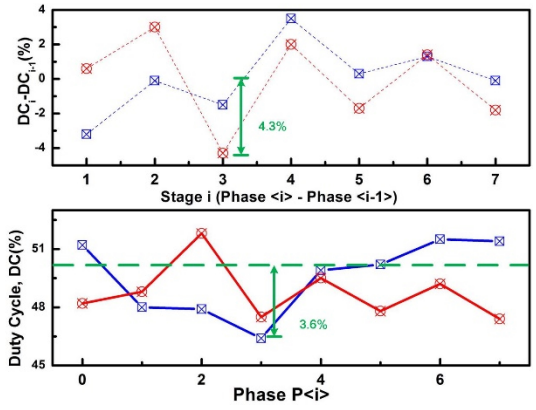


Fig. 15 Measurement result of duty cycle error and phase to phase duty cycle error.

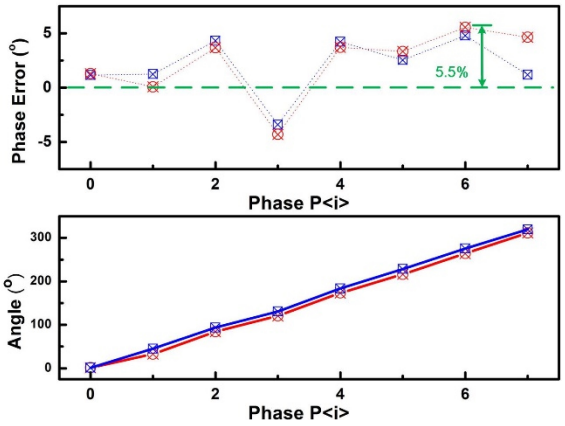


Fig. 16 Measurement result of output phase and phase to phase error.

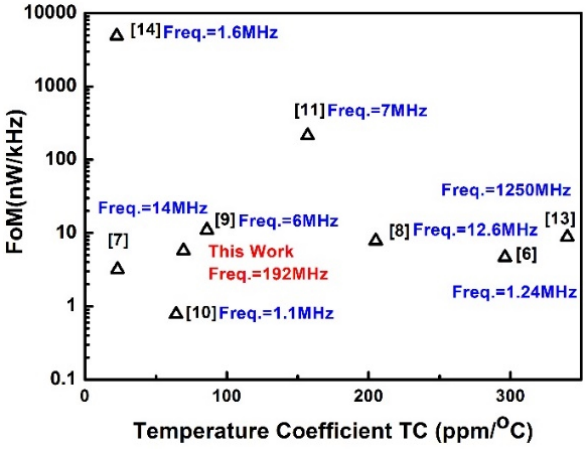


Fig. 17 FOM versus temperature coefficients.

3.3 Duty Cycle Error and Phase to Phase Error

In Fig. 15, the duty cycle and phase to phase errors under the two test chips are shown. The maximum duty cycle error is 3.6%, which occurs at P<3>. The phase to phase duty cycle error (DC_i–DC_{i-1}) is a crucial point for pulse width modulation (PWM) applied in power converter [22]. The maximum phase to phase duty cycle error is 4.3% occurring at stage 3 which is between P<2> and P<3>. Figure 16 represents the output phase and phase error of two chips respectively. Output phase increases 45° per phase. The phase error is the error between ideal phase and measured error. The maximum phase error is 5.5% occurring at P<6>. The total phase error is between −4.3 to +5.5%. The phase error can be reduced efficiently by adjusting the VDD of output buffers.

Table 1 summarizes and compares the current temperature calibrated clock generators and the proposed circuit. Compared to other ring oscillator, our proposed 8 phases CLCG exhibits the lowest temperature sensitivity, smaller size and lower jitter performance. Besides, the performance of the duty cycle error and phase error are quite excellent performance as well. Fig. 17 shows the figure of merits (FoM) versus temperature coefficients. The FOM is defined as a ratio of the power consumption to the oscillation frequency (nW/kHz) [10]. The calculated FOM is 5.73 nW/kHz for the proposed circuit, and is better than other works expect for [6], [7], and [10]. However, the area of the proposed circuit is smaller than others. Besides, the frequency of proposed circuit is much higher than other works. Comparing with traditional PVT calibration mechanism such as blending TC of polysilicon resistor and diffusion resistor or bandgap reference circuit [10], [11], the proposed PVT calibration circuit has nearly equivalent TC as above works. The oscillators of relaxation or thermal diffusivity based have lower TC than others structures. However, above designs have large die dimensions or high power consumption. Therefore, these designs are widely applied at precisely microelectromechanical systems.

4. Conclusion

The proposed 8 phases crystal-less clock generator circuit was fabricated in a 0.18 μm CMOS technology. It consumes 1.1 mW with a power supply of 1.8 V, and occupies

Table 1 Performance comparisons of clock generators.

	[6]	[7]	[8]	[9]	[10]	[11]	[12]	[14]	This work
Architecture	Rex.	Rex.	Rex.	RC.	Rex.	Ring	Ring.	Ther. Diff.	Ring
Technology (nm)	130	180	65	65	180	250	130	700	180
Multi-Phase	1	1	1	1	1	1	1	1	8
Supply voltage (V)	1.2	1.8	1.2	1.8	1.8	2.4	3.3	5	1.8
Frequency (MHz)	1.24	14	12.6	6	1.1	7.03	1250	1.6	192
Power (mW)	0.0058	0.045	0.0984	0.066	0.00086	1.5	11	7.8	1.1
TC(ppm/°C)	296	23@ -40~125 °C	205@ 0~80 °C	86@ 0~100 °C	64.3@ -20~80 °C	101@ -40~125 °C	340@ -40~125 °C	22.4@ -55~125 °C	69.5@ 0~100 °C
DC variation (%)	±1.8@ 1.01~0.99V	±0.16@ 1.7~1.9V	±0.07@ 1.1~1.5V	N.A	<3@ 1.2~2.4V	0.31@ 2.4~2.75V	N.A.	N.A.	±3.6
Jitter(ps) (RMS) (P-P)	3448p (0.278%)	40p(P-P) (0.056%)	N.A.	N.A.	N.A.	N.A.	N.A.	312ps (0.0195%)	4.58p (0.088%) 34.55p (0.665%)
PN(dBc/Hz) @1MHz	N.A	-115	-120	-94.6 @100kHz	-74.2	N.A.	-88	N.A.	-102
Area (mm^2)	0.016	0.04	0.01	0.03	0.075	1.6	0.014	6.75	0.0049
FOM(nW/kHz)	4.68	3.2	7.81	11	0.78	213.4	8.8	4875	5.73

core dimension of 65 μm × 75 μm excluding output buffer and MUX. The measured period jitters are a 4.58-ps RMS jitter and a 34.55-ps P2P jitter at 192 MHz within 12.67k hits. At 192 MHz, the phase noise of CLCG is −102 dBc/Hz at 1-MHz-offset. Operational frequencies vary ±0.34% at V_{DD} = 1.8 V and ±0.479% with 10% supply voltage variation between 0° and 100°C. The maximum duty cycle error is 4.3%, and the phase to phase errors are less than ±5.5°. This work not only realizes a CLCG operating with 8 phases outputs, but also fulfills sufficiently high frequency stability and accuracy under the process and temperature variations.

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