Quad-SCR Device for Cross-Domain ESD Protection

Federico A. Altolaguirre and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*— A new electrostatic discharge (ESD) protection device, called quad-silicon controlled rectifier (QSCR), is proposed and verified in a 0.25-μm CMOS process. The QSCR is designed to be used as ESD protection between separated power domains. Since the QSCR embeds four SCRs between its four terminals, no extra ESD clamps are needed to protect the interface circuits between two separated power domains. Implementations with different circuit topologies were also analyzed to achieve a comprehensive ESD protection design for different applications. From the experimental results, the QSCR can withstand 8-kV HBM and 600-V MM ESD stresses with a silicon area of 75 μm x 100 μm.**

***Index Terms*— Electrostatic discharge (ESD), separated power domains, silicon controlled rectifier (SCR).**

I. Introduction

ELECTROSTATIC discharge (ESD) is a main reliability issue in the IC industry [1]. ESDs are high-energy transient events that result due to the charge balance between bodies. ESD can affect ICs during handling, discharging several amperes through the chip in only a few nanoseconds. Such discharges can harm the internal devices of the ICs [2]–[4]. Therefore, special ESD protection devices are placed around the pads to protect the ICs from ESD damage. Due to the random nature of ESD, every pin-to-pin combination must be protected [5].

Whereas earlier technologies used only a single supply voltage, modern ICs tend to require several power supplies. With the continuous scaling down of the CMOS technology nodes, the core voltages have also been scaled down to reduce power consumption. However, IO voltages are not scaled down the same, and they still need to comply with legacy interfaces. Besides, some special circuits, such as PLLs, are very sensitive to noise in the supply lines, and thus require isolated supply lines [6]. In addition, some state-of-the-art circuits are designed with separated power domains for smart power control [7]. Thus, modern ICs often include at least two separated power domains.

Manuscript received March 29, 2016; revised May 25, 2016 and June 3, 2016; accepted June 6, 2016. Date of publication June 23, 2016; date of current version July 21, 2016. This work was supported by the Ministry of Science and Technology, Taiwan, under Contract MOST 103-2221-E-009-197-MY2 and Contract MOST 105-2622-8-009-001-TE1. The review of this paper was arranged by Editor B. Kaczer. *(Corresponding author: Ming-Dou Ker.)*

F. A. Altolaguirre is with the Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: federicoaa@gmail.com).

M.-D. Ker is with the Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, and also with the Department of Electronics, I-Shou University, Kaohsiung 840, Taiwan (e-mail: mdker@ieee.org).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2016.2579170

However, the chip implemented with separated power domains introduced new challenges to the ESD protection design. Since ESD may happen between any two pins of an IC, ESD between pins in different power domains would flow through the interface circuits (since the power and ground lines are isolated) thus causing damage [8]. Typically, the back-to-back diodes are added between the different ground lines to provide safe discharge paths to the ESD currents. Depending on specific cases, the back-to-back diodes may not provide enough protection, so extra ESD protection devices must be added to further protect the interface circuits. Some previous works had proposed different approaches to solve this problem [9]–[12]. In [9], ESD conduction elements were used to connect the separated power domains via the shared ESD buses, thus guaranteeing safe ESD paths between the multiple power domains. In [10], the interface circuits were engineered to avoid oxide degradation by having the ESD detection capability. In [11], secondary ESD clamps were added to the interface signals in order to protect the receiver circuits. In [12], the secondary cross-connected clamps were added between the power domains, offering similar protection as that in [11], but without adding extra elements to the signal lines.

In this work, a novel design is proposed for ESD protection between two separated power domains using a single ESD clamp. The use of a single ESD clamp simplifies the design and verification process, which also help to reduce the required silicon area of on-chip ESD protection. A comprehensive study of the proposed device and applications has been done, including TCAD and SPICE simulations, and silicon verification in a 0.25-μm CMOS process.

II. ESD Protection for Separated Power Domains

Fig. 1 shows the typical case of an interface circuit between two separated power domains and the corresponding ESD protection devices. Each domain has its own (same domain) power-rail ESD clamp device, typically a large nMOS transistor or a silicon controlled rectifier (SCR). In addition, two back-to-back diodes are added between the ground lines to provide a safe ESD discharge path between the two power domains. If an ESD event happens between, for example, V_{DD1} and V_{SS2}, the ESD current would flow through the same-domain ESD clamp between V_{DD1} and V_{SS1} first, then through the back-to-back diode to V_{SS2}. The total voltage drop between V_{DD1} and V_{SS2} is the voltage drop across the power-rail ESD clamp, plus the voltage drop across the back-to-back diode, plus the voltage drop across the parasitic resistance of the ground metal line. If this voltage drop is larger than

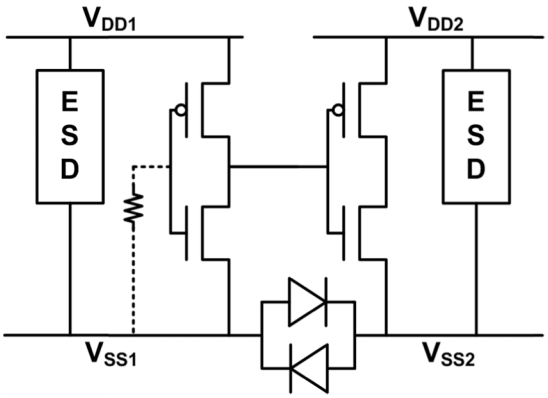

Fig. 1. Traditional ESD protection design for a chip with two separated power domains. The interface circuit is conceptually shown by two inverters.

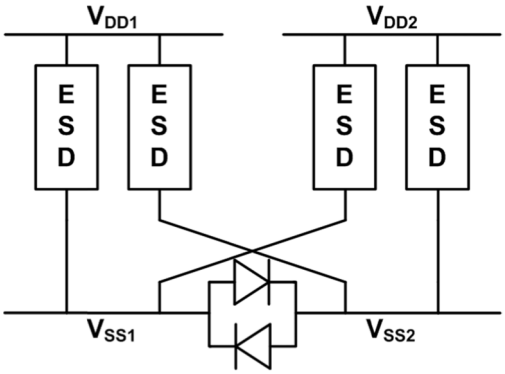

Fig. 2. Full ESD protection between two separated power domains using four ESD clamps. Interface circuit not shown.

the breakdown voltage of the MOS transistors, some current will flow through the interface circuits, causing damage to the devices of the interface circuits.

In order to reduce the voltage drop between V_{DD1} and V_{SS2} during ESD stress, an extra ESD clamp can be added between the power rails, as shown in Fig. 2. In this case, for an ESD zapping between V_{DD1} and V_{SS2}, the secondary ESD clamp (between V_{DD1} and V_{SS2}) helps to conduct ESD current in addition to the primary ESD clamp (between V_{DD1} and V_{SS1}), thus reducing the overall voltage drop between V_{DD1} and V_{SS2}. With the additional ESD clamps directly connected across the separated power and ground lines, the interface circuits can be safely protected against ESD damage.

III. Proposed ESD Protection Design

Fig. 3(a) shows the cross-sectional view of the proposed ESD device structure, Quad-SCR (QSCR), which is formed by two isolated p-wells (PW1 and PW2) and an n-well in between the two p-wells. The n-well has two p^+ regions connected to two positive terminals (V_{p1}, V_{p2}). Each p-well (PW1, PW2) is connected to one of the negative terminals (V_{N1}, V_{N2}), respectively. In addition, two poly gates are placed in the n-well/p-well interfaces in a similar way as that of LVTSCR [13]–[15]. There are a total of four SCR paths between the two positive terminals and the two negative terminals, hence this device is named QSCR.

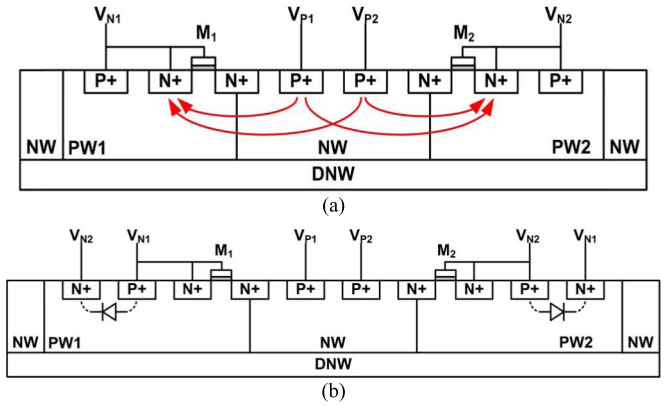

Fig. 3. (a) QSCR cross-sectional view with the four SCR paths indicated with arrows. (b) QSCR with back-to-back diodes embedded in the p-wells. The gates M_1 and M_2 are connected to V_{n1} and V_{n2}, respectively, through protection resistors (not shown).

In the standalone use, the two positive terminals are connected to V_{DD1} and V_{DD2} and the two negative terminals are connected to V_{SS1} and V_{SS2}. The resulting equivalent circuit is identical to that in Fig. 2 (with the exception of the back-to-back diodes).

The back-to-back diodes could be fully embedded into the QSCR by adding n^+ connections in the p-wells connecting the opposite ground line (V_{SS2} in PW1 and V_{SS1} in PW2) at the expense of extra metal routing complexity, as shown in Fig. 3(b). In addition, some applications would require diode strings in the ground-to-ground diodes or dual SCR devices to further increase the noise isolation. For this case, the M_1 and M_2 gates can be cross-connected (M_1 connected to V_{SS2} and M_2 connected to V_{SS1}) to create a low-triggered dual SCR path between V_{SS1} and V_{SS2}, similar to that reported in [16]. Note that for this case, only one parasitic SCR path in the QSCR will conduct current under ESD stress.

TCAD simulation was used to aid in the QSCR design. A 2-D simulation was done using Taurus Medici, including device physical models such as band-to-band tunneling, avalanche, and Shockley-Read-Hall (SRH) and auger recombination is used for high-current injection condition. The device cross-section of Fig. 3(a) was reproduced in TCAD using a 0.25-μm CMOS process model. The p^+ and n^+ regions are 1 μm in length, with the exception of the floating n^+ regions between the n-well and p-wells, which are set as 2 μm. The gates are drawn with $L = 1$ μm. An ESD-like event is simulated between V_{p1} and V_{n1}. V_{p2} is left floating, V_{n1} is set to 0 V, and V_{n2} is set to 0.7 V to simulate an external ground diode. Fig. 4 shows the TCAD simulation results, indicating the total current magnitude. It can be seen that both the SCR paths (V_{p1}-to-V_{n1} and V_{p1}-to-V_{n2}) are triggered. It was found in the simulation that the trigger voltage is 9.75 V.

The standalone QSCR cannot be used for supply voltages higher than the holding voltage of the parasite SCR path when considering the latch-up risk [17]. To avoid latch-up, diode strings can be added between the QSCR and the power rails to increase its total holding voltage. The trigger voltage also increases with every added diode. So for some designs with more diodes added in the diode strings, the trigger voltage would be too high to protect the interface circuits. The QSCR

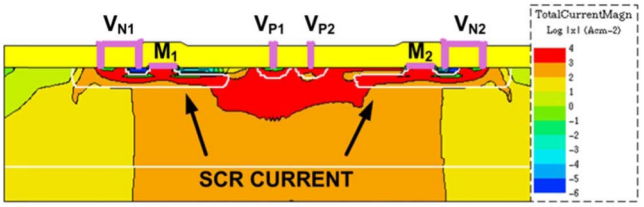

Fig. 4. TCAD simulation results for QSCR under ESD-like stress.

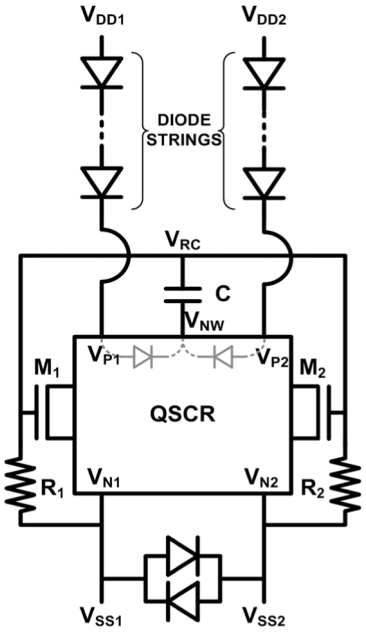

Fig. 5. QSCR with diode strings and trigger circuit. The internal terminal notations of the QSCR correspond to the terminals in Fig. 3(a).

in Fig. 3(a) can be modified to include an active trigger mechanism to reduce the trigger voltage. Fig. 5 shows a proposed realization using a CR circuit to trigger on the QSCR during ESD events. The diode strings are added between the V_{DD} and V_p connections. The two diode strings can be of different number of diodes if the two power supplies have different operation voltages (e.g., 2.5 and 5 V). The capacitor C is connected to the QSCR n-well via an n^+ tap. The two resistors (R_1 and R_2), of the same value, complete the RC circuit connected to the gates M_1 and M_2.

The circuit operation is as follows. During normal circuit operation, both V_{DD} lines are at the stable operation voltage and the ground lines are at 0 V. Since both V_{DD} lines are at a DC voltage, no current flows through the capacitor, and therefore both M_1 and M_2 are kept OFF. During an ESD-like event, suppose between V_{DD1} and V_{SS1}, V_{DD1} quickly rises to a high voltage, whereas V_{DD2} and V_{SS2} are floating. The capacitor C is initially discharged, so a current would flow through the diode string connected from V_{DD1} to V_{p1}, then to the n-well through the parasitic p^+/n-well diode to the capacitor. Some part of the transient current then flows through R_1 to V_{SS1}, and another part also flows through R_2 and the back-to-back diode to V_{SS1}. The voltage drops on the resistors turn M_1 and M_2 ON, which turn the SCR paths on. Since the SCR paths are self-latched, the

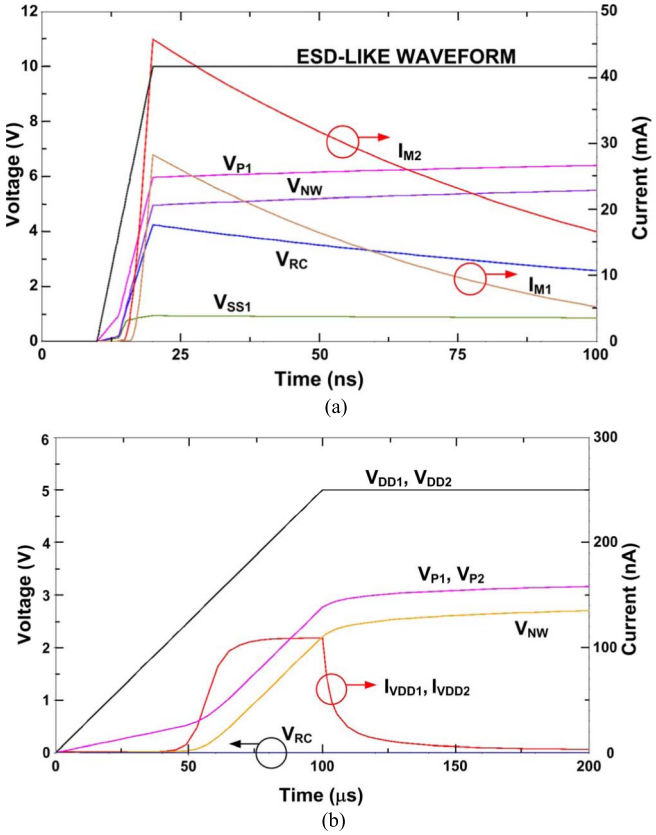

Fig. 6. Simulation results for the circuit of Fig. 5 under (a) ESD-like stress condition between V_{DD1} and V_{SS2} and (b) normal power-on condition.

transistors only need to be turned on long enough to trigger the SCRs.

For the ESD stress across the power domains, for example from V_{DD1} and V_{SS2}, whereas V_{DD2} and V_{SS1} are floating, the transient current is conducted from V_{DD1} to V_{p1}, then through the capacitor C to charge up the gate voltages of transistors M_1 and M_2 via the resistors R_1 and R_2 to the grounded V_{SS2}. The turned-on M_1 and M_2 will in turn trigger on the SCR path from V_{DD1} and V_{SS2}, and the SCR path from V_{DD1} and V_{SS1}. Therefore, the interface circuits across the separated power domains can be fully protected by the proposed QSCR design.

The circuit operations of Fig. 5 are simulated in SPICE using the device models of a 0.25-μm CMOS process. The SCR paths were not included, only the V_p/n-well parasitic diodes. For this simulation, four diodes were used on each diode string, M_1 and M_2 are drawn with dimension $W/L = 100/1\ \mu$m, C is 3 pF, and R_1 and R_2 are both 48 kΩ. Fig. 6(a) shows the SPICE simulation result for an ESD-like stress (10 V with $t_r = 10$ ns) between V_{DD1} and V_{SS2}. It can be seen that both the transistors (M_1 and M_2) are turned on. Although the M_1 current is smaller than the M_2 current, it is large enough to turn the SCR path on. The equivalent time constant was extracted from the simulation, and it is $\sim$160 ns. Note that this value is different from a direct multiplication of the R and C values, due to the diodes presented in the trigger circuit. Fig. 6(b) shows the simulation result for a power-ON condition, with both V_{SS1} and V_{SS2} grounded, and V_{DD1} and V_{DD2} slowly rising to 5 V with 100 μs rise time.

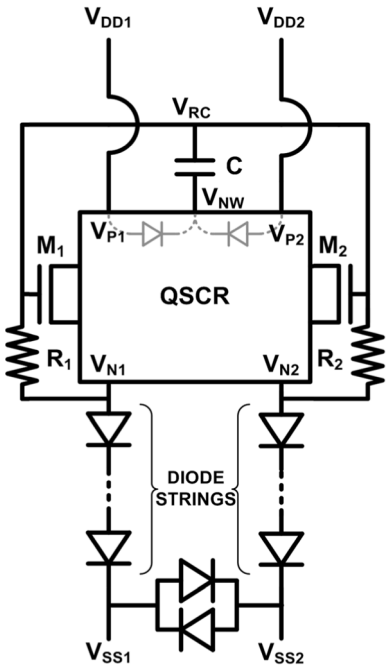

Fig. 7. QSCR with trigger circuit and the diode strings placed at the bottom.

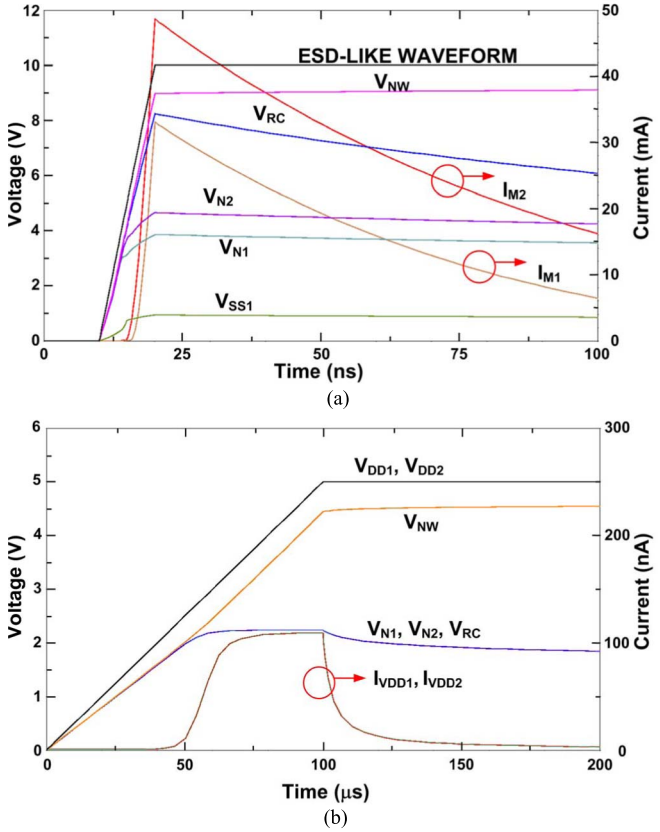

Fig. 8. Simulation results for the circuit of Fig. 7 under (a) ESD-like stress condition between V_{DD1} and V_{SS2} and (b) power-on condition.

After the initial transient, the leakage current stabilizes to less than 1 nA.

The circuit in Fig. 5 introduces a resistive path between the two ground lines ($R_1 + R_2$). The total resistance of this path is typically large, so it would not cause any misbehavior in the circuit. Although, if noise isolation is of concern, the diodes in the diode strings can be placed between the V_N and V_{SS} lines instead. Fig. 7 shows a realization of this circuit. The resistors are connected to the V_N lines, thus there are no resistivity paths between the ground lines. A limitation on the application of this configuration is that since the SCR paths are on the top, both the diode strings must be of the same size.

Fig. 8 shows the SPICE simulations for this circuit under the ESD-like stress condition between V_{DD1} and V_{SS2} and the normal power-on condition, using the same ESD-like waveform and device parameters as those in the simulation of Fig. 6. Note that in Fig. 8(a) during ESD stress, the transistors currents are slightly larger (5%), compared with that in Fig. 6(a). The fast-transient voltage applied to V_{DD1} is easier to reach the capacitor C in this circuit topology, so the gate voltages of M_1 and M_2 will be charged up higher to generate the larger transistor currents. It is clear from the simulations in Figs. 6 and 8 that these two proposed circuit topologies will trigger on the SCR paths in the same way. Therefore, it is up to the designer to choose the one that fits better with the design constraints.

IV. Experimental Results

A. Silicon Implementation

The QSCR was implemented in a 0.25-μm CMOS process with a deep n-well (DNW) layer. Several test devices were realized, including the standalone QSCR and the QSCR devices with two and four diodes in the diode strings. In addition, the QSCR with four diodes in the diode strings was realized with the CR trigger circuit shown in Fig. 5. The QSCR layout dimension is 100 μm $\times$ 32 μm. The QSCR with the four diodes in the diode string has a total layout area of 100 μm $\times$ 75 μm. The test devices include the separated ground diodes between V_{SS1} and V_{SS2}. All the diodes in this device work as p^+/n-well diodes, using the same width as the QSCR and 1-μm length. Fig. 9(a) shows the layout of the QSCR with the diode strings placed at the top and at the bottom of the QSCR, showing also a zoomed view of the QSCR structure with all the connections highlighted. Fig. 9(b) shows the layout of the QSCR with the trigger circuit of Fig. 5.

B. Transmission Line Pulsing

Transmission line pulsing (TLP) is an important verification tool for ESD devices [18]. A Celestron TLP tester was used with a 100-ns pulsewidth and 10-ns rise time. Fig. 10 shows the TLP-measured I–V curves for the QSCR with and without the diode strings. There are two different stress types for the QSCR, same-domain stress (from V_{DD1} to V_{SS1} and V_{DD2} to V_{SS2}) and cross-domain stress (from V_{DD1} to V_{SS2} and V_{DD2} to V_{SS1}). Because of the symmetry of the device, the TLP results for the two same-domain (or cross-domain) cases are the same. The QSCR holding voltage is $\sim$2 V for the same-domain case and $\sim$2.5 V for the cross-domain case. The cross-domain TLP test has

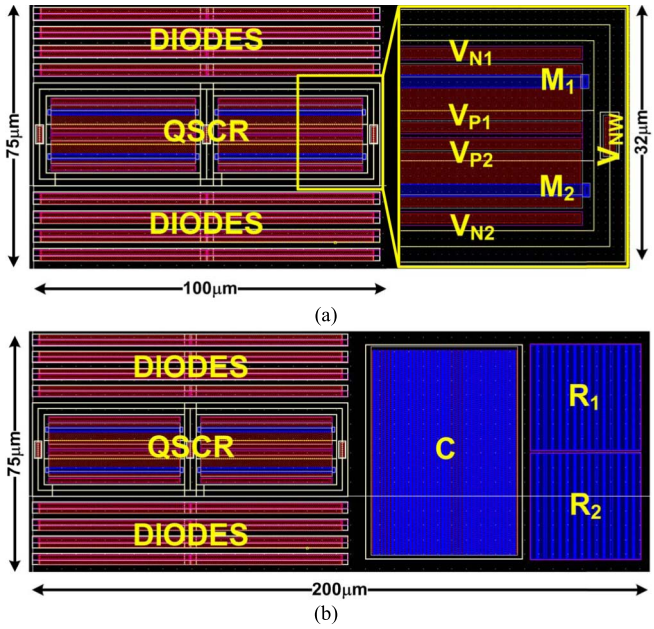

Fig. 9. (a) QSCR layout showing the diode strings disposition (four diodes each) and a zoomed-in view of the QSCR layout showing internal connections. (b) QSCR layout with diode strings and CR trigger circuit. Metal lines are not shown. V_{DD1} and V_{SS1} are drawn from the top and V_{DD2} and V_{SS2} are drawn from the bottom.

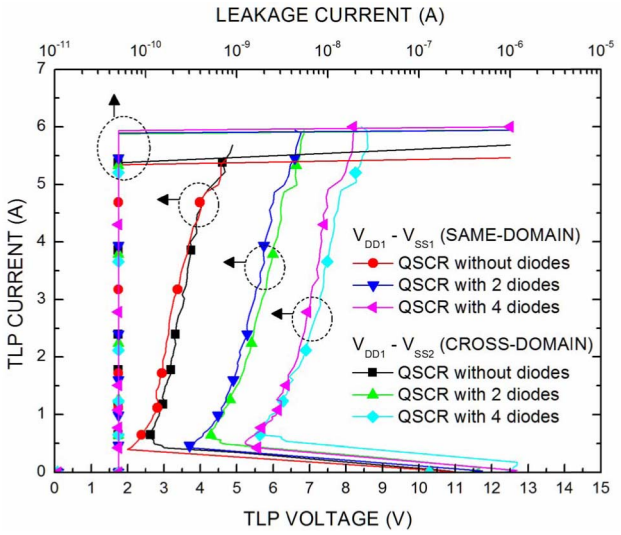

Fig. 10. TLP I–V curves for QSCR with and without diode strings. No CR trigger is added in this test.

a slightly higher holding voltage due to the longer SCR path. Trigger voltage is ~10 V for both the cases. The QSCR with diode strings show an increase in both the holding voltage and the trigger voltage at a ratio of 0.8 V per diode. I_{t2} is 5.5 A for the QSCR without diode strings, and slightly higher (~6 A) with the diode strings. The leakage current was measured with 2 V bias for all the cases at room temperature. The measured leakage current was below the equipment resolution (50 pA).

Fig. 11 shows the TLP results for the QSCR with four diodes in the diode strings and the CR trigger (as shown in Fig. 5). The holding voltage is ~5.35 V for the same-domain case and ~5.76 V for the cross-domain case. The trigger

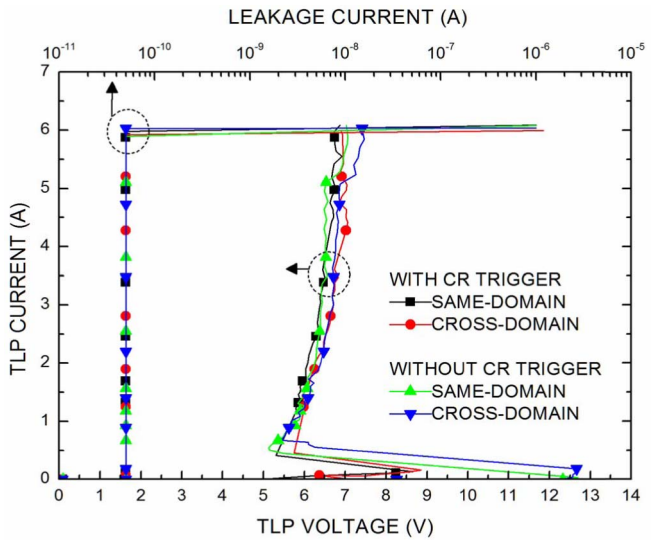

Fig. 11. TLP I–V curves for QSCR with four diodes in the diode strings and with (or without) the CR trigger.

voltage can be effectively reduced from ~12.5 to ~8.8 V using the CR trigger circuit. I_{t2} is ~6 A for the same-domain and cross-domain cases. The leakage current was measured at 2 V bias and was below the equipment resolution. The leakage current was further measured separately at 5 V bias and reports 2.74 nA at room temperature. The extra leakage current is attributed to the diode strings, and it can be further reduced by redesigning the diode strings with consideration of the leakage current [19]–[22].

C. ESD Robustness

To verify the ESD protection effectiveness of the QSCR, a simple interface circuit, such as that (inverter) shown in Fig. 1, was built in the test chip. The transistors in the interface circuit are 5 V devices with dimensions $W/L = 10\ \mu$m/500 nm for the nMOS and $W/L = 20\ \mu$m/500 nm for the pMOS. In addition, the ESD protection shown in Fig. 1 is used as comparison, and also fabricated in the same test chip, including the back-to-back diodes between V_{SS1} and V_{SS2}. The traditional ESD clamps were implemented with GGNMOS clamps with device size (W/L) of 560 μm/800 nm. Each GGNMOS layout area is 50 μm × 90 μm. The leakage current of such a GGNMOS clamp is 15.39 nA with 5 V bias at room temperature.

ESD robustness was tested using the human body model (HBM) [23] and machine model (MM) [24] for both the same- and cross-domain test modes. The results are summarized in Table I. The QSCR can pass >8 kV HBM and 600 V MM for the same- and cross-domain ESD tests. The comparison circuit (labeled GGNMOS in Table I) passes >8 kV HBM and 600 V MM for the same-domain ESD test, but only 5 kV HBM and 250 V MM for the cross-domain ESD test.

D. Failure Analysis

Failure analysis (FA) was done after ESD stress using scanning electron microscopy (SEM). Fig. 12 shows

TABLE I
ESD ROBUSTNESS

STRESS MODE	QSCR		GGNMOS	
	HBM	MM	HBM	MM
V_{DD1}-V_{SS1}	>8KV	600V	>8KV	600V
V_{DD1}-V_{SS2}	>8KV	600V	5KV	250V
V_{DD2}-V_{SS2}	>8KV	600V	>8KV	600V
V_{DD2}-V_{SS1}	>8KV	600V	5KV	250V

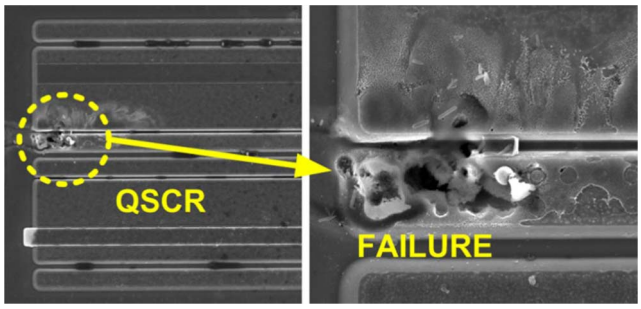

Fig. 12. FA image of the QSCR after a cross-domain 650 V MM stress. Failure is located inside the QSCR structure.

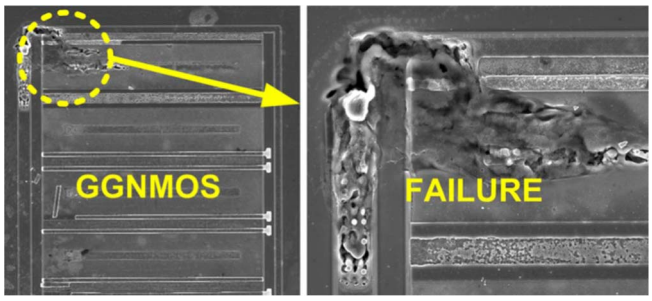

Fig. 13. FA image of the comparison circuit (Fig. 1) after a same-domain 650 V MM stress. Failure is located in the power-rail ESD clamp device (GGNMOS).

the FA image for the QSCR after the cross-domain 650 V MM stress. The failure is located inside the QSCR structure, whereas the interface transistors were not damaged. The failure location is consistent for the other stress cases.

For the comparison circuit, failure location after same-domain MM stress occurs in the power-rail ESD clamp (GGNMOS), as shown in Fig. 13. For cross-domain ESD stresses under both HBM and MM models, the failure in the comparison circuit is located on the interface circuit. Fig. 14 shows the typical image of such damage after a cross-domain 6 kV HBM stress, which is located on the gate oxide of the inverter at the receiver side.

V. DISCUSSION

The area efficiency of the QSCR greatly depends on the design specification, which includes a minimum holding voltage and a maximum trigger voltage. The addition of diode strings and external trigger circuit have a considerable impact on the total area utilization.

The CR circuit shown in Figs. 5 and 7 was done to maintain symmetry and simplicity, and it is not the most area efficient design. Removing one of the resistors would cause an

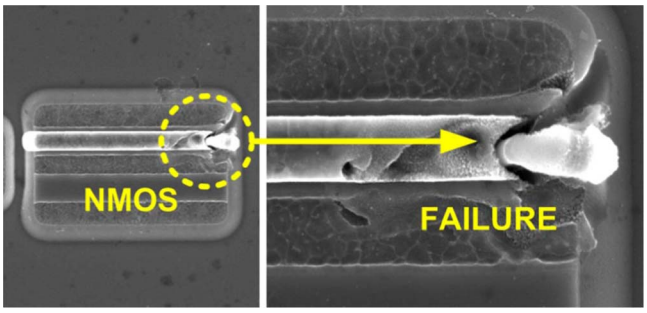

Fig. 14. FA image of the comparison circuit (Fig. 1) after a cross-domain 6 kV HBM stress. Failure is located on the gate oxide of the inverter at the receiver side of the interface circuit.

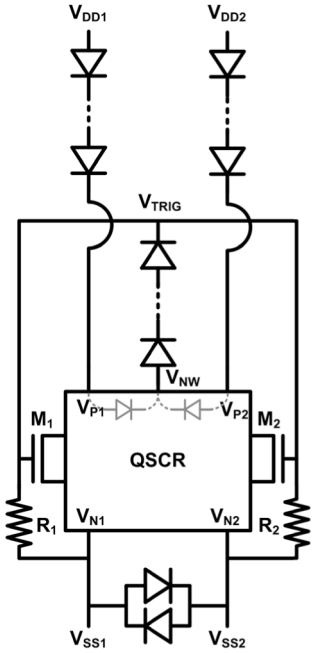

Fig. 15. QSCR with alternative trigger design formed by a diode string (from V_{NW} to V_{TRIG}).

unsymmetrical trigger voltage for the same- and cross-domain ESD stresses, but the circuit would have a larger equivalent RC constant, which leads to area utilization. Moreover, the capacitor size could be reduced using the circuital technique [25]. In addition, the CR trigger design can be further changed by the diode-string-based ESD detection circuit since it is more area efficient [26]. This can be easily achieved by replacing the capacitor C by a diode string, as shown in Fig. 15. The trigger voltage will be $(N + M) \times V_D + V_{TH}$, whereas N is the number of diodes between V_{DD1} and V_{p1}, M the number of diodes in the trigger path (from V_{NW} to V_{TRIG}), V_D is the diode voltage drop, and V_{TH} is the NMOS threshold voltage. For example, for the case of the QSCR implemented in the 0.25-μm CMOS process, using $N = 4$ and $M = 4$, the QSCR trigger voltage will be 7.2 V. By such a modified design, the silicon area can be further reduced.

Very fast TLP (vf-TLP) is an important device-level tool to verify the performance of the ESD device for protection against CDM events. The vf-TLP used in this work is with a pulsewidth of 5 ns and a rise time of 200 ps. Fig. 16 shows the vf-TLP measured results for the QSCR with four diodes

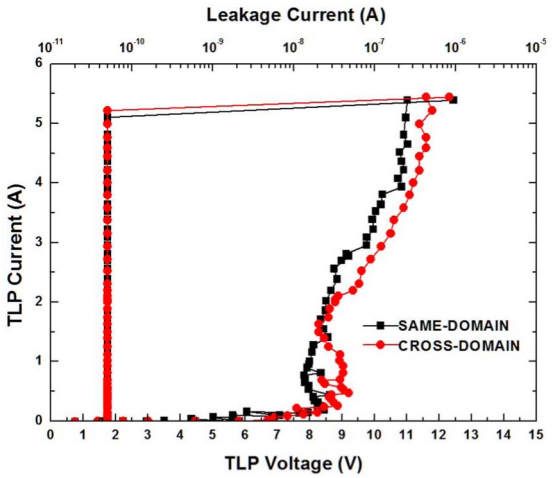

Fig. 16. vf-TLP I–V curves of the QSCR with four diodes in the diode strings and with CR trigger.

in the diode strings and with a CR trigger. Compared with the 100-ns TLP measured results in Fig. 11, the aparent higher holding voltage and larger turn-on resistance (Ron) under vf-TLP in Fig. 16 are attributed to the slow turn-on speed of the SCR. The QSCR fabricated in this work has shallow trench isolation (STI) formations inside its structure, thus the turn-on time of the SCR paths would be too slow for CDM protection. To further improve the turn-on speed of the SCR paths for CDM ESD protection, the dummy-gate structure should be applied to the QSCR and the diodes to block the STI regions [27], [28].

VI. Conclusion

QSCR was proposed as an effective ESD clamp for separated power domains. By integrating four SCRs, it can achieve full-direction ESD current paths for the same- and cross-domain ESD stresses, thus simplifying considerably the ESD protection design. Different circuit topologies were analyzed in order to have a comprehensive ESD protection design that can be easily adapted to different technologies and applications. The QSCR has been also verified with a silicon chip in a 0.25-μm CMOS process. The implemented device was able to pass ESD stresses of 8-kV HBM and 600-V MM ESD tests while successfully protecting the interface circuit between two separated power domains.

Acknowledgment

The authors would like to thank Vanguard International Semiconductor Corporation, especially K. Nidhi and G.-L. Lin for chip fabrication and measurement support.

References

[1] E. A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*. New York, NY, USA: Wiley, 2002.
[2] W. D. Greason, Z. Kucerovsky, and K. W. K. Chum, "Latent effects due to ESD in CMOS integrated circuits: Review and experiments," *IEEE Trans. Ind. Appl.*, vol. 29, no. 1, pp. 88–97, Jan./Feb. 1993.
[3] Y. Huh *et al.*, "A study of ESD-induced latent damage in CMOS integrated circuits," in *Proc. IEEE Int. Rel. Phys. Symp.*, Mar./Apr. 1998, pp. 279–283.
[4] J. Wu, P. Juliano, and E. Rosenbaum, "Breakdown and latent damage of ultra-thin gate oxides under ESD stress conditions," in *Proc. EOS/ESD Symp.*, Sep. 2000, pp. 287–295.
[5] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 173–183, Jan. 1999.
[6] P. Heydari and M. Pedram, "Jitter-induced power/ground noise in CMOS PLLs: A design perspective," in *Proc. Int. Conf. Comput. Design*, 2001, pp. 209–213.
[7] D. Flynn, A. Gibbons, R. Aitken, and K. Shi, *Low Power Methodology Manual: For System-on-Chip Design*. New Work, NY, USA: Springer, 2007.
[8] E. R. Worley, "Distributed gate ESD network architecture for inter-power domain signals," in *Proc. EOS/ESD Symp.*, Sep. 2004, pp. 1–10.
[9] M.-D. Ker, H.-H. Chang, and T.-Y. Chen, "ESD buses for whole-chip ESD protection," in *Proc. IEEE Int. Symp. Circuits Syst.*, Jul. 1999, pp. 545–548.
[10] N. Kitagawa, H. Ishii, J. Watanabe, and M. Shiochi, "An active ESD protection technique for the power domain boundary in a deep submicron IC," in *Proc. EOS/ESD Symp.*, 2006, pp. 196–204.
[11] S. H. Chen, M.-D. Ker, and H. P. Hung, "Active ESD protection design for interface circuits between separated power domains against cross-power-domain ESD stresses," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 3, pp. 549–560, Sep. 2008.
[12] M. Okushima, "ESD protection design for mixed-power domains in 90 nm CMOS with new efficient power clamp and GND current trigger (GCT) technique," in *Proc. EOS/ESD Symp.*, 2006, pp. 205–213.
[13] A. Chatterjee and T. Polgreen, "A low-voltage triggering SCR for on-chip ESD protection at output and input pads," in *VLSI Technol. Dig. Tech. Papers*, Jun. 1990, pp. 75–76.
[14] A. Chatterjee and T. Polgreen, "A low-voltage triggering SCR for on-chip ESD protection at output and input pads," *IEEE Electron Device Lett.*, vol. 12, no. 1, pp. 21–22, Jan. 1991.
[15] M.-D. Ker, C.-Y. Wu, H.-H. Chang, T. Cheng, and T.-S. Wu, "Complementary-LVTSCR ESD protection scheme for submicron CMOS IC's," in *Proc. IEEE Int. Symp. Circuits Syst.*, Apr./May 1995, pp. 833–836.
[16] X. Wang *et al.*, "Cross-coupling low-triggering dual-polarity CLTdSCR ESD protection in CMOS," *IEEE Electron Device Lett.*, vol. 31, no. 10, pp. 1143–1145, Oct. 2010.
[17] S. H. Voldman, *Latchup*. Hoboken, NJ, USA: Wiley, 2007.
[18] T. Maloney and N. Khurana, "Transmission line pulsing techniques for circuit modeling of ESD phenomena," in *Proc. EOS/ESD Symp.*, 1985, pp. 49–54.
[19] S. H. Voldman, G. Gerosa, V. P. Gross, N. Dickson, S. Furkay, and J. Slinkman, "Analysis of snubber-clamped diode-string mixed voltage interface ESD protection network for advanced microprocessors," *J. Electrostatics*, vol. 38, nos. 1–2, pp. 3–31, Oct. 1996.
[20] T. J. Maloney and S. Dabral, "Novel clamp circuits for IC power supply protection," *IEEE Trans. Compon., Packag., Manuf. Technol. C*, vol. 19, no. 3, pp. 150–161, Jul. 1996.
[21] M.-D. Ker, Y.-W. Hsiao, and W.-L. Wu, "ESD-protection design with extra low-leakage-current diode string for RF circuits in SiGe BiCMOS process," *IEEE Trans. Device Mater. Rel.*, vol. 6, no. 4, pp. 517–527, Dec. 2006.
[22] C.-Y. Lin, P.-H. Wu, and M.-D. Ker, "Area-efficient and low-leakage diode string for on-chip ESD protection," *IEEE Trans. Electron Devices*, vol. 63, no. 2, pp. 531–536, Feb. 2016.
[23] *Standard Test Method for Electrostatic Discharge (ESD) Sensitivity Testing: Human Body Model (HBM)—Component Level*, Standard ANSI/ESDA/JEDEC JS-001-2014, 2014.
[24] *Standard Test Method for Electrostatic Discharge (ESD) Sensitivity Testing: Machine Model (MM)—Component Level*, Standard JEDEC JESD22-A115C, 2010.
[25] F. A. Altolaguirre and M.-D. Ker, "Area-efficient ESD clamp circuit with a capacitance-boosting technique to minimize standby leakage current," *IEEE Trans. Device Mater. Rel.*, vol. 15, no. 2, pp. 156–162, Jun. 2015.
[26] F. A. Altolaguirre and M.-D. Ker, "Power-rail ESD clamp circuit with diode-string ESD detection to overcome the gate leakage current in a 40-nm CMOS process," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3500–3507, Oct. 2013.
[27] M.-D. Ker and K.-C. Hsu, "SCR device fabricated with dummy-gate structure to improve turn-on speed for effective ESD protection in CMOS technology," *IEEE Trans. Semicond. Manuf.*, vol. 18, no. 2, pp. 320–327, May 2005.
[28] W.-Y. Chen, E. Rosenbaum, and M.-D. Ker, "Diode-triggered silicon-controlled rectifier with reduced voltage overshoot for CDM ESD protection," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 1, pp. 10–14, Mar. 2012.

Federico A. Altolaguirre received the B.S. degree from the Universidad Nacional del Sur, Bahia Blanca, Argentina, and the M.S. degree form National Chiao Tung University, Hsinchu, Taiwan, where he is currently pursuing the Ph.D. degree with the Institute of Electronics.

His current research interests include ESD protection design and I/O circuit design.

Ming-Dou Ker (F'08) received the Ph.D. degree from the Institute of Electronics, National Chiao Tung University (NCTU), Hsinchu, Taiwan, in 1993.

He is currently a Distinguished Professor with the Department of Electronics Engineering, NCTU, and also the Director of the Biomedical Electronics Translational Research Center.

Dr. Ker is serving as the Editor of the IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY.