A CMOS-Process-Compatible Low-Voltage Junction-FET With Adjustable Pinch-Off Voltage

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***Abstract*— A novel horizontal n-channel junction field-effect transistor (n-JFET) device is proposed and verified in a 0.25-μm bulk CMOS process. This horizontal JFET consists of alternating n- and p-regions formed by using the P-type electro-static discharge (ESD) implantation. P-type ESD implantation has been an optional and commonly well supported process step by most of foundries to improve ESD robustness of the I/O devices. Device parameters such as the pinch-off voltage (V_P) and the zero-bias drain current (I_{DS0}) of the proposed n-JFET device can be modified by adjusting the P+ separation (L) in the layout. With the adjustable pinch-off voltages, this device can be used for different circuit applications. The 2-D device simulations with technology computer aided design are used to analyze the depletion region and to verify the pinch-off voltage under different L values. The pinch-off voltage remains almost unchanged with the temperature variations. In addition, SPICE simulation results show good agreement with the experimental silicon (Si) data in term of I_D–V_D and I_D–V_G.**

***Index Terms*— CMOS process, ESD implantation, junction field-effect transistor (JFET), pinch-off voltage (V_p), SPICE, zero-bias drain current (I_{DS0}).**

I. Introduction

NOWADAYS, the major challenges in the semiconductor are not only to continuously improve in product quality, reliability, and zero defects but also to minimize the complexity in the process to achieve greater functionality and higher performance with high operating speed [1]. As the number of transistors per chip increases with each technology node, the manufacturing cost per transistor falls by approximately 25% every year. However, due to growing complexity, process maintenance for transistors becomes a daunting task for semiconductor foundries. The junction field-effect transistor (JFETs) would probably be the simplest voltage-controlled (i.e., small change in input voltage causes a large change in output current) unipolar device with an electrical field to control its channel current [2], [3]. JFETs usually have fast switching speed and are virtually free of the problems like limited bandwidth, popcorn noise, complex design procedure to optimize noise performance, and high distortions. JFETs are suitable for low-noise amplifiers at low and medium frequencies, for charge sensitive amplifiers, for high input impedance amplifiers, and can be applied as controllable feedback elements. FETs are continued to be a preferred favorable choice for many analog applications due to their low price, high input impedance, and wide operating temperature range (−200 °C to +125 °C) along with a broad range of operation from dc to ultrahigh frequency [4], [5]. The major concern for JFET device is normally ON, even if there is no voltage applied to the gate. So, in order to switch JFET device OFF, a negative voltage (i.e., pinch-off voltage) applied to the gate must be large enough to switch the gate OFF [2]–[12].

Recently, a number of approaches have been reported to improve the performance for JFET devices. The improved silicon-on-insulator (SOI)-based enhanced mode JFET structure for ultralow-power applications offered low threshold voltage [6]. A shallow body and a JFET region with a smaller width and higher doping concentration were proposed to reduce the JFET's resistance and gate–drain charge density [7]. Enhanced ON to OFF current performance was shown in a vertical SOI-based enhancement mode JFET structure with improved gate control [8]. Few structures with uniformed body and ion-implanted JFETs (high doping concentration at JFET region than epitaxial layer) were proposed to reduce the threshold voltage variations and the specific on-resistance [9], [10]. A segmented JFET in a low-voltage planer power MOSFET were proposed to reduce the gate–drain charge density of the structure [11]. A "bottom gate/deep N-well (NW) junction" JFET structure using CMOS triple well isolation, deep (NW), to isolate the bottom gate from a substrate was demonstrated for low capacitance and high breakdown voltage [12]. An embedded JFET in an n-channel laterally diffused metal-oxide semiconductor (n-LDMOS) in HV LDMOS process provided an adjustable and wide range of pinch-off voltages [13]. Since different designs currently available for JFET devices are usually embedded in a MOS structure and their pinch-off voltage varies from −10 to −40 V. The pinch-off voltage of conventional JFET is dominated by junction depth [4]–[17]. Therefore, it is unlikely to provide different pinch-off voltages of the JFET in the same chip.

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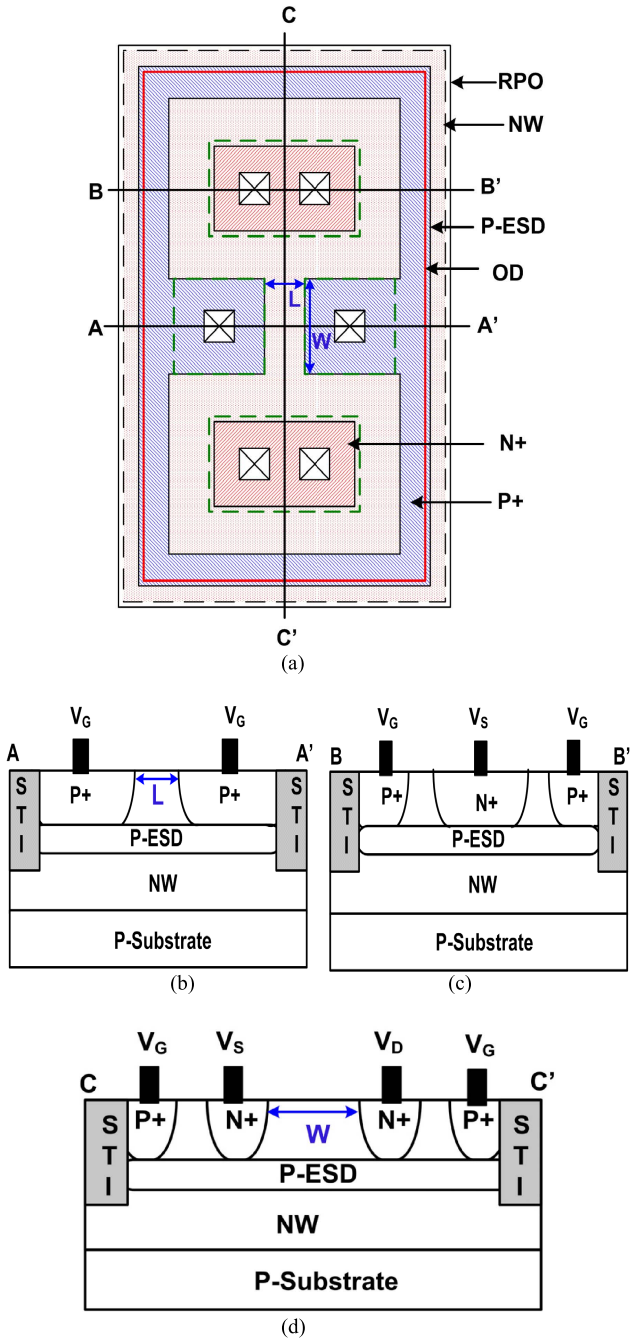


Fig. 1. (a) Layout top view of the proposed n-channel horizontal JFET structure and the different cross-sectional views along (b) A-A', (c) B-B', and (d) C-C' regions.

JFETs are hard to be implemented in bulk CMOS process. Actual implementations often require extra masks added into the CMOS process.

In this paper, a horizontal n-channel JFET device for low-voltage applications is proposed and realized in bulk CMOS process. Its performance has been successfully verified in silicon to provide a designable and adjustable pinch-off voltage to meet different circuit applications. This paper is organized as follows. Section II describes novel JFET device structure along with numerical model and technology computer aided design (TCAD) simulation for

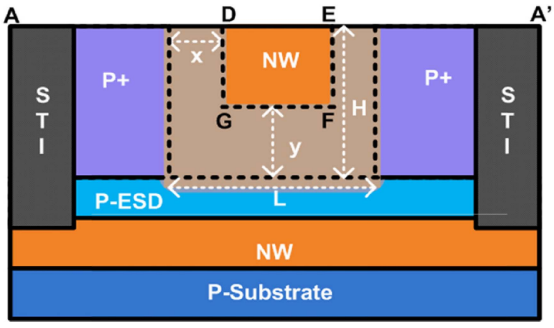


Fig. 2. Cross-sectional view of depletion distribution along A-A' region.

pinch-off voltage. This is followed by results and discussions in Section III. In Section IV, a conventional physics-based SPICE model is used to draw a comparison between SPICE simulation and the experimental silicon data for I_D–V_D and the pinch-off voltages [18]–[22]. Section V includes a discussion and comparison among the existing JFETs and the proposed bulk silicon-based LV JFET structure. Finally, Section VI draws the major conclusions of this work.

II. Device Structure

Fig. 1(a) shows the layout top view of the proposed horizontal n-type JFET. The device consists of the NW implantation over the p-type substrate. Fig. 1(b)–(d) shows cross-sectional views of the proposed structure across A-A', B-B', and C-C' regions, respectively. The channel is formed by isolating the upper part of the NW with the p-type ESD implantation (P-ESD).

Technology scaling which leads to thinner gate oxides, shallower junctions, thin epi substrates, high doping densities, silicided formation, etc., has caused negative impact on ESD immunity of CMOS devices. These challenges can be overcome by reoptimization of protection devices themselves or by novel on-chip ESD protection designs [23]–[25]. ESD implantations play an important role, as both of the P-type and the N-type ESD implantations were used in the MOS devices to create a higher ESD robustness [26]. Many experimental results from various technologies were reported with the effectiveness among those ESD implantation methods of CMOS chip [25]–[29]. In order to enhance ESD robustness, both of the N-type and P-type ESD implantations were used in nMOS devices. The N-type ESD implantation was used to cover the lightly doped drain peak structure and to make a deeper junction in nMOS device for better ESD robustness. On the contrary, the P-type ESD implantation with a higher doping concentration located under the drain junction of nMOS was used to reduce the junction breakdown voltage, and to earlier trigger on the parasitic lateral n-p-n bipolar junction transistor of the nMOS [27]–[32]. The ESD robustness of CMOS chips can be effectively improved by the ESD implantation methods, and most of foundries have already included ESD implantation layer into their CMOS processes.

The P+ ring is used to isolate the upper part of the NW. Two ohmic electrical connections in the N+ regions are used for the source/drain contacts as shown in Fig. 1(c), whereas

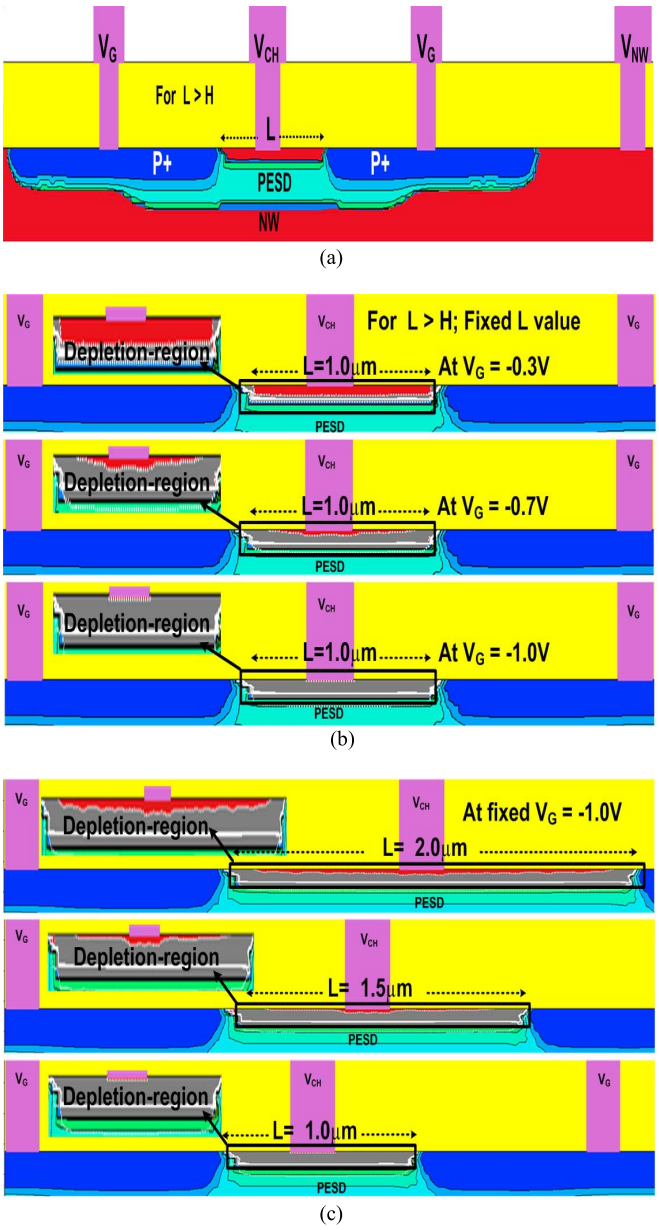


Fig. 3. (a) 2-D TCAD simulated structure of JFET under $L = 1$ μm, (b) depletion region at different V_G under a fixed channel length ($L = 1$ μm), and (c) depletion region at a fixed ($V_G = 1$ V) for different channel length ($L = 1$, 1.5, and 2 μm).

the P+ regions are used for the gate contacts forming a P-n junction with the main channel. The P+ ring is thicker in the channel region to create a shorter channel length (L) in the device. Thus, the device pinch-off voltage can be adjusted by varying L. The channel width (W) is kept minimum to have small channel resistance. Since the P-ESD implantation is shallower than the STI, a combination of OD and resist protection oxide (RPO) (used to block the silicided diffusion) masks (those are standard masks in the bulk CMOS process) are used to block the STI formation inside the JFET structure. The key advantage of the proposed structure is to obtain different pinch-off voltages in the same chip by changing in the separation between the P+ gates.

Fig. 2 shows the depletion region in the proposed JFET channel for a given voltage, where the separation between

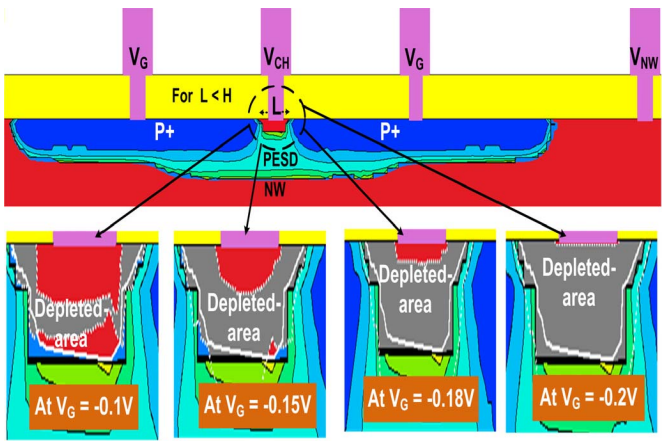


Fig. 4. 2-D TCAD simulated view for depleted area under different gate voltages for $L < H$.

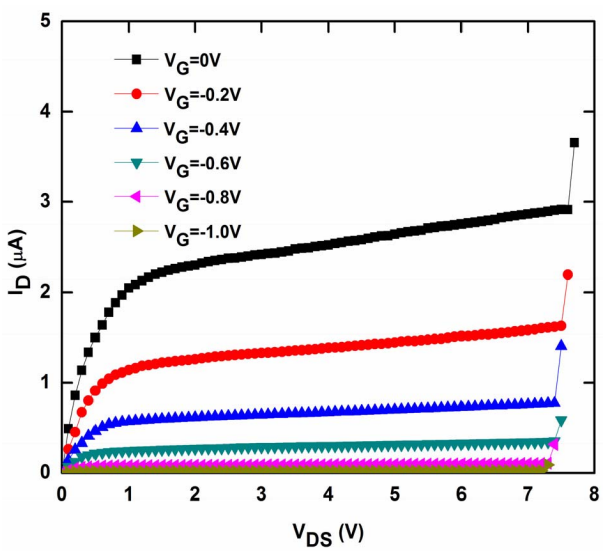


Fig. 5. Measured drain current (I_D) versus drain voltage (V_{DS}) at different V_G under $L = 2$ μm.

two gates and the distance from the silicon surface to P-ESD is denoted by L and H, respectively. The depletion region between the P+/NW junction denoted by x can be expressed as

$$x = x_0\sqrt{1 - V_{G1}/\phi_{B1}}, \quad \text{for } N_{P+} \gg N_{\text{NW}} \tag{1}$$

where

$$x_0 \approx \sqrt{2\varepsilon_S\phi_{B1}/qN_{\text{NW}}} \tag{2}$$

where N_{P+} and N_{NW} are the doping concentrations for the P+ and the NW implantations, respectively. V_{G1} is the applied voltage, ϕ_{B1} is the built-in voltage, q is the electron charge, and ε_S is the permittivity in the semiconductor.

Similarly, the depletion region at P-ESD/NW junction denoted by y can be expressed as

$$y = y_0\sqrt{1 - V_{G2}/\phi_{B2}}, \quad \text{for } N_{\text{P-ESD}} \approx N_{\text{NW}} \tag{3}$$

where

$$y_0 \approx \sqrt{\varepsilon_S\phi_{B2}/qN_{\text{NW}}} \tag{4}$$

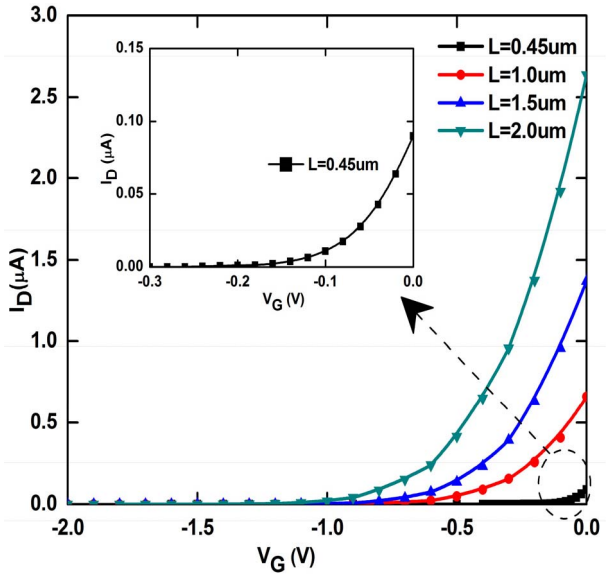


Fig. 6. Measured I_D–V_G characteristics of the proposed horizontal n-channel JFET at $V_{DS} = 5$ V with different values of L.

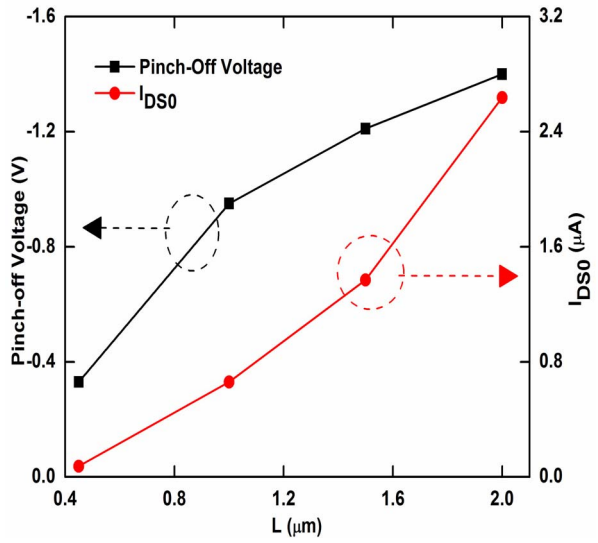


Fig. 7. Measured relation between the pinch-off voltage (V_p) and the zero-bias drain current (I_{DS0}) with respect to L.

where N_{P-ESD} is the doping concentration of P-ESD implantation, V_{G2} is the applied voltage at P-ESD/NW junction, and ϕ_{B2} is the built-in voltage.

From Fig. 2, DE $= L - 2x$ and EG $=$ H$-$y, are the nondepleted NW region. To determine the pinch-off voltage of device, the area of the nondepleted NW region is expressed as

$$[(L - 2x)(H - y)] = 0. \tag{5}$$

If L is larger than H, the device will reach the pinch-off voltage only when L gets fully depleted. So, V_{PL} (pinch-off voltage due to L) will be dominated by L at the P+/NW junction. The depletion region can be approximated as $L = 2x$ from Fig. 2.

TABLE I
PINCH-OFF VOLTAGE COMPARISON FOR MEASURED SILICON WITH 2-D TCAD SIMULATION

Channel Length (L)	V_p (V), measured from Wafer	V_p (V), simulated in TCAD
L=2.0μm	-1.40	-1.40
L=1.5μm	-1.21	-1.24
L=1.0μm	-0.95	-1.0V
L=0.45μm	-0.33	-0.35V
L=0.25μm	-	-0.2V

TABLE II
PINCH-OFF VOLTAGE VARIATION WITH TEMPERATURE

Temperature (°C)	-25	25	75	125
V_p under L=1.0μm	-1.0V	-0.95V	-1.0V	-1.0V
V_p under L=1.5μm	-1.22 V	-1.21V	-1.21V	-1.22V
V_p under L=2.0μm	-1.41 V	-1.40V	-1.41V	-1.40V

Hence, from (1), we can get

$$V_{PL} = \phi_{B1}\left[1 - \left(L^2/4x_0^2\right)\right]. \tag{6}$$

For the case of $L < H$, V_{PH} (pinch-off voltage due to H) will be dominated by H at P-ESD/NW junction. H needs to be depleted to reach the pinch-off voltage. The depletion region can be approximated as $y = H$ from Fig. 2.

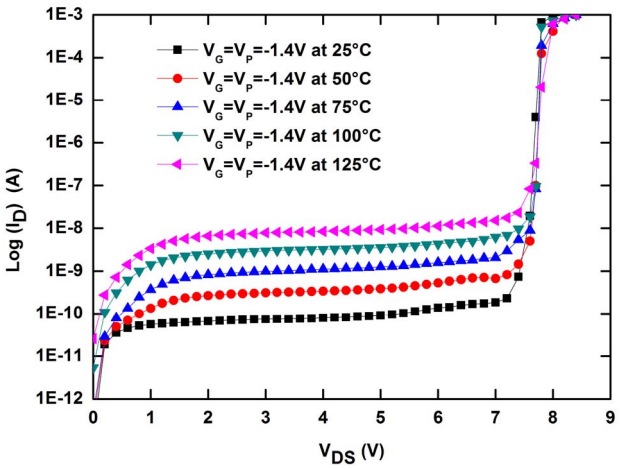
From (3), V_{PH} is defined as

$$V_{PH} = \phi_{B2}\left[1 - \left(H^2/y_0^2\right)\right]. \tag{7}$$

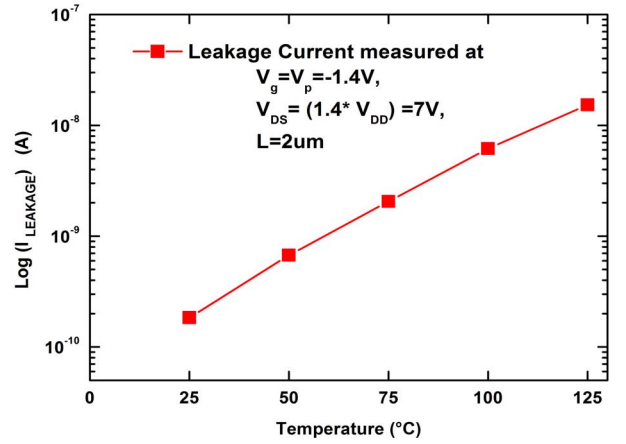
From (6), different pinch-off voltages can be designed and achieved by varying L in the layout when L is greater than H. Equation (7) refers that the pinch-off voltage will be dominated by diffusion depth of P-ESD implantation when L is smaller than H.

The 2-D TCAD simulations were performed using TSUPREM and Medici to obtain a clear insight into the device structural characteristics. The depletion region of the device and the pinch-off voltage conditions were analyzed and compared for different L values.

Fig. 3(a) shows the 2-D TCAD structure for net doping concentration under $L = 1.0$ μm. An extra contact (V_{CH}) is added for TCAD simulation which is set to 0 V. V_G is connected to the P+ regions and V_{NW} is contacted to the NW region outside the channel. The NW is used only for isolation and could be any voltage higher than V_G to avoid the leakage current ($V_{NW} = 5$ V for simulation). Fig. 3(b) shows the depletion region for a fixed channel length ($L = 1$ μm). The channel region starts to deplete at $V_G = -0.3$ V and almost fully depleted at $V_G = -1$ V. For the device channel length higher than H, depletion along L will dominate as shown in Fig. 3(b) and (c). At a fixed gate voltage (in this case $V_G = -1$ V), the devices under $L = 1.5$ and 2 μm are



(a)



(b)

Fig. 8. (a) Measured log drain current (Log I_D) versus drain voltage (V_{DS}) at different temperatures and (b) variation in leakage current with respect to temperatures under a fixed $V_{DS} = 7$ V.

TABLE III
DEFAULTS AND OPTIMIZED PARAMETERS FOR JFET MODEL

Model Parameters	Optimized Value	Default Value
VTO (Pinch-off)	-1.44 V	-2 V
I_S (Saturation current)	1e-10 A	1e-14 A
R_S (Source resistance)	100 ohm	0 ohm
R_D (Drain resistance)	100 ohm	0 ohm
BETA (Transconductance coefficient)	0.16μA/ volt^2	100 μA/volt^2
Lamda (Channel length modulation)	0.051 V^{-1}	0 V^{-1}
C_{GD} (Gate-Drain cap.)	0.3pF	0 F
C_{GS} (Source-Drain cap.)	0.2pF	0 F

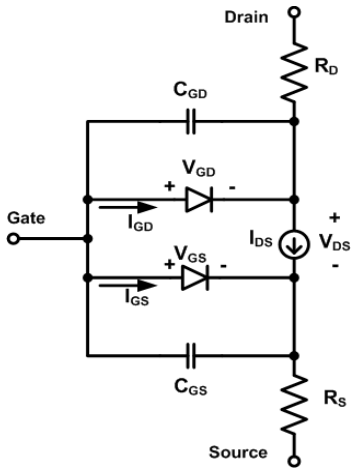


Fig. 9. Equivalent circuit representation of conventional n-channel JFET.

partially depleted. The device under $L = 1$ μm is almost depleted completely as shown in Fig. 3(c). Different gate voltages are required to deplete the device channel region completely for different L values.

Fig. 4 shows the depletion process for the channel length smaller than H under different gate voltages ($V_G = -0.1$ to -0.2 V) for a fixed L value ($L = 0.25$ um). The channel region of the device almost is fully depleted at $V_G = -0.2$ V. Depletion along H is responsible for achieving the pinch-off voltage of the JFET structure.

III. Experimental Result and Discussion

The proposed horizontal n-type JFET had been fabricated in a 0.25-μm 5 V bulk CMOS process with the additional mask layer of p-type ESD implantation, which is commonly supported by most of foundries. Some test devices were made with different L values (0.45, 1.0, 1.5, and 2.0 μm) under a fixed W value ($W = 1.1$ μm).

Fig. 5 shows the measured I_D–V_{DS} plot of the n-JFET under $L = 2$ μm. A change in V_G can be used to control the current through source–drain channel from its maximum (saturated) value to zero current. It has been found that the current amplitude between two consecutive gate voltages is not equal as V_G varies from 0 to -1 V with V_S grounded, because the depletion region width varies as square root of the applied voltage. For the device with the smallest value of L (0.45 μm) in this paper, drain saturation current levels are very low (order of 10^{-8}) under different gate bias (V_G) voltages. Drain saturation current increases significantly for $L = 1.0$, 1.5, and 2.0 μm.

Fig. 6 shows the I_D versus V_G measurements for four devices with different L values. Measurements were performed with V_D fixed at 5 V and V_S is grounded. The pinch-off voltage (V_P) and the zero-bias drain current (I_{DS0}) are -0.33 V and 0.074 μA, respectively, when L is 0.45 μm.

Fig. 7 shows the dependence of the pinch-off voltage and the zero-bias drain current (I_{DS0}) with respect to L. It can be inferred from Fig. 7 that the pinch-off voltage will saturate for larger L values while the zero-bias drain current increasing almost exponentially from 0.08 to 2.6 μA.

Table I shows the comparison of pinch-off voltages between measured and the 2-D TCAD simulated results for different L values. The dependence on the pinch-off voltage and the zero-bias drain current with respect to L gives design

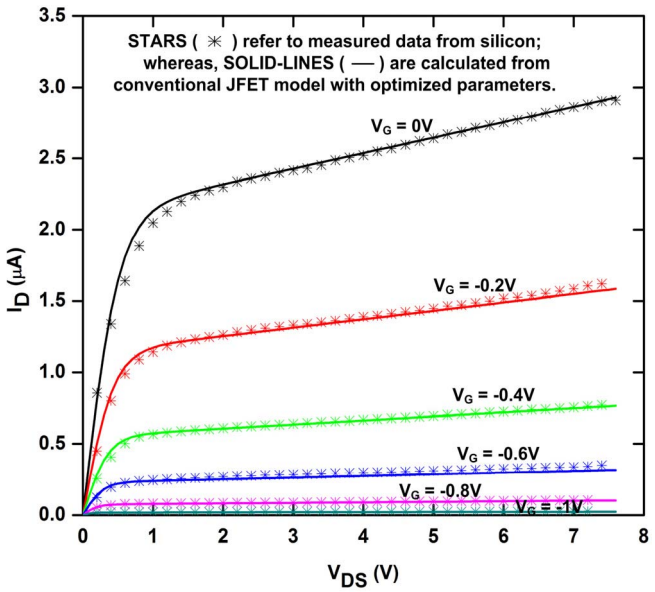


Fig. 10. Compare for measured I_D–V_{DS} and curve extracted from a conventional JFET model in SPICE with optimized parameters at different V_G under $L = 2$ μm.

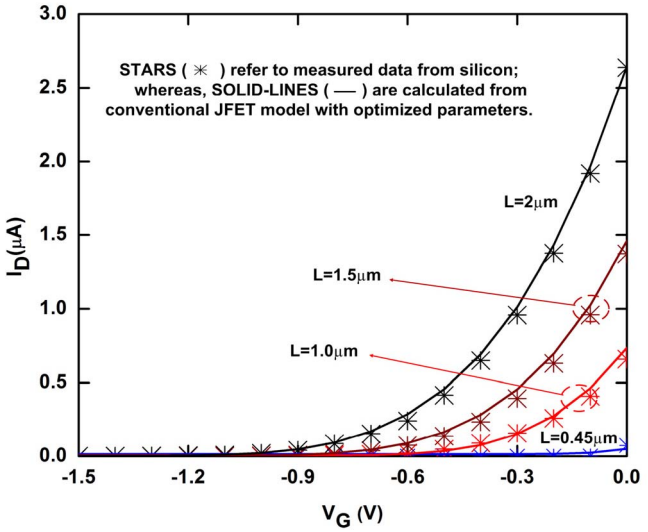


Fig. 11. I_D–V_G curves comparison with measured data from silicon and SPICE model for different values of channel length (L).

TABLE IV
COMPARISON AMONG THE PROPOSED JFET AND THE EXISTING JFETS

Parameters	Proposed JFET (this work)	SOI based JFET [6], [8]	BCD based JFETs [7], [9]-[17]
Bulk Si compatible	Yes	No	Few
Additional mask required	P-ESD Implantation	Yes	Yes
Variable pinch-off voltages in same chip	Yes	No	Few with additional masks
Cost-effective	Yes	No	No
Temperature variation	Negligible	High	Low ~ Middle
ESD susceptible	Less	More	Less
Breakdown Voltage	7.6V	HV range	5~8V (FOR LV)

flexibility and allows the proposed n-JFET for different applications.

Table II shows the variation in the pinch-off voltage under different temperatures for $L = 1$, 1.5, and 2 μm. The change in the pinch-off voltage with respect to the temperature is almost negligible.

Fig. 8(a) shows Log (I_D) versus V_{DS} curve at a fixed gate voltage for different temperatures. Measurements were performed with $V_G = V_p = -1.4$ V (off-state mode) for $L = 2$ μm. Fig. 8(b) shows the variation in the leakage current with respect to temperature at a fixed $V_{DS} = 1.4 \times V_{DD} = 7$ V under $L = 2$ μm. It can be inferred from Fig. 8(b) that the Log leakage current [Log ($I_{LEAKAGE}$)] varies linearly with rise in temeratures for a fixed V_{DS}. The breakdown voltage of the proposed device is 7.6 V. The breakdown voltage of the device is not affected by a change in separation between the P+ (L in Fig. 2) because the breakdown point occurs at the N+ and P-ESD junction.

IV. JFET SPICE MODEL

SPICE is the most widely used circuit simulation tool in the semiconductor industries for analog circuit simulation and design due to its device physics-based sophisticated device model and yield accurate representation of the device terminal behaviors [18]–[20]. The proposed horizontal n-type JFET is considered for implementation in the conventional JFET SPICE model. Fig. 9 shows the physics-based voltage-controlled current source conventional JFET model. It consists of two p-n junctions across gate–source and gate–drain, respectively. Two linear resistors R_D and R_S are used for modeling as ohmic resistances of the drain and source regions [18]–[22]. The SPICE model parameters are extracted from the device by using an Agilent B1500A semiconductor device parameter analyzer. Table III shows a comparison between optimized and default parameters for conventional JFET model for $L = 2$ μm.

The simulation results from conventional model are validated by comparing with the experimental results obtained on JFET samples. Fig. 10 shows the comparison between measured I_D–V_{DS} and SPICE simulated data of n-JFET under $L = 2$ μm. Measured data is almost matched with SPICE simulation result.

Fig. 11 shows that the I_D–V_G curves between SPICE simulated and measured silicon data have reasonably good agreement under different channel lengths. Different pinch-off zero-bias threshold voltage (VTO) values are used for different values of L (V_p measured from wafer in Table I) to simulate I_D–V_G in SPICE.

V. DISCUSSION

Earlier reported BCD compatible JFET structures generally required additional masks to standard process and segmented

from MOS structures [7], [9]–[17]. In case of low-voltage JFET structure, where the pinch-off voltage is small, a slight variation in dose and energy of implants can cause a significant variation in the pinch-off voltage of device [10]–[12], [15]. The proposed JFET structure in this paper is fully porcess compatible to general CMOS process with the ESD-implanation layer. In addition, the proposed JFET structure can achieve various pinch-off voltages in the same chip by simply adjusting P+ separation in the device layout. Recently, SOI-based JFET structure has been gaining popularity irrespective of high cost in volume production [6], [8]. However, most of SOI JFETs often suffered the problem from the heat build up in the device due to insulating silicon oxide in buried oxide layer, which is poor heat conductor and prevents effective heat dissipation into bulk silicon below the buried oxide layer. A comparison among the proposed low-voltage JFET structure and other existing JFET structures is shown in Table IV.

VI. Conclusion

A horizontal n-type JFET device has been proposed and successfully verified in silicon, which can be implemented in the standard bulk CMOS processes with P-type ESD implantation. Moreover, the proposed JFET device enables to adjust its pinch-off voltage (V_P) and zero-bias drain current (I_{DS0}) via layout modification. Measurement results have verified that different pinch-off voltages can be accommodated in the same chip. Simulation results from the conventional SPICE model shows good agreement with the experimental data. The proposed JFET device can be used as an ON/OFF switch for controlling electrical power to a load when its size is suitably scaled.

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