A High-Voltage-Tolerant and Precise Charge-Balanced Neuro-Stimulator in Low Voltage CMOS Process

Zhicong Luo, *Student Member, IEEE*, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*—This paper presents a $4 \times V_{DD}$ neuro-stimulator in a 0.18-μm 1.8 V/3.3 V CMOS process. The self-adaption bias technique and stacked MOS configuration are used to prevent transistors from the electrical overstress and gate-oxide reliability issue. A high-voltage-tolerant level shifter with power-on protection is used to drive the neuro-stimulator The reliability measurement of up to 100 million periodic cycles with 3000-μA biphasic stimulations in 12-V power supply has verified that the proposed neuro-stimulator is robust. Precise charge balance is achieved by using a novel current memory cell with the dual calibration loops and leakage current compensation. The charge mismatch is down to 0.25% over all the stimulus current ranges (200–300 μA) The residual average dc current is less than 6.6 nA after shorting operation.**

***Index Terms*—Charge balance, current memory cell, high-voltage-tolerant, leakage current compensation, level shifter, stimulator.**

I. Introduction

THERE are ~1% of the people in the world affected by the epilepsy. Typically, the epilepsy is treated with the anti-epileptic drugs. However, there are still many patients who cannot be cured by the medications. For these medically refractory patients, implantable deep brain stimulation (DBS) is another alternative [1]. When the people with epilepsy have a sudden seizure, the seizure detector of the DBS system detects the overload of electrical activity in the brain, and then the neuro-stimulator delivers charges into the brain tissue via electrodes [2]. If sufficient charges are injected into the working electrodes, it will depolarize the membrane of the tissue to the threshold, and produce a unidirectional propagating action potential signal to prevent the epilepsy seizure.

However, an improperly designed neuro-stimulator may cause damage to the tissue. There are two major classes of the mechanisms. The first proposed mechanism is the mass action theory which shows that tissue damage is caused by the intrinsic biological processes as excitable tissue is over stimulated [3].

The second proposed mechanism for tissue damage is the charge imbalance or the residual average dc current. This mechanism shows that tissue damage is caused by the toxic electrochemical reaction products at the electrode surface. The level of the residual average dc current at which tissue damage begins to occur has been widely studied. Aran *et al.* reported that the tissue in guinea pig cochleae was damaged with the residual average dc current levels of 20–40 μA for stimulus periods of up to 24 hours [4]. Hurlbert *et al.* reported that there was no pathological change in the vicinity of the stimulating electrodes with the residual average dc current level of 1.5 μA to stimulate the rat spinal cord for stimulus periods of up to 12 weeks. But, there was significant pathological change including inflammation and fibrosis at the electrode surface with the residual average dc current level of 3 μA to stimulate the rat spinal cord [5]. Shepherd *et al.* reported that the chronic intracochlear electrical stimulation, using charge-balanced biphasic current with the residual average dc current of less than 0.1 μA, does not damage the tissue in the cochlea [6], [7]. In consideration of the human safety, the specified industry limit of the residual average dc current in cochlear implants is 25 nA [8].

There are several methods to achieve charge balance, e.g., inserting a large dc blocking capacitor in series with each electrode and the active charge balancer. But, they are detrimental for the implantable devices because of increasing the area and hardware complexity. The current-controlled passive charge balancer is another solution. Biphasic current stimulation with the inter-phase delay is generally used for charge balance purpose. A typical current-controlled passive charge balancer consists of only current sink or source [9], [10]. But the charge imbalance can be caused by the leakage currents due to the crosstalk between the adjacent stimulating channels *in vitro* testing [11]–[13]. Another passive charge balancer which consists of both current source and sink with matched currents can avoid the crosstalk between the adjacent stimulating channels. H. Chun *et al.* reported such a charge balanced stimulator [13], which is achieved by employing a dynamic current mirror at the output of stimulator. But the matched accuracy of the dynamic current mirror is impaired by the capacitive division, charge injection, clock feedthrough, channel length modulation, and so on [14]. J.-J. Sit *et al.* reported another stimulator whose residual average dc current is less than 6 nA. It employs two steps strategy to achieve charge balance [15].

Manuscript received July 27, 2015; revised October 20, 2015 and December 01, 2015; accepted December 21, 2015. Date of publication March 24, 2016; date of current version December 30, 2016. This work was supported in part by the Ministry of Science and Technology (MOST), Taiwan, under Contracts of MOST 103-2221-E-009-197-MY2 and MOST 104-2220-E-009-004. This paper was recommended by Associate Editor P. Chiang.

The authors are with the Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, and also with the Biomedical Electronics Translational Research Center, National Chiao-Tung University, Hsinchu 300, Taiwan (e-mail: luozhicong.ee02g@nctu.edu.tw; mdker@ieee.org).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TBCAS.2015.2512443

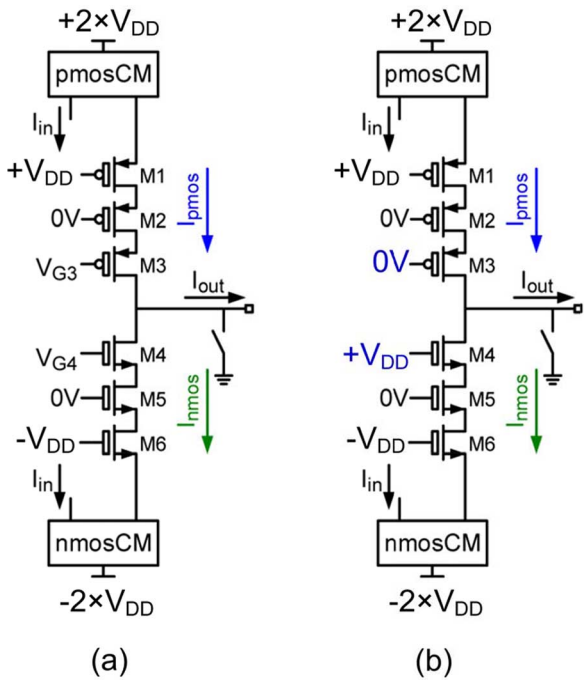

Fig. 1. (a) Stimulator using stacked LV transistors reported in [25]. (b) The stimulator with bias voltages during anodic phase.

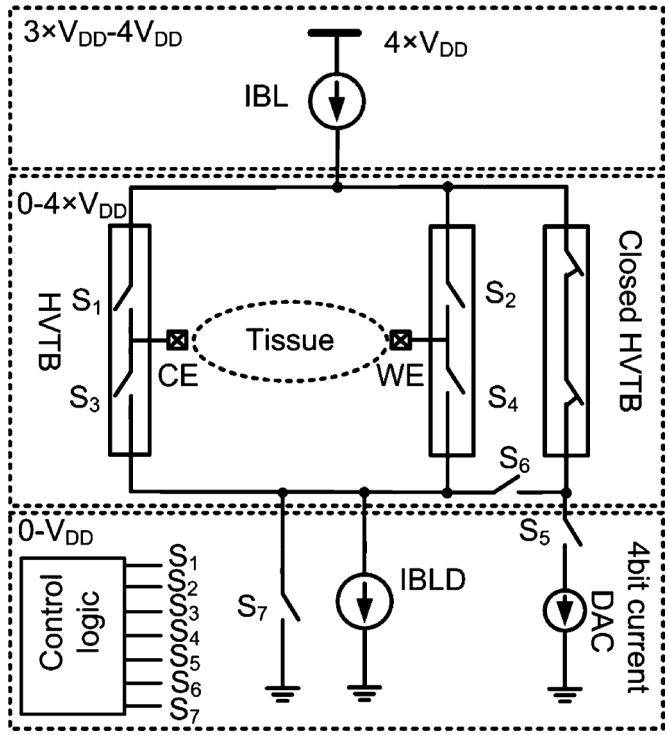

Fig. 2. Block schematic of the proposed neuro-stimulator.

The neuro-stimulator should inject an appropriate amount of charges into the electrodes to ensure efficacious stimulation, and the required supply voltage is typically much higher than that of the low voltage (LV) CMOS process [16], [17]. One approach is to use the high voltage (HV) process at the expense of the area and power consumption [18]–[22]. The other approach is to use the concept of stacked devices with the dynamic bias voltage to tolerate the high supply voltage. One of the advantages of this approach is that it can be fully integrated with the digital signal processor in a digital technology without extra process [1], [2], [16], [23], [24]. However, in the prior designs, the dynamic bias voltages were set according to the stimulation phase. The stimulator shown in Fig. 1(a) is an example with such a technique, which was reported in [25]. As shown in Fig. 1(b), during the anodic phase, the gate voltage (V_{G3}) of transistor M3 is set to 0 V. However, during the cathodic phase, V_{G3} is set to $-V_{DD}$. When the stimulator operates in the normal status, the stimulator is robust. But, if the output of the stimulator is accidentally shorted to the passive power supply $(2 \times V_{DD})$ or to the negative power supply $(-2 \times V_{DD})$, some failures may occur because the voltages across the terminals of the transistors exceed to the nominal value. In consideration of the device reliability, the dynamic bias voltages can't be set according to the stimulation phase.

In this work, a neuro-stimulator with the self-adaption bias circuit is proposed. It employs four stacked transistors for the pull-down switch and the pull-up switch, respectively, to withstand 4 times the nominal supply voltage $(4 \times V_{DD})$ without affecting device reliability. In addition, it employs a novel basic current memory cell to provide 0.25% charge mismatch, and the residual average dc current is less than 6.6 nA with shorting operation after the biphasic stimulation.

II. Neuro-Stimulator System

A. Neuro-Stimulator System Block Diagram

The block schematic of the proposed charge-balanced neuro-stimulator is shown in Fig. 2. It consists of a basic current memory cell with the leakage current compensation (IBL), basic current memory cell with the dual calibration loops and leakage current compensation (IBLD), 4-bit current DAC, control logic, $4 \times V_{DD}$ high-voltage-tolerant buffer (HVTB), and $4 \times V_{DD}$ closed high-voltage-tolerant buffer (closed HVTB). The IBLD, 4-bit current DAC, and control logic operate from 0 V to V_{DD}, the HVTB and closed HVTB operate from 0 V to $4 \times V_{DD}$, and the IBL operates from $3 \times V_{DD}$ to $4 \times V_{DD}$.

The IBL and IBLD are the novel current memory cells with sample-and-hold technique. Their output currents are more constant over time than that of the basic current memory cell. The detailed strategy and functions of the IBL and IBLD will be described in Section III. The HVTB consists of four stacked transistors for the pull-down switch and the pull-up switch, respectively. It can withstand $4 \times V_{DD}$ without affecting device reliability. The detailed strategy and functions of HVTB will be described in Section IV. The closed HVTB is the same as the HVTB, except which switches always be turned on. The 4-bit current DAC performs the function of the current reference, and the output current varies from 200 μA to 3000 μA according to the control signals.

B. Neuro-Stimulator Operating Sequence

The stimulator is designed to generate biphasic current pulses shown in Fig. 3. Once the stimulator becomes active, it is operating with 5 phases in the one-cycle biphasic stimulation. During phase 1 (calibration stage), S_5 is firstly turned

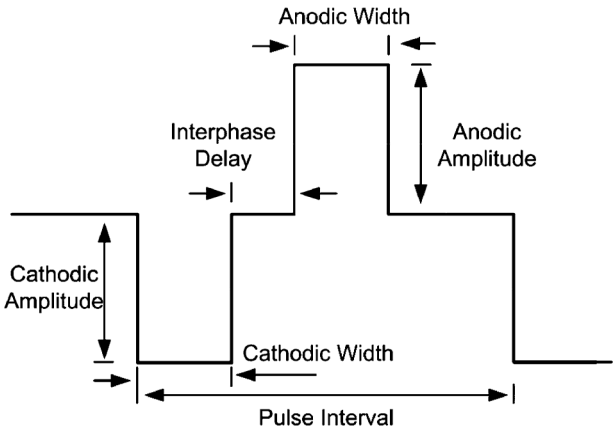

Fig. 3. Biphasic current pulse with interphase delay.

on, and all of the other switches are turned off, the output current $(\mathrm{I_{DAC}})$ of the 4-bit current DAC is sampled by the IBL. Secondly, $\mathrm{S_5}$ is turned off, and the output current of the IBL is roughly matched to the $\mathrm{I_{DAC}}$ because of the channel charge injection and clock feedthrough caused by the switches. Thirdly, $\mathrm{S_6}$ is turned on, the output current $(\mathrm{I_{IBL}})$ of the IBL is sampled by the IBLD. Fourthly, $\mathrm{S_6}$ is turned off, and the output current of the IBLD is precisely matched to the $\mathrm{I_{IBL}}$ with low power dissipation. During phase 2 (cathodic stimulation stage), $\mathrm{S_2}$, $\mathrm{S_3}$, $\mathrm{S_5}$, $\mathrm{S_6}$ and $\mathrm{S_7}$ are turned off, $\mathrm{S_1}$ and $\mathrm{S_4}$ are turned on, and cathodic current flows as such, IBL $\rightarrow$ $\mathrm{S_1}$ $\rightarrow$ CE $\rightarrow$ tissue $\rightarrow$ WE $\rightarrow$ $\mathrm{S_4}$ $\rightarrow$ IBLD. During phase 3 (interphase delay stage), all of the switches are turned off. During phase 4 (anodic stimulation stage), $\mathrm{S_1}$, $\mathrm{S_4}$, $\mathrm{S_5}$, $\mathrm{S_6}$, and $\mathrm{S_7}$ are turned off, $\mathrm{S_2}$ and $\mathrm{S_3}$ are turned on, and anodic current flows as such, IBL $\rightarrow$ $\mathrm{S_2}$ $\rightarrow$ WE $\rightarrow$ tissue $\rightarrow$ CE $\rightarrow$ $\mathrm{S_4}$ $\rightarrow$ IBLD. During phase 5 (shorting stage), $\mathrm{S_1}$, $\mathrm{S_2}$, $\mathrm{S_5}$, and $\mathrm{S_6}$ are turned off, $\mathrm{S_3}$, $\mathrm{S_4}$, and $\mathrm{S_7}$ are turned on, so the anodic and cathodic electrodes are shorted to ground.

III. Strategy to Achieve Precise Current Match

A. Current Error With Basic Current Memory Cell

The schematic of the basic current memory cell is shown in Fig. 4, which is a simple sample-and-hold circuit. The voltage at the drain of $\mathrm{M_{A1}}$ is set to $\sim$ $\mathrm{V_{TH}}$ (threshold voltage of the transistor $\mathrm{M_{A2}}$) by employing the active cascode circuit. During the sample mode, $\mathrm{S_{A1}}$ and $\mathrm{S_{A2}}$ are turned on, and $\mathrm{S_{A3}}$ is turned off. The input current (I_{in}) is sampled at the memory capacitor $(\mathrm{C_H})$. During the hold mode, $\mathrm{S_{A1}}$ and $\mathrm{S_{A2}}$ are turned off, and $\mathrm{S_{A3}}$ is turned on. The current I_{in} is copied to the output current (I_{out}) [26].

However, the accuracy of the basic current memory cell is impaired by the parasitic components. The dotted components in Fig. 4 represent the parasitic components of the basic current memory cell, where g_{ds} represents the channel length modulation of the transistor $\mathrm{M_{A1}}$, it's negligible because the drain-source voltage of $\mathrm{M_{A1}}$ is set to $\sim$ $\mathrm{V_{TH}}$ in the operating phase. Neglect the effect of the well diode.

The circuit of Fig. 4 operates in three phases, including sample phase, hold phase, and working phase.

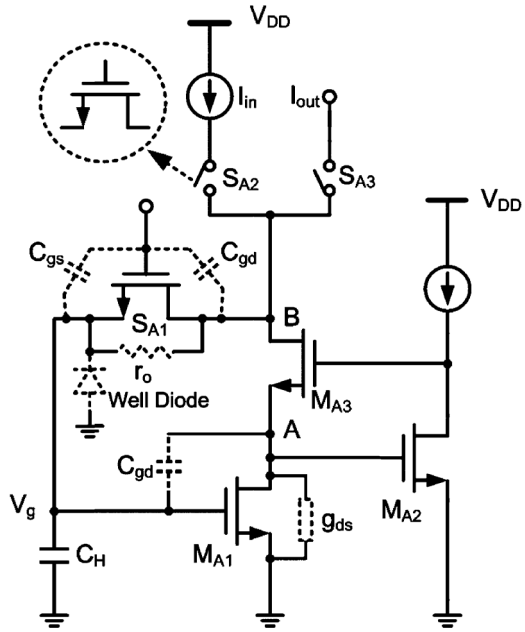

Fig. 4. Basic current memory cell with parasitic.

At sample phase: Switches $\mathrm{S_{A1}}$ and $\mathrm{S_{A2}}$ are turned on, and switch $\mathrm{S_{A3}}$ is turned off. The voltage (V_g) on the $\mathrm{C_H}$ will reach the value required to support the drain current of $\mathrm{M_{A1}}$ equals to the $\mathrm{I_{in}}$ by charge or discharge the $\mathrm{C_H}$. When $\mathrm{S_{A1}}$ is turned off, a portion of the charge, due to the effect of channel charge injection and clock feedthrough, is injected into the $\mathrm{C_H}$, causing the voltage V_g to change by [27]

$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_g - V_{TH})}{2C_H} + V_{ck}\frac{WC_{ov}}{WC_{ov} + C_H} \tag{1}$$

where V_{ck} is the amplitude of the clock, C_{ov} is the overlap capacitance per unit width, and V_{DD} is the power supply voltage. In (1), the first item represents the effect of channel charge injection, and the second item represents the effect of clock feedthrough.

At hold phase $(0 < \mathrm{t} \leq \mathrm{T})$: Switches $\mathrm{S_{A1}}$, $\mathrm{S_{A2}}$, and $\mathrm{S_{A3}}$ are turned off. The voltages at nodes A and B are pulled down to 0 V. The finite off-state resistance of $\mathrm{S_{A1}}$ provides a current path to discharge the charges stored in the $\mathrm{C_H}$. At the same time, the voltage variation at the node A is transferred to the $\mathrm{C_H}$ by the capacitive coupling of $\mathrm{C_{gd}}$, causing the voltage V_g to change by

$$\Delta V(t) = \mathrm{V_g}\left(1 - \mathrm{e}^{-\frac{\mathrm{t}}{\mathrm{r_o C_H}}}\right) + \frac{C_{gd}V_{\mathrm{TH}}}{C_{gd} + C_{\mathrm{H}}} \tag{2}$$

where r_o is the off-state resistance of $\mathrm{S_{A1}}$. In (2), the first item represents the effect of the finite off-state resistance of $\mathrm{S_{A1}}$, the second item represents the capacitive coupling of $\mathrm{C_{gd}}$.

At the working phase: $\mathrm{S_{A1}}$ and $\mathrm{S_{A2}}$ are kept in the previous states, $\mathrm{S_{A3}}$ is turned on. The voltage at node A is pushed up to $\mathrm{V_{TH}}$. The voltage variation at the node A is transferred to the

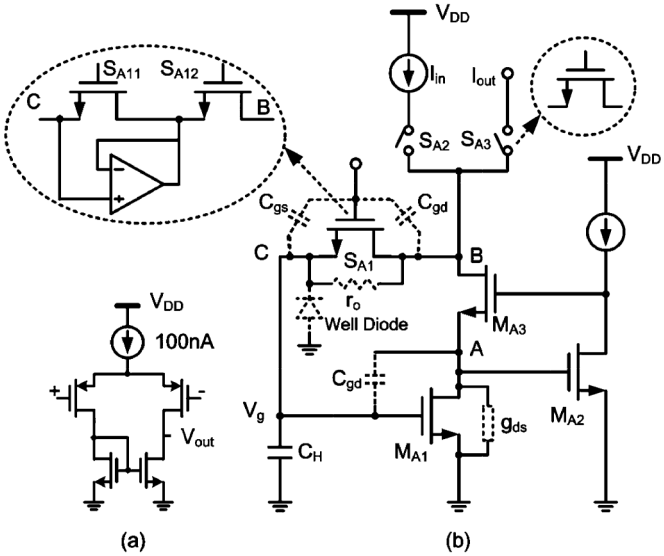

Fig. 5. (a) Basic current memory cell with leakage current compensation. (b) The simple schematic of the amplifier.

C_H by the capacitive coupling of C_{gd}, causing the voltage V_g to change by

$$\Delta V(t) = -\frac{C_{gd}V_{TH}}{C_{gd}+C_H}. \tag{3}$$

So, the total voltage error of V_g between the sample phase and working phase can be expressed approximately as

$$\Delta V = \frac{WLC_{ox}\left(V_{DD}-V_g-V_{TH}\right)}{2C_H} + V_{ck}\frac{WC_{ov}}{WC_{ov}+C_H} + V_g\left(1-e^{-\frac{T}{r_o C_H}}\right). \tag{4}$$

This voltage error (ΔV) results a current error between the I_{out} and I_{in}, which can be expressed approximately as

$$\Delta I = I_{out} - I_{in} = \Delta V \cdot g_m \tag{5}$$

where g_m is the transconductance of M_{A1}, which is evaluated at the operating current I_{in}. Equation (5) shows that the current error ΔI is proportional to the transconductance of M_{A1}. In other word, the larger off-state resistance of S_{A1} and the smaller input current I_{in} result a smaller current error ΔI.

B. Voltage Error With Leakage Current Compensation

Fig. 5(b) shows the proposed solution to lowering the effect of the finite off-state resistance of S_{A1} [28]. In Fig. 5(b), S_{A1} is replaced by the transistors S_{A11} and S_{A12}, and a unity gain amplifier with the bias current of ~100 nA is connected between the transistor S_{A11}. Fig. 5(a) shows the simple schematic of the amplifier. In this way, the drain-to-source voltage of S_{A11} is ~0 V. Thus, the leakage current caused by the finite off-state resistance is zero, and the leakage current flowing through S_{A12} is supplied by the amplifier. That means, the effect of the finite off-state resistance of S_{A1} is canceled, the total voltage error of V_g between the sample phase and working phase in the Section A can be expressed approximately as

$$\Delta V = \frac{WLC_{ox}(V_{DD}-V_g-V_{TH})}{2C_H} + V_{ck}\frac{WC_{ov}}{WC_{ov}+C_H}. \tag{6}$$

Equation (6) shows that only channel charge injection and clock feedthrough impair the voltage error.

C. Current Error With Dual Calibration Loops and Leakage Current Compensation

There are many methods to cancel the effect of the charge injection and clock feedthrough. But, each leads to other trade-offs, such as addition of dummy device, using of complementary switches, and using differential sampling circuit.

A charge-balanced stimulator which used low-leakage differential mode sample-and-hold circuit was reported in [15], where the input current I_{in} was fully sampled on a memory capacitor that resulted in a large transconductance g_m and a large current error ΔI, as shown in (5).

The proposed differential mode sample-and-hold circuit with the dual calibration loops and leakage current compensation is shown in Fig. 6(a). The first calibration loop consists of transistors (M_{B1}, M_{B2}, and M_{B3}), switch S_{B1}, and memory capacitor C_{B1}. The second calibration loop consists of transistors (M_{B4}, M_{B5}, and M_{B6}), switches (S_{B3}, S_{B4}, and S_{B5}), capacitors (C_{B2} and C_{B3}), and a differential amplifier. The second calibration loop is aimed to calibrate the current error caused by the first calibration loop, and it employs a differential operational amplifier along with two memory capacitors (C_{B2} and C_{B3}) to partially cancel the charge injection errors caused by the switches (S_{B3} and S_{B4}). In this way, the final current error will become smaller because the transconductance of M_{B4} is smaller, as shown in (5). The dotted switches in . 6(a) are the switches with the leakage current compensation. The differential operational amplifier is shown in . 6(b). The voltage at the positive terminal of the differential operational amplifier should be of low noise for reducing the drain-current noise of M_{B4}, thus it's supplied by a bandgap with resistor divider.

Let $(W/L)_1 : (W/L)_4 = N$, where $N \gg 1$. The circuit in Fig. 6(a) operates in three phases. At phase1: S_{B0}, S_{B1}, S_{B3}, and S_{B4} are turned on. S_{B2} and S_{B5} are turned off. Thus, the drain currents of M_{B1} and M_{B4} are $[N/(N+1)]\times I_{in}$ and $[1/(N+1)]\times I_{in}$, respectively.

At phase 2: S_{B1} turned off. S_{B0}, S_{B2}, S_{B3}, S_{B4}, and S_{B5} are kept in the previous states. When S_{B1} is turned off, a portion of the charge, due to the effect of the channel charge injection and clock feedthrough, is injected into the memory capacitor C_{B1}, causing the drain current of M_{B1} to change to$[N/(N+1)]\times I_{in}\pm\Delta I$. Meanwhile, the drain current of M_{B4} is changed to $[1/(N+1)]\times I_{in}\mp\Delta I$, automatically.

At phase 3: S_{B3} is turned off after S_{B4} does, and S_{B5} is turned on finally. S_{B0}, S_{B1}, and S_{B2} are kept in the previous states. By this way, the charge injected by S_{B3} is eliminated. The channel charge of S_{B4} results in a constant offset voltage at the input terminals of the differential operational amplifier when S_{B4} is turned off, but the charge injected by S_{B4} appears

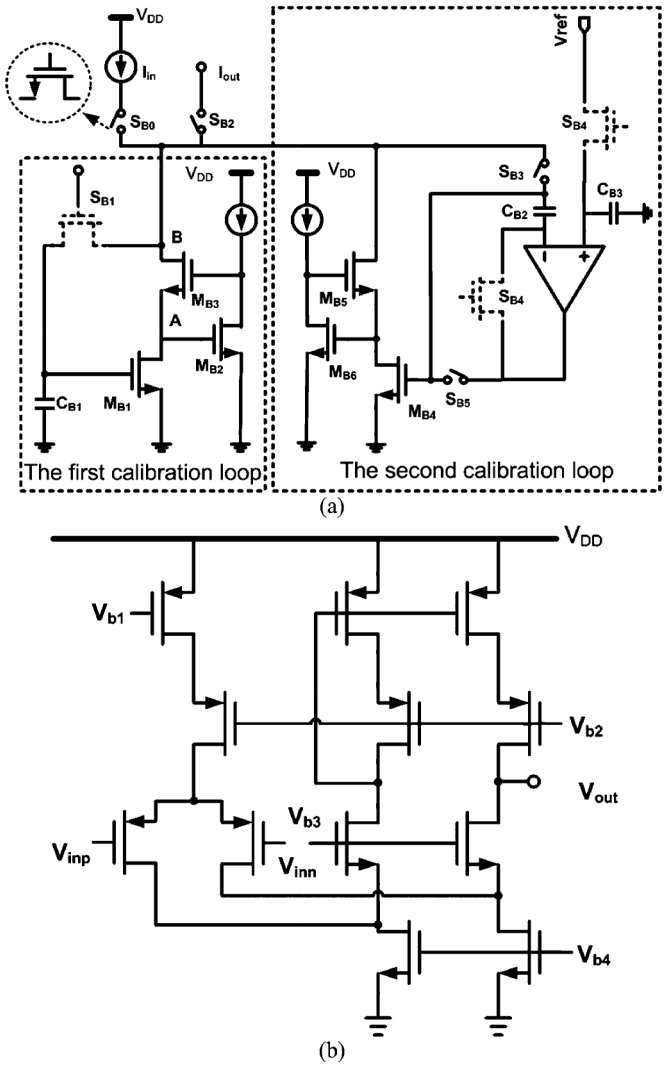

Fig. 6. (a) Basic current memory cell with leakage current compensation and dual calibration loops. (b) Differential operational amplifier.

as a common-mode disturbance. That is also eliminated. The precision of this circuit depends on the open loop gain of the differential operational amplifier. Referring to [25], it has

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx \frac{1}{1+A_V^{-1}} \tag{7}$$

where V_{in} is the gate voltage of M_{B4} at phase 2, V_{out} is the gate voltage of M_{B4} at phase 3, and A_V is the open loop gain of the differential operational amplifier. Thus, the gate voltage error of M_{B4} between phase 2 and phase 3 is about

$$\Delta V = V_{\text{out}} - V_{\text{in}} = \frac{V_{\text{in}}}{1+A_V}. \tag{8}$$

It results a small current error(ΔI) between I_{in} and I_{out}

$$\Delta I = I_{\text{out}} - I_{\text{in}} = \frac{V_{\text{in}}}{1+A_V} \cdot g_m \tag{9}$$

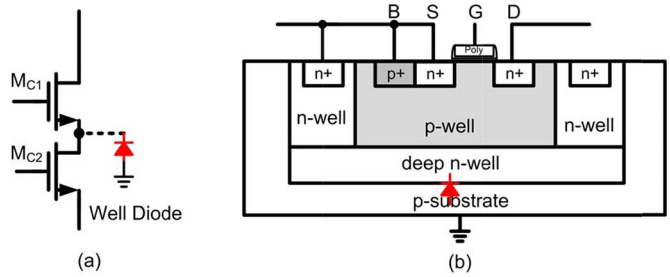

Fig. 7. (a) Principle of two stacked transistors. (b) NMOS devices with deep n-well layer and the parasitic well diode.

where g_m is the transconductance of M_{B4}, which is evaluated at the operating current $[1/(\text{N}+1)]\times\text{I}_{\text{in}}$. That means using dual calibration loops technique can decrease the total current error ΔI by the factor of $(\text{N}+1)$ compared with the sample-and-hold circuit reported in [15].

IV. Strategy to Achieve High-Voltage-Tolerant Buffer in Low Voltage CMOS Process

The proposed strategy is to employ stacked transistors to withstand the higher power supply voltage. An example of two stacked transistors is shown in Fig. 7(a), where the source of transistor M_{C1} is connected to the drain of the next transistor M_{C2}. By this way, the voltage across from the drain of the upper device M_{C1} to the source of the lower device M_{C2} can rise up to two times of the nominal supply $(2 \times \text{V}_{\text{DD}})$. In this topology, the gate bias of the transistors M_{C1} and M_{C2} should be carefully set, and the maximum voltage across the terminals of all transistors should be limited by the nominal supply voltage (V_{DD}). If n transistors are stacked, it can withstand n times the nominal supply voltage $(\text{n} \times \text{V}_{\text{DD}})$ without decreasing the transistors reliability [29]–[32].

However, the maximal voltage at the source of the upper devices M_{C1} in Fig. 7(a) is limited by the breakdown voltage of the parasitic well diode. For the triple-well technologies, the breakdown voltages of NMOS transistor with deep n-well layer, NMOS transistor without deep n-well layer, and PMOS transistor are limited by the n-well/p-substrate diode, $\text{n}+$/p-well diode, and n-well/p-substrate diode, respectively. The prior work reported that the breakdown voltage of the n-well/p-substrate diode is higher than that of the $\text{n}+$/p-well diode [30]. The proposed high-voltage-tolerant buffer is realized with the 3.3 V PMOS and NMOS transistors with the deep n-well layer to withstand a higher operation voltage, and all of the bodies of the transistors are connected to their source terminals.

A. $4 \times V_{DD}$ High-Voltage-Tolerant Buffer

Fig. 8 shows the detailed schematic of the $4 \times \text{V}_{\text{DD}}$ high-voltage-tolerant buffer with the self-adaption bias circuit and the nth V_{DD} bias circuit. PMOS transistors M_{BP1} to M_{BP4} and resistors R_1 to R_4 perform the function of the voltage divider. The sizes of the transistors and the resistance of the resistors are set to the same, so the gate voltage (V_{b2}) of M_{BBP1} is $(3 \times$ VDD $\text{V}_{\text{THP}})$. On the same principle, the gate voltage (V_{b1}) of M_{BBN1} is $(3 \times \text{V}_{\text{DD}} + \text{V}_{\text{THN}})$. Thus, the voltage at node b_1 is $3 \times \text{V}_{\text{DD}}$. The voltages at nodes b_2 and b_3 are $2 \times \text{V}_{\text{DD}}$

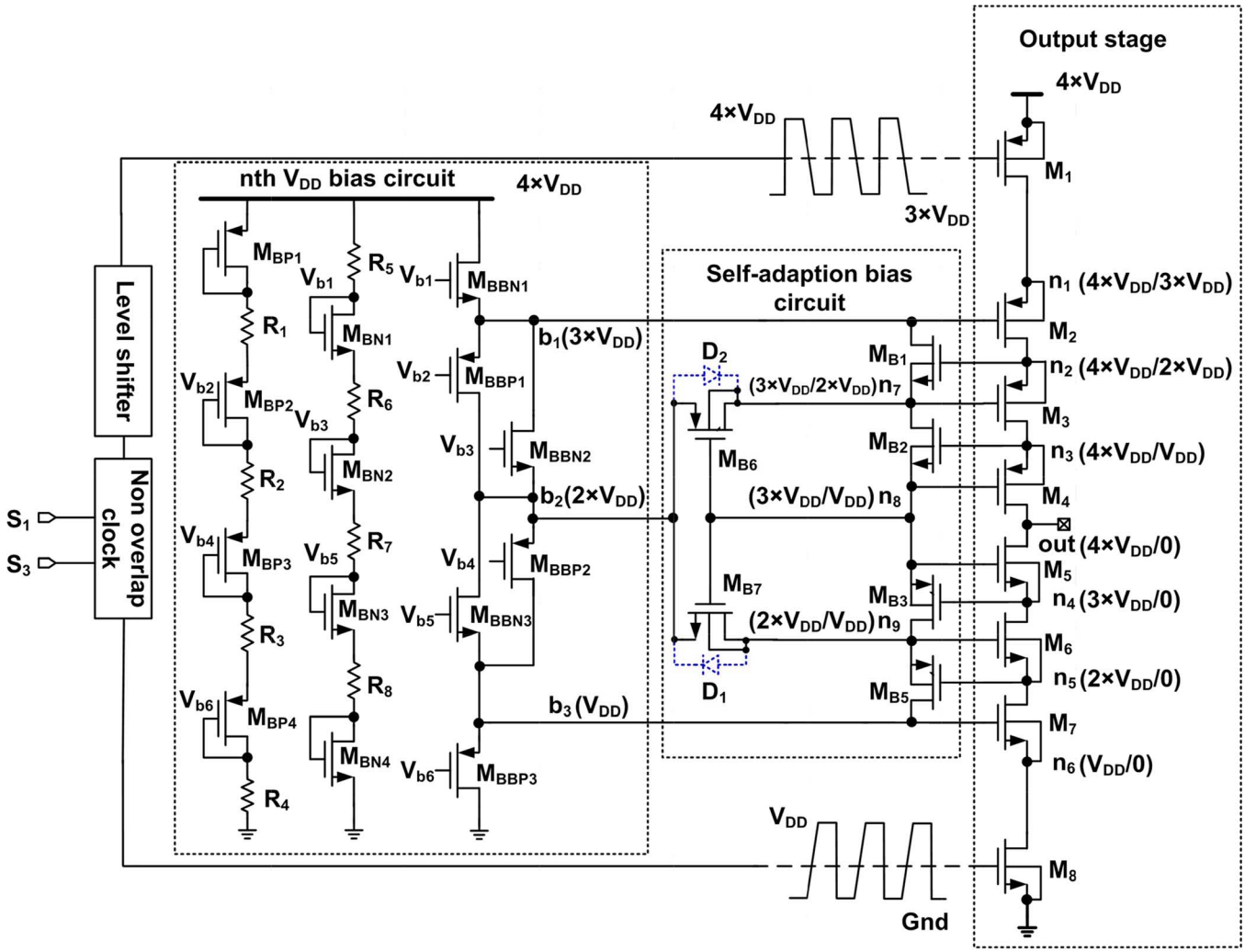

Fig. 8. The detailed schematic of $4 \times \mathrm{V_{DD}}$ high-voltage-tolerant buffer with transistor dimensions. The transistors $(\mathrm{M_1} \sim \mathrm{M_8})$ in the output stage have the identical geometrical dimension which is 80 μm/0.34 μm. In addition, the dimensions of the transistors $\mathrm{M_{B1}}, \mathrm{M_{B2}}, \mathrm{M_{B3}}, \mathrm{M_{B5}}, \mathrm{M_{B6}}$, and $\mathrm{M_{B7}}$ are 1 μm/1 μm, 1 μm/1 μm, 4 μm/0.5 μm, 4 μm/0.5 μm, 20 μm/0.34 μm, and 20 μm/0.34 μm, respectively, realized in a 0.18-μm CMOS process.

and $\mathrm{V_{DD}}$, respectively. Transistors $\mathrm{M_{BBN1}}$ and $\mathrm{M_{BBP1}}$ perform the function of the push-pull output stage which has low power dissipation in the standby condition. The output stage consists of four stacked transistors for the pull-down switch and the pull-up switch, respectively, to withstand $4 \times \mathrm{V_{DD}}$. A self-adaption bias circuit was designed to keep the voltages across the terminals of the stacked transistors within the nominal supply voltage $\mathrm{V_{DD}}$. The bodies of transistors $\mathrm{M_{B6}}$ and $\mathrm{M_{B7}}$ are connected to the nodes $\mathrm{n_7}$ and $\mathrm{n_9}$, respectively. If the voltage at node $\mathrm{n_7}$ tends to be less than $2 \times \mathrm{V_{DD}}$, or the voltage at node $\mathrm{n_9}$ tends to be higher than $2 \times \mathrm{V_{DD}}$, the parasitic diode ($\mathrm{D_2}$ or $\mathrm{D_1}$) turns on, thus the voltages at nodes $\mathrm{n_7}$ and $\mathrm{n_9}$ will be clamped to $2 \times \mathrm{V_{DD}}$. The high-voltage-tolerant buffer is controlled by the outer stacked transistors. The level shifter converts the low-level voltage to the high-level voltage with DC offset of 3 times $\mathrm{V_{DD}}$. A non-overlap clock circuit is used to drive the level shifter for avoiding the short-circuit current in the output stage of the high-voltage-tolerant buffer.

When the upper transistor $\mathrm{M_1}$ is turned on and the lower transistor $\mathrm{M_8}$ is turned off, the quiescent voltages at the nodes $\mathrm{n_1}$ to $\mathrm{n_9}$ are $4 \times \mathrm{V_{DD}}, 4 \times \mathrm{V_{DD}}, 4 \times \mathrm{V_{DD}}, 3 \times \mathrm{V_{DD}}, 2 \times \mathrm{V_{DD}}$, $\mathrm{V_{DD}}$, $3 \times \mathrm{V_{DD}}$, $3 \times \mathrm{V_{DD}}$, $2 \times \mathrm{V_{DD}}$, respectively. When the transistor $\mathrm{M_1}$ is turned off and transistor $\mathrm{M_8}$ is turned on, the quiescent voltages at the nodes $\mathrm{n_1}$ to $\mathrm{n_9}$ are $3 \times \mathrm{V_{DD}}$, $2 \times \mathrm{V_{DD}}$, $\mathrm{V_{DD}}$, 0 V, 0 V, 0 V, $2 \times \mathrm{V_{DD}}$, $\mathrm{V_{DD}}$, $\mathrm{V_{DD}}$, respectively. Thus, the voltages across the terminals of all the transistors are limited to the nominal supply voltage $\mathrm{V_{DD}}$.

When the output stage $(\mathrm{M_1} \sim \mathrm{M_8})$ switches from low (0 V) to high $(4 \times \mathrm{V_{DD}})$, the previous state of the quiescent voltages at the nodes $\mathrm{n_1}$ to $\mathrm{n_9}$ are $3 \times \mathrm{V_{DD}}$, $2 \times \mathrm{V_{DD}}$, $\mathrm{V_{DD}}$, 0 V, 0 V, 0 V, $2 \times \mathrm{V_{DD}}$, $\mathrm{V_{DD}}$, $\mathrm{V_{DD}}$, respectively. The control signals from the level shifter turn $\mathrm{M_1}$ on and $\mathrm{M_8}$ off, the circuit is operating with four phases. At phase 1: the node out is charged from 0 V to $\mathrm{V_{DD}}$. The voltages at nodes out, $\mathrm{n_4}$, $\mathrm{n_5}$, $\mathrm{n_6}$, $\mathrm{n_8}$, and $\mathrm{n_9}$ increase. When the node out is charged to $\mathrm{V_{DD}}$, transistor $\mathrm{M_7}$ will be turned off, and node $\mathrm{n_6}$ is finally charged to $\mathrm{V_{DD}}$. At phase 2: the node out is charged from $\mathrm{V_{DD}}$ to $2 \times \mathrm{V_{DD}}$. The voltages at nodes out, $\mathrm{n_4}$, $\mathrm{n_5}$, $\mathrm{n_8}$, and $\mathrm{n_9}$ increase. When the voltage at $\mathrm{n_5}$ increases to $(2 \times \mathrm{V_{DD}} - \mathrm{V_{THN}})$, transistor $\mathrm{M_{B5}}$ turns off and transistor $\mathrm{M_{B7}}$ turns on, thus $\mathrm{n_9}$ is charged to $2 \times \mathrm{V_{DD}}$ through

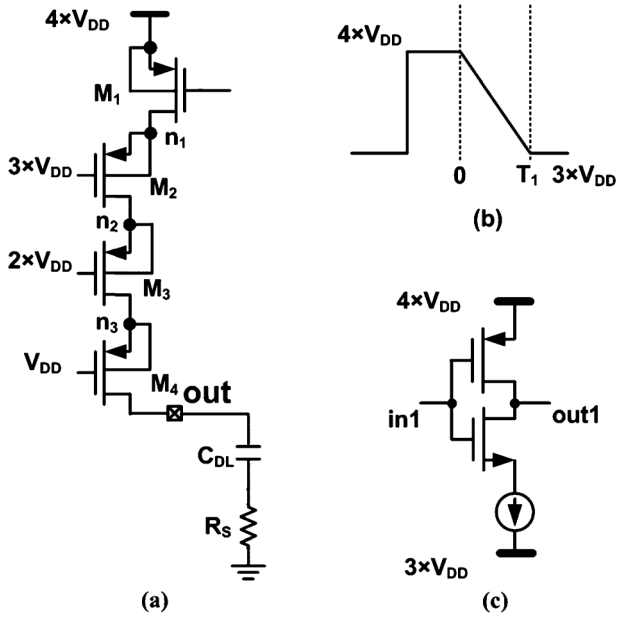

Fig. 9. (a) Simple schematic of the high-voltage-tolerant buffer with loading capacitor and resistor when it switches from 0 V to $\mathrm{V_{DD}}$. (b) The gate voltage of the transistor $\mathrm{M_1}$. (c) Simple schematic of driver for transistor $\mathrm{M_1}$.

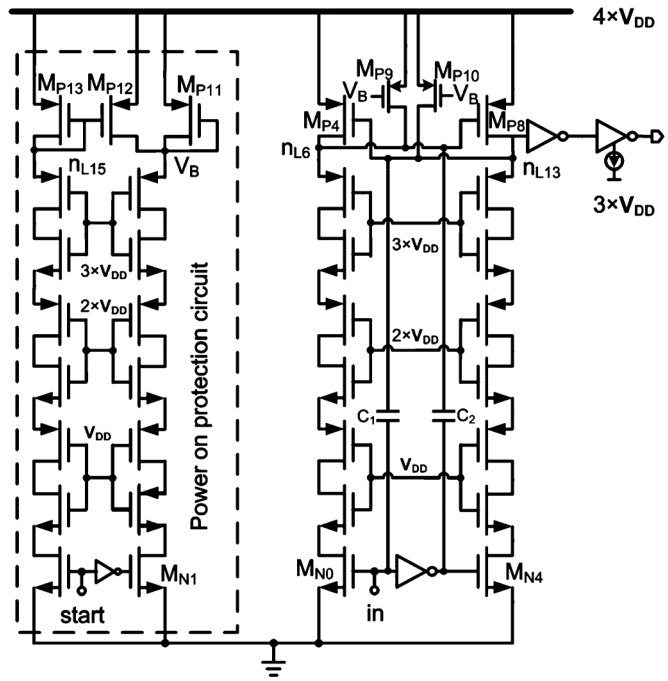

Fig. 10. High-voltage-tolerant level shifter with power-on protection.

transistor $\mathrm{M_{B7}}$. Then, transistor $\mathrm{M_6}$ will be turned off, and node $\mathrm{n_5}$ is finally charged to $2 \times \mathrm{V_{DD}}$. As a result, the voltages at nodes $\mathrm{n_7}$ and $\mathrm{n_8}$ increase. At phase 3: the node out is charged from $2 \times \mathrm{V_{DD}}$ to $3 \times \mathrm{V_{DD}}$. The voltages at nodes out and $\mathrm{n_4}$ increase, and transistors $\mathrm{M_5}$ and $\mathrm{M_{B3}}$ will be turned off. Finally, nodes $\mathrm{n_4}$, $\mathrm{n_7}$, and $\mathrm{n_8}$ are charged to $3 \times \mathrm{V_{DD}}$. At phase 4: the node out is charged from $3 \times \mathrm{V_{DD}}$ to $4 \times \mathrm{V_{DD}}$. Nodes $\mathrm{n_1}$, $\mathrm{n_2}$, and $\mathrm{n_3}$ are charged to $4 \times \mathrm{V_{DD}}$. The dimension of transistor $\mathrm{M_{B7}}$ should be larger than that of the $\mathrm{M_{B5}}$. The similar operation can be explained for the transition of the output stage from high $(4 \times \mathrm{V_{DD}})$ to low (0 V).

However, when the output stage switches from 0 V to $\mathrm{V_{DD}}$, the drain-to-source transient voltage of transistor $\mathrm{M_4}$ may exceed to the nominal supply. Fig. 9(a) shows the simple schematic of the high-voltage-tolerant buffer with the double layer capacitor $(\mathrm{C_{DL}})$ and the solution spreading resistance $(\mathrm{R_{SW}})$. When the output stage switches from 0 V to $\mathrm{V_{DD}}$, as described in the previous section, the gate voltages of transistors $\mathrm{M_2}$, $\mathrm{M_3}$, and $\mathrm{M_4}$ are $3 \times \mathrm{V_{DD}}$, $2 \times \mathrm{V_{DD}}$, and $\mathrm{V_{DD}}$, respectively. Assume that the gate voltage of transistor $\mathrm{M_1}$ is linearly discharged from $4 \times \mathrm{V_{DD}}$ to $3 \times \mathrm{V_{DD}}$ by the level shifter in the period of $\mathrm{T_1}$ seconds as shown in Fig. 9(b), and neglect the channel length modulation $(\lambda = 0)$, the voltage at the gate of transistor $\mathrm{M_1}$ can be expressed approximately as

$$V_{g1}(t) = -\frac{\mathrm{V_{DD}}}{T_1}t + 4\mathrm{V_{DD}}. \tag{10}$$

Because the drain currents of $\mathrm{M_1}$ and $\mathrm{M_4}$ are the same, the voltage at the source (node $\mathrm{n_3}$) of $\mathrm{M_4}$ can be expressed approximately as

$$V_{s4}(t) = \frac{\mathrm{V_{DD}}}{T_1}t + \mathrm{V_{DD}}. \tag{11}$$

So, the source-to-drain voltage of $\mathrm{M_4}$ can be expressed as

$$V_{sd4}(t) = \frac{\mathrm{V_{DD}}}{T_1}t + \mathrm{V_{DD}} - \left(I_D \cdot R_{SW} + \frac{I_D}{C_{DL}}t\right) \tag{12}$$

where I_D is the drain current of $\mathrm{M_1}$. However, if $\mathrm{C_{DL}}$ is large enough, and $\mathrm{R_{SW}}$ is small enough, and the gate voltage of transistor $\mathrm{M_1}$ is quickly discharged from $4 \times \mathrm{V_{DD}}$ to $3 \times \mathrm{V_{DD}}$ (T_1 approximates to 0), the drain-to-source transient voltage of transistor $\mathrm{M_4}$ is approximated to $2 \times \mathrm{V_{DD}}$. Thus, the falling time (T_1) of the level shifter should be well adjusted.

In our design, a constant current source will be inserted between the $4 \times \mathrm{V_{DD}}$ and the source of $\mathrm{M_1}$. The falling time (T_1) of the level shifter is set to 1 μs to ensure the drain-to-source transient voltage of $\mathrm{M_4}$ limited to the nominal supply $\mathrm{V_{DD}}$.

B. High-Voltage-Tolerant Level Shifter

The proposed level shifter is shown in Fig. 10 [34], [35]. All of the transistors are 3.3 V device. Three stacked inverters are used to withstand a higher operation voltage. The capacitor $\mathrm{C_1}$ $(\mathrm{C_2})$ couples the gate of the transistor $\mathrm{M_{N0}}$ $(\mathrm{M_{N4}})$ with the gate of the transistor $\mathrm{M_{P4}}$ $(\mathrm{M_{P8}})$, respectively. If the input control signal (in) switches from low (0 V) to high $(\mathrm{V_{DD}})$, the voltage at the node $\mathrm{n_{L13}}$ couples up with a factor ΔV, which is expressed approximately as

$$\Delta V = \frac{C_1 \cdot V_{DD}}{C_1 + C_{par}} \tag{13}$$

where C_{par} is the parasitic capacitance at the node $\mathrm{n_{L13}}$. On the contrary, the voltage at the node $\mathrm{n_{L6}}$ couples down with a factor $\Delta \mathrm{V}$. By well adjustment, the cross coupled pair $\mathrm{M_{P4}}$ and $\mathrm{M_{P8}}$ can switch faster from one state to the other.

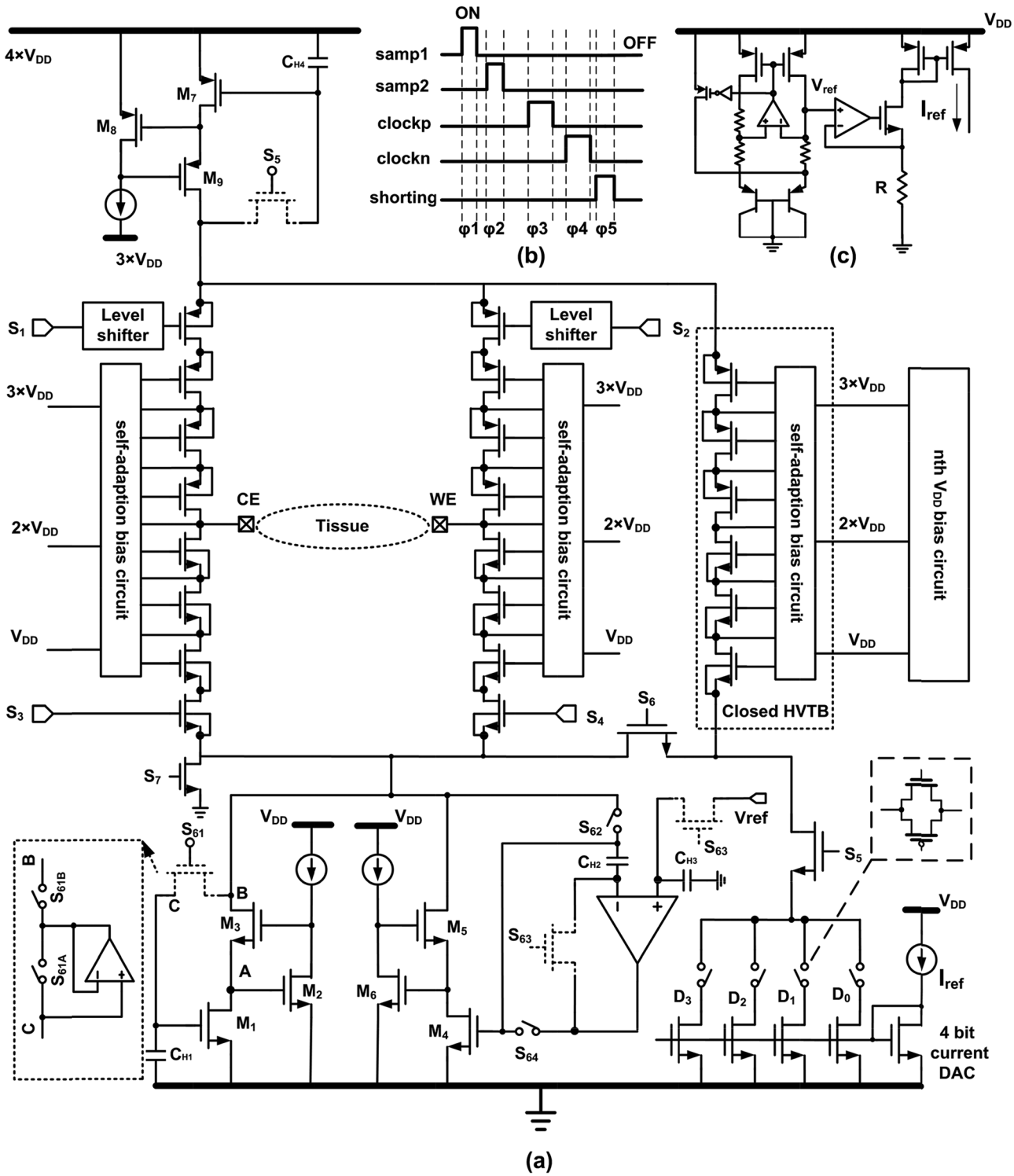

Fig. 11. (a) The fully circuit of neuro-stimulator. (b) Control signal. (c) Current reference circuit.

The high-voltage-tolerant level shifter may have a start-up issue at power-on state, especially with the coupling capacitors. In the worst case, the level shifter may not work properly. For example, when the power supply rises from 0 V to $4 \times \mathrm{V_{DD}}$, the voltage at node $\mathrm{n_{L6}}$ (or $\mathrm{n_{L13}}$) may be pulled up to $4 \times \mathrm{V_{DD}}$. So, the drain current (leakage current) of transistor $\mathrm{M_{P8}}$ (or $\mathrm{M_{P4}}$) is very small. As a result, node $\mathrm{n_{L13}}$ (or $\mathrm{n_{L6}}$) is slowly charged up. If the charged up time is longer than the rising time of $4 \times \mathrm{V_{DD}}$ power supply, the voltages across the terminals of transistors $\mathrm{M_{P8}}$ and $\mathrm{M_{P4}}$ may exceed the nominal supply voltage $\mathrm{V_{DD}}$. The proposed protection circuit is shown in Fig. 10. At power-on state, the voltage of the control signal (start) is set to 0 V. So, transistors $\mathrm{M_{N1}}$, $\mathrm{M_{P11}}$, $\mathrm{M_{P9}}$, and $\mathrm{M_{P10}}$ are turned on, nodes $\mathrm{n_{L13}}$ and $\mathrm{n_{L6}}$ are quickly charged up. At the normal operation state, the voltage of the control signal (start) is $\mathrm{V_{DD}}$, node $\mathrm{n_{L14}}$ is charged up, thus, transistors $\mathrm{M_{P9}}$ and $\mathrm{M_{P10}}$ are turned off.

V. Neuro-Stimulator Full Circuit Implementation

The neuro-stimulator which consists of the IBL, IBLD, HVTB, closed HVTB, and 4-bit current DAC is shown in Fig. 11(a). The voltages at the drains of M_1 and M_4 are set to $\sim V_{THN}$, and let $(W/L)_1 : (W/L)_4 = 10$. Fig. 11(b) shows the timing diagram of the control signals, including the calibration stage ($\varphi 1$ and $\varphi 2$), biphasic stimulation stage ($\varphi 3$ and $\varphi 4$), and the shorting stage ($\varphi 5$). Fig. 11(c) shows the circuit of the current reference, which uses an amplifier in a negative feedback loop to ensure that the voltage across the off-chip resistor R equals to the output voltage (V_{ref}) of the band-gap. Thus, the output current I_{ref} equals to V_{ref}/R. The current reference will be turned off, except during phase $\varphi 1$ for improving power efficiency purpose.

VI. Experimental Results

A stimulator chip has been fabricated in a 0.18-μm 1.8 V/3.3 V CMOS process. The die photo is shown in Fig. 12.

A. Test Bench Configuration

The control signals shown in Fig. 11(b) are generated by the off-chip FPGA (Spartan-3 XC3S400) from Xilinx. While the control signals are given, the stimulator starts to generate biphasic stimulus current. In the operating period, the IBL and IBLD are calibrated in each cycle of biphasic stimulation, and the electrodes are shorted to ground once every 10 cycles of biphasic stimulation for the purpose of precise measurement. The accumulated residual voltages of 10-cycles biphasic stimulation with different stimulus currents are measured by the oscilloscope (Tektronix MSO5104).

B. Voltage Waveforms With Various Stimulus Current

Fig. 13 shows the measured output voltages of the stimulator with the different stimulus currents, where the loading of the stimulator is a 2-kΩ discrete resistor in series with the parallel 100-nF Teflon capacitor and 10-MΩ resistor. The output voltage compliance exceeds 10 V in 12-V power supply. The headroom voltage is $\sim$ 2 V because the IBL and IBLD are realized in the active cascode circuit. Four digital bits were used to set the stimulus current via the 4-bit current DAC. The size of LSB of the 4-bit current DAC is set to 200 μA by an off-chip precise resistor. Thus, 1 bit corresponds to 200-μA stimulus current and 15 bit corresponds to 3000-μA stimulus current.

C. Residual Voltages on Interface Capacitor and Charge Mismatch

Fig. 14 shows an oscilloscope capture of the voltage on 100-nF Teflon capacitor at 3000-μA stimulus current, where the loading of the stimulator is a 1-kΩ discrete resistor in series with the parallel 100-nF Teflon capacitor and 10-MΩ resistor. The accumulated residual voltage at the end of the 10th biphasic stimulation is 118.9 mV. Thus, the residual voltage of

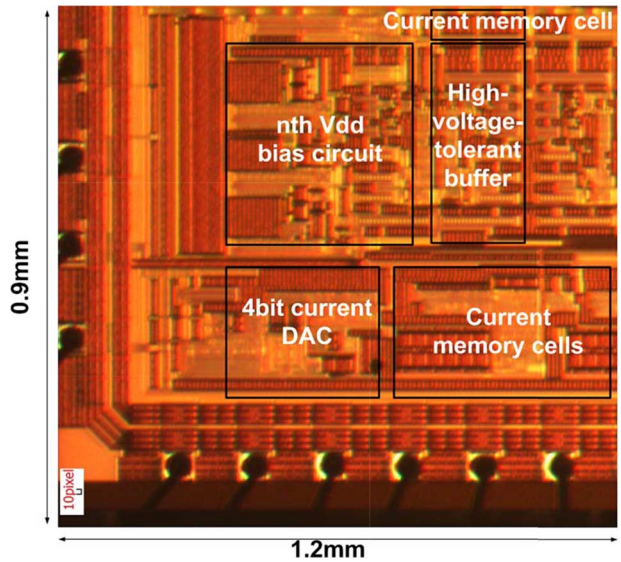

Fig. 12. Die photo of the fabricated stimulator.

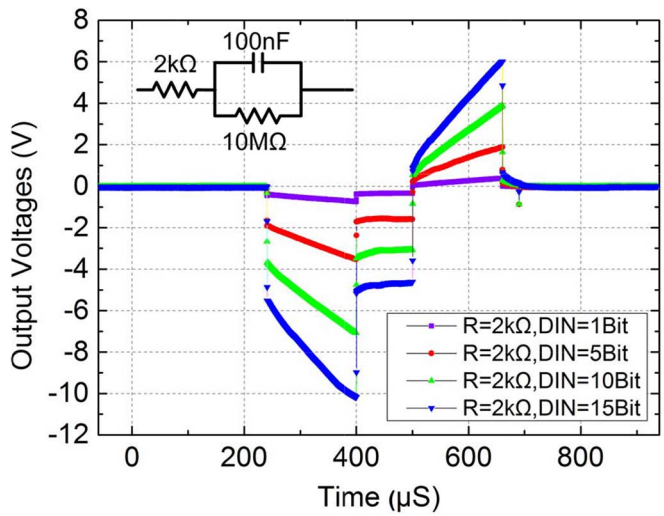

Fig. 13. Output voltages measured with different stimulus currents. The upper inset shows the equivalent circuit with quasi-static loss model.

one-cycle biphasic stimulation is 118.9 mV/10 = 11.89 mV. It means that the injected charge in one-cycle biphasic stimulation is 3000 μA $\times$160 μs = 480 nC, and results in charge error of 11.89 mV $\times$100 nF = 1.19 nC. Thus, the charge mismatch is 1.19 nC/480 nC = 0.25%.

Fig. 15(a) shows the measured residual voltage over the range of DAC current after one-cycle biphasic stimulation. The maximum residual voltage is 11.89 mV caused by one cycle of 3000-μA biphasic stimulation. Fig. 15(b) shows the charge error and charge mismatch as the function of the injected charge. The maximum charge error is 1.19 nC at 480-nC injected charge with 0.25% charge mismatch.

Three fabricated chips have been measured. Fig. 16 shows the probability distribution of the post-stimulation residual voltage under 3000-μA stimulus current. The number of stimulations is 100 for each chip. The mean post-stimulation baseline voltages

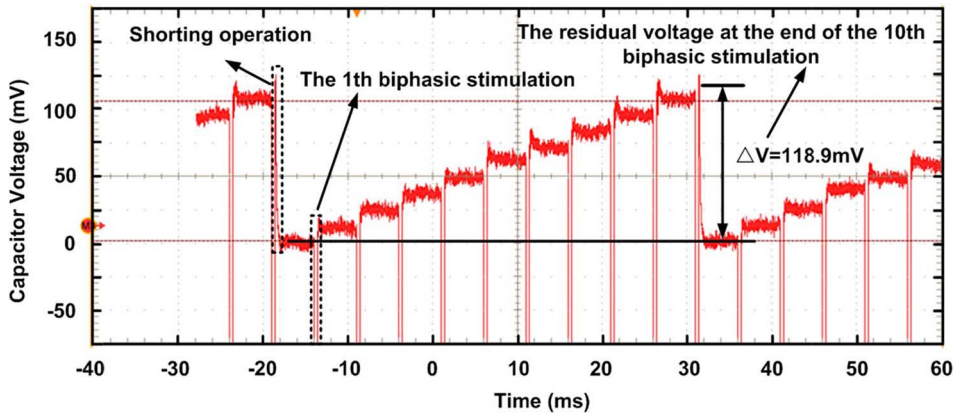

Fig. 14. An oscilloscope capture of the voltage on the 100-nF Teflon capacitor at 3000-μA stimulus current, which allow measurements of the accumulated residual voltage at the end of the 10th biphasic stimulation.

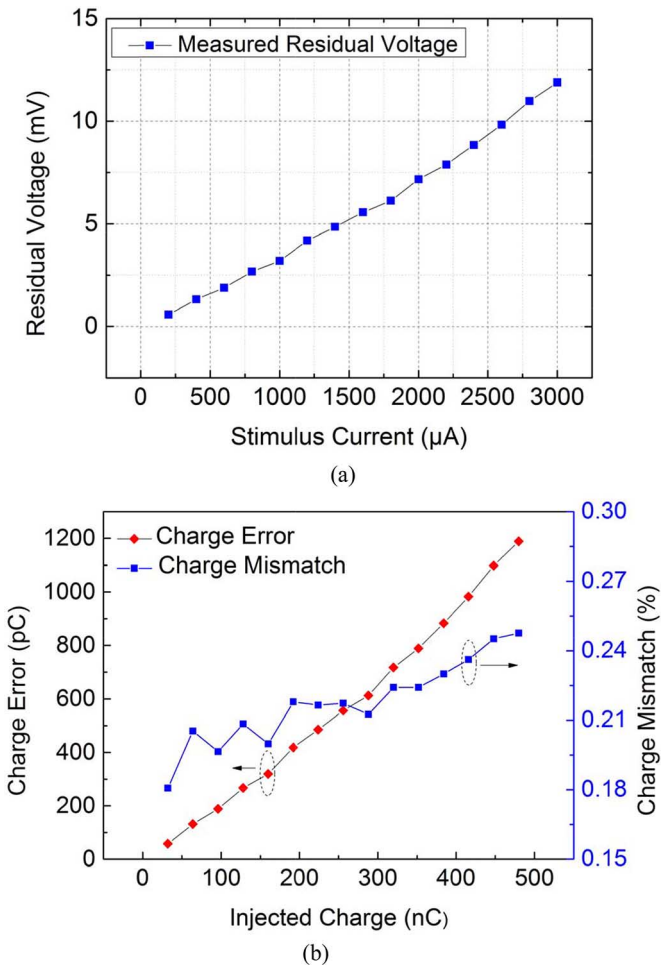

Fig. 15. (a) Residual voltage over the range of DAC current after one-cycle biphasic stimulation. (b) Charge error and charge mismatch factor as the function of injected charge.

are 11.03 mV, 10.83 mV, and 11.44 mV for chip #1, chip #2, and chip #3, respectively.

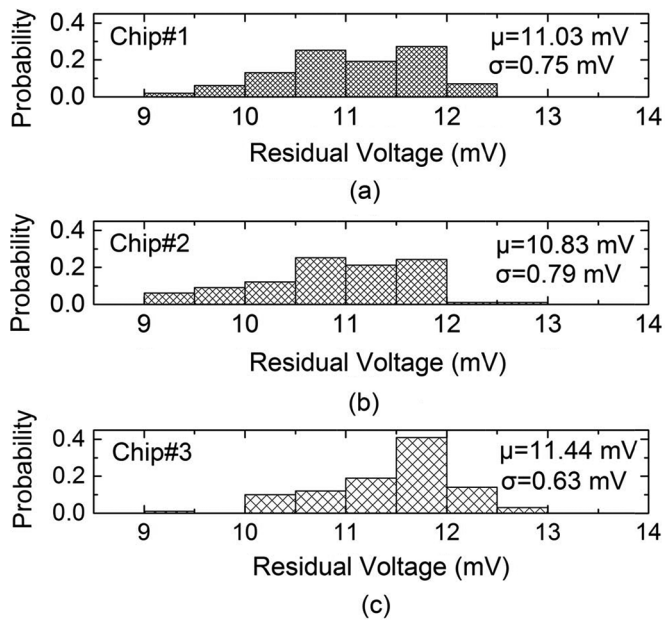

Fig. 16. The probability distribution, mean (μ), and standard deviation (σ) of the post-stimulation residual voltage on the loading capacitor. Three chips have been measured, (a) chip #1, (b) chip #2, and (c) chip #3.

D. Residual Average DC Current Error With Shorting

By following the biphasic stimulation with shorting operation, the residual charge on the interface capacitor is discharged as

$$q(t) = q(0) \cdot e^{-t/RC} \tag{14}$$

where $q(t)$ is the residual charge after t seconds of the shorting operation, $q(0)$ is the residual charge before shorting operation, R is the solution resistance, and C is the interface double capacitor. Equation (14) shows that an additional reduction of the residual charge can be achieved by the available shorting time, solution resistance, and interface double capacitor.

In this work, the maximum charge error is 1.19 nC, the time constant is 1 kΩ $\times$100 nF $=$ 100 μs, and the available shorting

TABLE I
PERFORMANCE COMPARISON WITH PRIOR WORKS

	TBCAS in 2007[15]	JSSC in 2007[20]	TBCAS in 2008[22]	JSSC in 2010[21]	TBCAS in 2013[19]	TBCAS in 2013[13]	TBCAS in 2013[25]	This work
Technology	0.7μm HV	0.35μm HV	0.35μm HV	0.18μm HV	0.18μm HV	0.35μm HV	65nm LV	0.18μm LV
Operation Voltage	-6~9V	0~22.5V	0~10V	±12V	0~12V	0~15V	±2.5V	0~12V
Vout Range	≥11 V	≥20 V	-	±10V	≥11.5V	-	±2.4 V	≥10V
Current Range	0~1000μA	0~1000μA	0~750μA	0~500μA	0~504μA	0~1000μA	0~50μA	0~3000μA
Charge Mismatch	≤0.4%	≤5%	≤0.5%	≤2.9%	≤0.45%	≤0.3%	≤2.24%	≤0.25%
Residual Average DC Current	6nA@1mA	-	-	-	-	1.5nA@1mA	-	6.6nA@3mA 1.7nA@1mA
Power Consumption	≤47μW	≥100μW	≤198.47μW	-	-	≤30μW	-	≤150μW

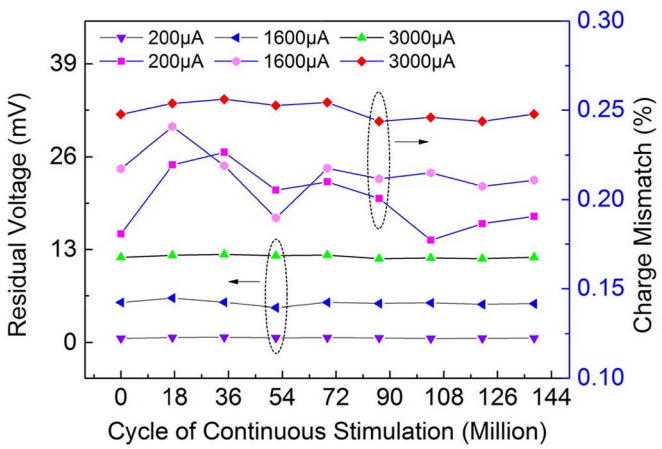

Fig. 17. Reliability measurement results under different stimulus currents as the function of continuous stimulus cycles.

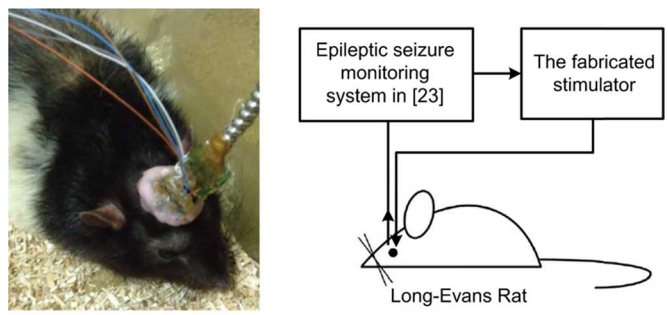

Fig. 18. (a) The Long-Evans Rat with implanted electrodes for detection and stimulation. (b) Measurement setup for animal test [23].

time is 1000 μs -480 μs $=$ 520 μs (assume that the pulse interval is 1000 μs in the high frequency stimulation condition. The time periods of the cathodic stimulation, interphase delay, and anodic stimulation are 160 μs, respectively). So, it can achieve a reduction of the residual charge at least $e^{-5.2} \approx 1/180$. The residual average dc current is the residual charge after shorting operation and divided by the pulse interval, which is calculated as 1.19 nC/180/1 ms $=$ 6.6 nA.

E. Reliability Measurement Results

The reliability measurement of up to 100 million periodic cycles with 3000-μA biphasic stimulation and 5-ms pulse interval in 12-V power supply has been done. The residual voltages on the interface capacitor at 200-μA, 1600-μA, and 3000-μA biphasic stimulation are measured by the oscilloscope once every 24 hours, respectively. Fig. 17 shows the measured residual voltages and charge mismatches as the function of the continuous stimulus cycles. The results show that the charge mismatch is less than 0.25%, and the performance of the neuro-stimulator does not degrade over the continuous stimulus cycles of more than 138.2 million.

F. Performance Comparison With Prior Works

Table I summarizes the performances of this neuro-stimulator relative to the prior works. The charge mismatch in this work is less than 0.25% which is better than that of the prior works. The residual average dc current in this work meets the specified industry limit in cochlear implants. In addition, thanks to using the transistors with the deep n-well layer, the operation voltage of the proposed neuro-stimulator can be up to 12 V which is higher than that of the prior high-voltage-tolerant buffers developed in the LV CMOS process [28]–[32].

G. Animal Test

Animal trials have been performed, and all the experimental procedures have been reviewed and approved by the Institutional Animal Care and Use Committee of National Cheng-Kung University, Taiwan. Fig. 18(a) shows the Long-Evans Rat with implanted electrodes for detection and stimulation, and Fig. 18(b) shows the measurement setup for animal test [23]. Because the solution spreading resistance (R_{SW}) of the Long-Evans rat is larger than that of the human, the size of LSB of the 4-bit current DAC is adjusted to 7 μA by the off-chip precise resistor. Whenever the system detects an epileptic seizure, the stimulator is activated. The stimulus current of the pulse train with $\pm$28-μA amplitude, 0.5-ms pulse width, 2.5-ms period, and 500-ms duration is used to suppress the epileptic seizure of

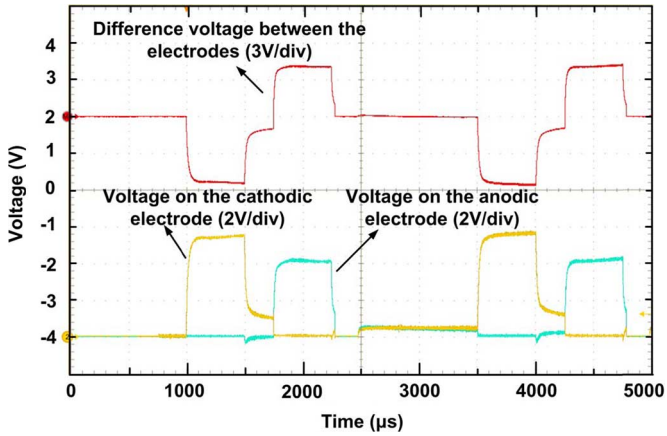

Fig. 19. The voltages on the electrodes in animal test with 28-μA stimulus current.

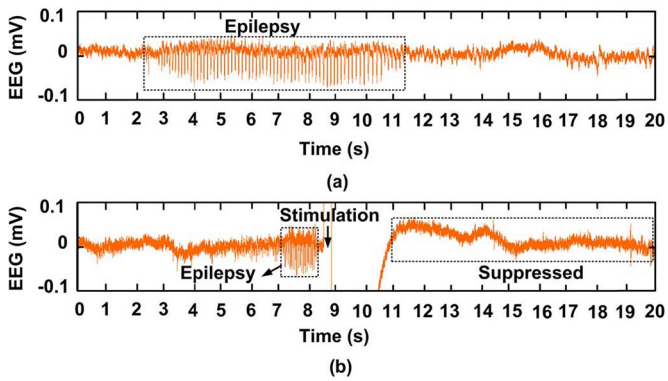

Fig. 20. Experimental results on EEG signals of Long-Evans rat (a) without stimulation, and (b) with stimulation.

the Long-Evans rat. Fig. 19 shows an oscilloscope capture of the voltages on the electrodes. Fig. 20(a) and (b) show the electroencephalography (EEG) signals of the long-Evans rat without and with applying the stimulation, respectively. In Fig. 20(a), the epileptic discharges are observed during 3–11.5 s. In Fig. 20(b), the intensive and rapidly brain activities are suppressed by the stimulation.

According the experiment results, the functionalities of the proposed stimulator have been successfully verified.

VII. Conclusion

A charge-balanced and high-voltage-tolerant neuro- stimulator has been designed and successfully verified in a 0.18-μm 1.8 V/3.3 V CMOS process. The current memory cell with dual calibration loops and leakage current compensation is proposed to ensure the charge mismatch less than 0.25% and the residual average dc current less than 6.6 nA with shorting operation.

References

[1] C.-Y. Lin, W.-L. Chen, and M.-D. Ker, "Implantable stimulator for epileptic seizure suppression with loading impedance adaptability," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 2, pp. 196–203, Apr. 2013.

[2] W.-M. Chen *et al.*, "A fully integrated 8-channel closed-loop neural-prosthetic CMOS SoC for real-time epileptic seizure control," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 232–247, Jan. 2014.

[3] D. R. Merrill, M. Bikson, and J. G. Jefferys, "Electrical stimulation of excitable tissue: Design of efficacious and safe protocols," *J. Neurosci. Methods*, vol. 141, no. 2, pp. 171–198, Feb. 2005.

[4] J. M. Aran *et al.*, "Electrical stimulation of the ear: Experimental studies," *Ann. Otol. Rhinol. Laryngol.*, vol. 92, no. 6, pp. 614–620, Nov. 1983.

[5] R. J. Hurlbert, C. H. Tator, and E. Theriault, "Dose-response study of the pathological effects of chronically applied direct current stimulation on the normal rat spinal cord," *J. Neurosurg.*, vol. 79, no. 6, pp. 905–916, Dec. 1993.

[6] R. K. Shepherd, N. Linahan, J. Xu, G. M. Clark, and S. Araki, "Chronic electrical stimulation of the auditory nerve using non-charge-balanced stimuli," *Acta Otolaryngologica*, vol. 119, no. 6, pp. 674–684, Dec. 1999.

[7] J. Xu, R. K. Shepherd, R. Millard, and G. M. Clark, "Chronic electrical stimulation of the auditory nerve at high stimulus rates: A physiological and histopathological study," *Hear Res.*, vol. 105, no. 1, pp. 1–29, Mar. 1997.

[8] C. Q. Huang, R. K. Shepherd, P. M. Carter, P. M. Seligman, and B. Tabor, "Electrical stimulation of the auditory nerve: Direct current measurement in vivo," *IEEE Trans. Biomed. Eng.*, vol. 46, no. 4, pp. 461–470, Apr. 1999.

[9] R. Shulyzki, K. Abdelhalim, A. Bagheri, M. T. Salam, C. M. Florez, J. L. P. Velazquez, P. L. Carlen, and R. Genov, "320-Channel active probe for high-resolution neuromonitoring and responsive neurostimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 1, pp. 34–49, Feb. 2015.

[10] X. Liu, A. Demosthenous, and N. Donaldson, "An integrated implantable stimulator that is fail-safe without off-chip blocking-capacitors," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 3, pp. 231–244, Sep. 2008.

[11] N. Dommel, G. Suaning, P. Preston, T. Lehmann, and N. Lovell, "In-vitro testing of simultaneous charge injection and recovery in a retinal neuroprosthesis," in *Proc. 27th Annu. Int. Conf. Engineering in Medicine and Biology Soc.*, Sep. 2005, pp. 7612–7615.

[12] M. Ghovanloo, K. Otto, D. Kipke, and K. Najafi, "In vitro and in vivo testing of a wireless multichannel stimulating telemetry micro system," in *Proc. 26th Annu. Int. Conf. IEEE Engineering in Medicine and Biology Soc.*, Sep. 2004, pp. 4294–4297.

[13] H. Chun, Y. Yang, and T. Lehmann, "Safety ensuring retinal prosthesis with precise charge balance and low power consumption," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 1, pp. 108–118, May 2013.

[14] J. H. Baek, M. Lee, J. H. Lee, H. S. Pae, C. J. Lee, J. T. Kim, C. S. Choi, H. K. Kim, T. J. Kim, and H. K. Chung, "A current-mode display driver IC using sample-and-hold scheme for QVGA full-color AMOLED displays," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2974–2982, Dec. 2006.

[15] J.-J. Sit and R. Sarpeshkar, "A low-power blocking-capacitor-free charge balanced electrode-stimulator chip with less than 6 nA DC error for 1-mA full-scale stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 3, pp. 172–183, Sep. 2007.

[16] E. Lee, "High-voltage tolerant stimulation monitoring circuit in conventional CMOS process," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2009, pp. 93–96.

[17] C.-Y. Lin and M.-D. Ker, "Overview of on-chip stimulator designs for biomedical applications," *J. Neurosci. Neuroeng.*, vol. 1, no. 2, pp. 204–212, Dec. 2012.

[18] X. Liu, A. Demosthenous, and N. Donaldson, "An integrated stimulator with DC-isolation and fine current control for implanted nerve tripoles," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1701–1714, Jul. 2011.

[19] I. Williams and T. Constandinou, "An energy-efficient, dynamic voltage scaling neural stimulator for a proprioceptive prosthesis," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 2, pp. 129–139, Apr. 2013.

[20] M. Ortmanns, A. Rocke, M. Gehrke, and H. J. Tiedtke, "A232-channel epiretinal stimulator ASIC," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2946–2959, Dec. 2007.

[21] K. Chen, Z. Yang, L. Hoang, J. Weiland, M. Humayun, and W. Liu, "An integrated 256-channel epiretinal prosthesis," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1946–1956, Sep. 2010.

[22] T. G. Constandinou, J. Georgiou, and C. Toumazou, "A partial-current-steering biphasic stimulation driver for vestibular prostheses," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 2, pp. 106–113, Jun. 2008.

[23] M.-D. Ker *et al.*, "Stimulus driver for epilepsy seizure suppression with adaptive loading impedance," *J. Neural Eng.*, vol. 8, no. 6, Dec. 2011.

[24] P. Swaroop, A. J. Vasani, and M. Ghovanloo, "A high-voltage output driver for implantable biomedical stimulators and I/O applications," in *Proc. 49th IEEE Int. Midwest Symp. Circuits and Systems*, Aug. 2006, pp. 566–569.
[25] M. Monge *et al.*, "A fully intraocular high-density self-calibrating epiretinal prosthesis," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 6, pp. 747–760, Dec. 2013.
[26] I. O. Conner and A. Kaiser, "Automated synthesis of current-memory cells," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 19, no. 4, pp. 413–424, Apr. 2000.
[27] B. Razavi, *Design of Integrated Circuits for Optical Communications*. New York, NY, USA: McGraw-Hill, 2002.
[28] P. Shah, "A short term analogue memory," in *Proc. 18th Eur. Solid-State Circuits Conf.*, Sep. 1992, pp. 21–23.
[29] B. Serneels, T. Piessens, M. Stepert, and W. Dehaene, "A high-voltage output driver in a standard 2.5 V 0.25 μm CMOS technology," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2004, pp. 146–148.
[30] B. Serneels, M. Steyaert, and W. Dehaene, "A 237 mW aDSL2+CO line driver in standard 1.2 V 0.13 μm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2007, pp. 524–526.
[31] B. Serneels, E. Geukens, B. De Muer, and T. Piessens, "A 1.5 W 10 V-output class-D amplifier using a boosted supply from a single 3.3 V input in standard 1.8 V/3.3 V 0.18 μm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2012, pp. 94–96.
[32] A. J. Annema, G. Geelen, and P. de Jong, "5.5 V I/O in a 0.25 μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 528–538, Mar. 2011.
[33] Y. Ismail *et al.*, "A 34 V charge pump in 65 nm bulk CMOS technology," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 408–410.
[34] B. Serneels, M. Steyaert, and W. Dehaene, "A high speed, low voltage to high voltage level shifter in standard 1.2 V 0.13 μm CMOS," in *Proc. IEEE Int. Conf. Electronics, Circuits, and Systems*, Mar. 2006, pp. 668–671.
[35] D. Pan, H. W. Li, and B. M. Wilamowski, "A low voltage to high voltage level shifter circuit for MEMS application," in *Proc. 15th Biennial University/Government/Industry Microelectronics Symp.*, Jul. 2003, pp. 128–131.

Zhicong Luo (S'15) received the B.S. and M.E. degrees in electrical engineering from College of Physic and Information Engineering, Fuzhou University, Fuzhou, China, in 2006 and 2009, respectively.

Currently, he is working toward the Ph.D. degree in analog circuit design for biomedical applications at the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan. Since 2010, he has been a Lecturer at the College of Mechanical and Electronic Engineering, Fujian Agriculture and Forestry University, Fuzhou, China.

Ming-Dou Ker (F'08) received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University (NCTU), Hsinchu, Taiwan, in 1993.

He has worked as the Department Manager with the VLSI Design Division, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. Since 2004, he has been a Full Professor in the Department of Electronics Engineering at NCTU. From 2008–2011, he was rotated to be Chair Professor and Vice President of I-Shou University, Kaohsiung, Taiwan. Now, he has been the Distinguished Professor in the Department of Electronics Engineering, National Chiao-Tung University. He has served as the Executive Director of National Science and Technology Program on System-on-Chip (NSoC) in Taiwan during 2010–2011; and the Executive Director of National Science and Technology Program on Nano Technology (NPNT) in Taiwan (2011–2015). From 2012–2015, he was the Dean of the College of Photonics at NCTU. Currently, he is serving as the Director of the Biomedical Electronics Translational Research Center (BETRC), NCTU, working on biomedical electronics translational projects. In the technical field of reliability and quality design for microelectronic circuits and systems, he has authored more than 500 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability and quality of integrated circuits, which have been granted with hundreds of U.S. patents and Taiwan patents. He has been invited to teach and/or to consult the reliability and quality design by hundreds of design houses and semiconductor companies in the worldwide IC industry. His research interests include the circuits and systems for biomedical applications, as well as circuit-related reliability issue.

Dr. Ker has served as a member of the Technical Program Committee and the Session Chair of numerous international conferences for many years. He ever served as the Associate Editor for the IEEE TRANSACTIONS ON VLSI SYSTEMS (2006–2007). He was selected as the Distinguished Lecturer in the IEEE Circuits and Systems Society (2006–2007) and in the IEEE Electron Devices Society (2008–2015). He was the Founding President of Taiwan ESD Association. Currently, he is the editor of IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY.