Low-Leakage Bidirectional SCR With Symmetrical Trigger Circuit for ESD Protection in 40-nm CMOS Process

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***Abstract*—This paper presents a novel bidirectional electrostatic discharge protection device based on a dual silicon-controlled rectifier with a symmetrical trigger circuit. The proposed device has been realized and verified in a 40-nm CMOS process, which can pass a 3.75-kV HBM and a 250-V MM with a very low standby leakage current of $\sim$27 nA at 25 °C and a bias voltage of 0.9 V with a silicon footprint of only 13 μm $\times$ 100 μm.**

***Index Terms*—Electrostatic Discharge (ESD) Protection, silicon-controlled rectifier (SCR), bidirectional SCR, mixed voltage.**

I. Introduction

ELECTROSTATIC discharge (ESD) is still a challenging topic in IC design, which is one of the major reliability concerns in IC industry [1]. ESD are the result of charge balance within two bodies that reach contact. The charge difference between the bodies causes a current to flow to equalize the charge levels. Such currents are in the order of several amperes, which are discharged in few nanoseconds. Such discharges may harm the internal devices of an IC. Therefore, ICs have special ESD protection devices to allow safe discharge paths to ESD currents, and to protect the internal circuits from ESD damage. ESD protection becomes ever more challenging in nanoscale CMOS processes. With the continuous miniaturization of CMOS transistors, the scaled-down gate oxide thickness becomes a critical feature for ESD protection. With thinner gate oxide, the breakdown voltage is also reduced, and the gate becomes extremely sensitive to ESD stress. Moreover, in advanced nanoscale CMOS processes, the gate oxide thickness has been reduced to a few nanometers, which increases the gate oxide tunneling effect to cause severe leakage issues [2]–[4].

The whole-chip ESD protection network must ensure that every pin-to-pin combination is protected from ESD damage. The whole-chip ESD protection scheme proposed in [5] had been widely used, although it only showed with single power domain. Typical ICs in nanoscale CMOS technologies use differentiated power domains for different purposes, such as different operation voltages, noise immunity, and smart power control. Having multiple power domains adds further complexity to the ESD protection network. Some solutions have been proposed for multiple power domain ESD protection [6], [7], which required bidirectional ESD conduction devices. Typical devices used as ESD protection, such as diodes, MOSFET, and silicon-controlled-rectifiers (SCR), have fixed polarity since they have parasitic diodes embedded in their structures. A simple solution to achieve a bidirectional ESD protection element was to connect two diodes (or diode strings) in antiparallel connection, i.e., the cathode of the first diode (string) with the anode of the second diode (string) and the anode of the first diode (string) with the cathode of the second diode (string), although this configuration may lead to large area utilization and large leakage current in the diode strings [8]. On the other hand, the dual-SCR (DSCR), also called bi-directional-SCR, can achieve bidirectional ESD protection with smaller area and lower leakage current. Some previous works have reported the use of dual SCR for bidirectional ESD protection [9]–[12]. In [9] diode strings were used to trigger the dual SCR but there would still be large leakage current in the diodes. Similarly, the previous work in [10] proposed the use of a depletion pMOS transistor as trigger device, but this would have serious leakage issue due to gate leakage, and moreover, this device required an external control voltage to turn the device off. In [11], the cross-coupled nMOS transistors were used to achieve low trigger voltage, which is good for ground to ground ESD protection but not acceptable for core voltage operations. Finally, the prior work in [12] proposed the use of a dummy gate to block the STI formation to reduce the self-trigger voltage of the DSCR structure, but this structure would also be affected by the gate leakage issue. It is clear from previous works that a bidirectional DSCR with consideration of gate leakage is needed.

In this work, a novel bi-directional SCR with consideration of the gate leakage is proposed and successfully verified in a 40-nm CMOS process.

II. Proposed DSCR Device

A. Device Structure

The proposed bi-directional ESD protection device is based on a dual SCR, and designed with focus on turn-on speed, since SCR structures are known to suffer from slow turn-on speed [13]. The device cross-sectional view and equivalent circuit are shown in Fig. 1. The DSCR is formed with two n-wells

Manuscript received June 4, 2016; revised August 1, 2016; accepted August 12, 2016. Date of publication August 15, 2016; date of current version December 1, 2016. This work was supported in part by the Ministry of Science and Technology, Taiwan, under contracts MOST 103-2221-E-009-197-MY2, MOST 105-2622-8-009-001-TE1, and MOST 105-2221-E-009-166.

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Digital Object Identifier 10.1109/TDMR.2016.2600276

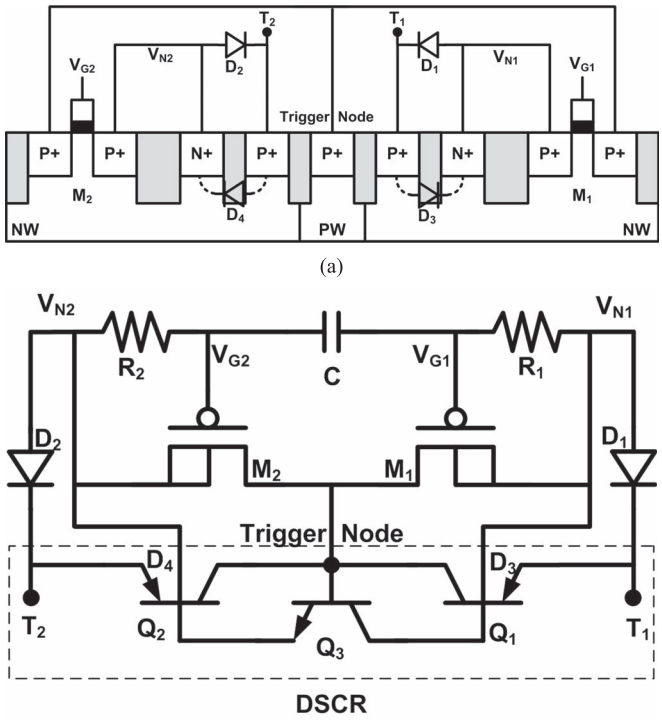

Fig. 1. Proposed DSCR structure with a symmetrical trigger circuit. (a) and (b) Device cross-sectional view and equivalent circuit, including the RCR trigger circuit, respectively.

and a middle p-well, so the embedded trigger transistors, M_1 and M_2, are pMOS transistors, which have lower leakage current than their nMOS counterpart. The pMOS transistors are designed with the floating n-wells to decrease the turn-on time of the DSCR [14], [15]. The diodes D_1 and D_2 are designed in external n-wells which are required to complete the trigger current paths because the n-wells are not connected to the DSCR terminals. The resistors and capacitor are used to detect the fast transient characteristic of ESD waveforms, and to trigger on the pMOS transistors. The intrinsic diodes D_3 and D_4 are the emitter-base diodes of the parasitic bipolars between the terminal contact p+ region, the n-well, and the p-well, which play an important role in the trigger process.

B. Operation Under ESD Condition

When an ESD-like waveform zaps the device (suppose a positive voltage from T_1 to T_2) with voltage V_{ESD}, a current will flow through D_3, R_1, C, R_2, and D_2 to charge the capacitor C. This current is given by

$$I_C = \frac{V_{\mathrm{ESD}} - 2V_D}{2R} e^{\frac{-t}{2RC}} \tag{1}$$

where V_D is the voltage drop across the diodes D_3 and D_2. This current will bias the n-well of M_1 to $V_{\mathrm{ESD}} - V_D$ and the well of M_2 to V_D. Also, since the capacitor is initially discharged, V_{G1} and V_{G2} are biased to $V_{\mathrm{ESD}}/2$. V_{G1} then rises exponentially to $V_{\mathrm{ESD}} - V_D$ with time constant 2RC. The voltage drop across R_1 is given by

$$V_{R1} = \frac{V_{\mathrm{ESD}} - 2V_D}{2} e^{\frac{-t}{2RC}}. \tag{2}$$

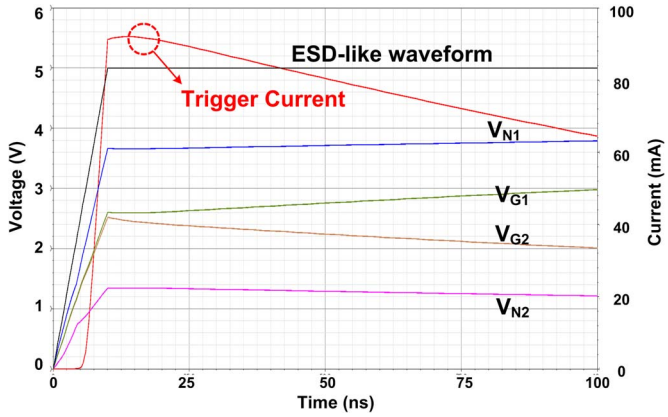

Fig. 2. Simulation result for an ESD-like waveform zapping from T_1 to T_2.

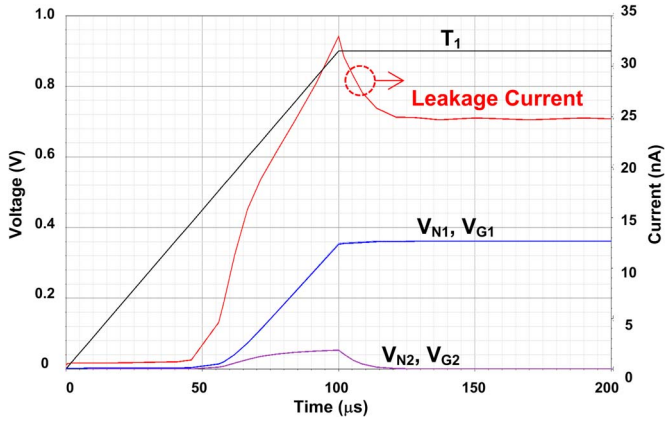

Fig. 3. Simulation result for normal circuit operation.

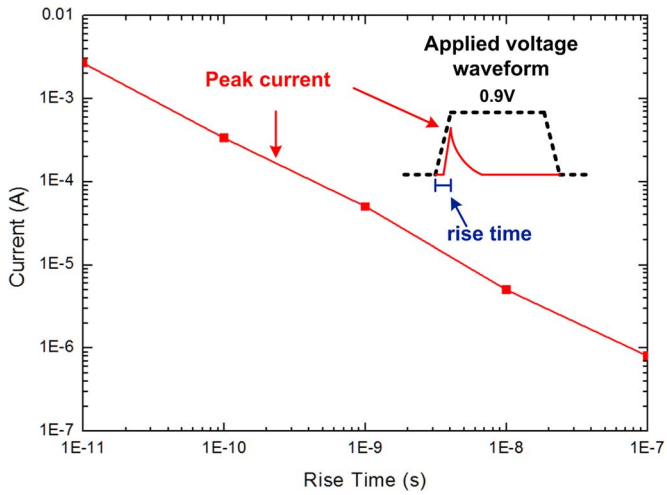

Fig. 4. Simulated peak current for a 0.9-V square pulse with different rise times.

This voltage drop turns M_1 on to trigger the DSCR. M_2 remains turned-off since its V_{GS} voltage is positive. The trigger current flows first through D_3, causing the bipolar Q_1 to turn on, and then through M_1 into the trigger node, which causes both Q_2 and Q_3 to turn on. Finally, the ESD current at the terminal T_1 will be discharged from the SCR (formed by Q_1 and Q_3) and the diode D_2 to the terminal T_2.

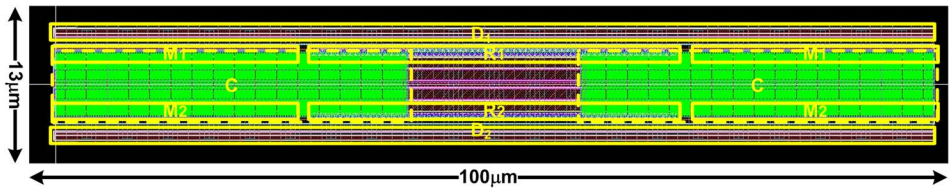

Fig. 5. Layout view of the proposed DSCR with a symmetrical trigger circuit. The total area is 13 μm $\times$ 100 μm.

A simulation result for an ESD-like waveform is shown in Fig. 2. A 5 V stress with 1 ns rise time is applied to T_1. The DSCR is simplified for simulation purpose. Transistors M_1 and M_2 size is W/L $=$ 120 μm/80 nm, and the RCR time constant is 160 ns. The trigger current is the current entering the trigger node in the DSCR structure. Results show the transistor M_1 can successfully provide the trigger current of $\sim$90 mA into the DSCR structure.

C. Normal Circuit Operation

To understand the circuit behavior during normal circuit operation, suppose the voltage at T_1 rises slowly to the operating voltage while T_2 is grounded. The trigger node is also grounded since it is connected to the substrate. During the rising period, a current flows through the capacitor and charges V_{G1} to $\sim V_{T1} - V_D$. Since the current is very small, V_{N1} is almost equal to V_{G1}, thus M_1 is kept off. After the transient, T_1 reaches the DC operating voltage, V_{G1} and V_{N1} are kept at the same voltage, thus M_1 remains off. The leakage current in the circuit is mainly due to M_1 and flows from T_1 to the substrate. A simulation result is shown in Fig. 3. The overall leakage current for a 0.9 V bias is $\sim$25 nA. If both T_1 and T_2 terminals were biased at the same voltage, then the leakage current would be doubled.

In Fig. 3, the rise time used for the simulation was chosen to be the typical rise time during power-on condition. The proposed DSCR could also be used in application which may require faster rise times. The RCR trigger circuit (R_1, C, and R_2) would not have excessive peak currents during fast rise times since the capacitor current also flows through two diodes (D_3 and D_2 for a signal from T_1 to T_2). The simulation of Fig. 3 was repeated with different rise times and the peak current was annotated. The Simulated peak currents for a 0.9 V square pulse with different rise times on the proposed DSCR are summarized in Fig. 4.

D. Silicon Implementation

The proposed structure was implemented in a general-purpose 40-nm CMOS process. Fig. 5 shows the layout of the proposed DSCR with symmetrical trigger circuit. The transistors (M_1 and M_2) are designed with dimension of W/L $=$ 120 μm/80 nm and separated into two parts to comply with DRC rules. The resistors are realized with polysilicon in the space between the transistors. The capacitor is MOM capacitor and placed on top of the DSCR, realized metal layers 5 to 7 (metal layers 1 and 2 are used for internal connections and metal layers 3 and 4 are used for pad connection). The resulting

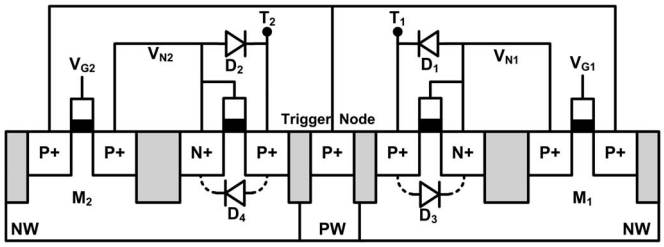

Fig. 6. Proposed DSCR structure with polybounded diodes D_3 and D_4.

TABLE I
LIST OF SPLIT CONDITIONS

Split Name	D_1/D_2 diode	D_3/D_4 diode
STI	POLY	STI
POLY	POLY	POLY

RCR time constant is $\sim$160 ns. The diodes D_1 and D_2 are placed in individual n-wells besides the DSCR. Total cell area is 13 μm $\times$ 100 μm. The diodes D_1 and D_2 are implemented as poly-bounded structures. In addition, the implicit diodes D_3 and D_4 can also be implemented as poly-bounded structures to increase the turn-on speed, as it was suggested in [16]. In order to do so, the STI formation between the p+ terminal contact and n+ n-well contact is blocked by adding a dummy gate, as shown in Fig. 6. Table I show the list of split conditions and naming convention that is used in the following sections.

III. Measurement Results

A. Leakage Current

Leakage current measurements are performed on die with ultra-low-leakage probes and under controlled temperature. Results shown in Fig. 7 correspond to positive voltages applied to T_1 with T_2 grounded.

The fabricated devices measure the leakage current of 29 nA and 37 nA at 0.9 V bias and 25 °C for the STI and POLY designs, and 7.2 μA and 9.8 μA at 0.9 V bias and 125 °C for the STI and POLY designs, respectively. The difference between the simulated and measured leakage currents is attributed to the gate leakage caused in the dummy gates on the poly-bounded diodes.

B. TLP

Transmission line pulsing (TLP) is an important characterization tool for ESD protection circuits [17], [18]. A TLP tester

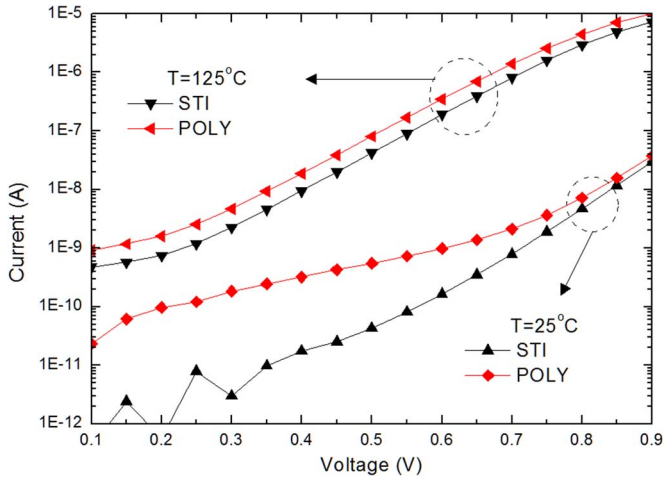

Fig. 7. Leakage current measurement for different bias voltages under controlled temperature.

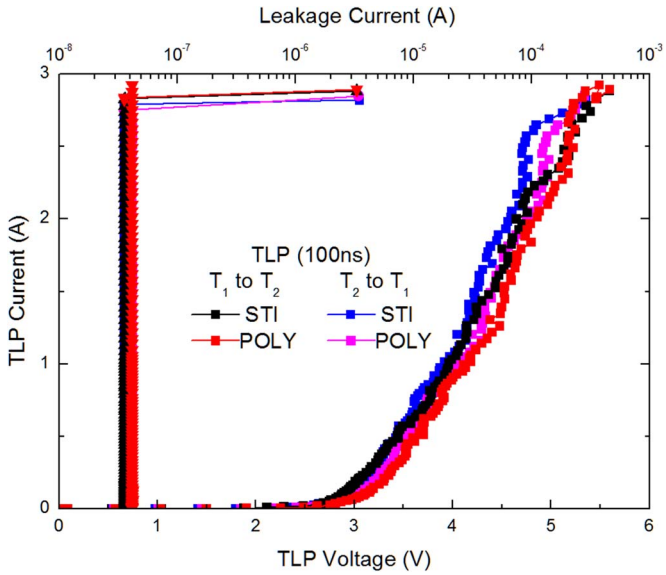

Fig. 8. TLP I–V measurement results for the implemented devices.

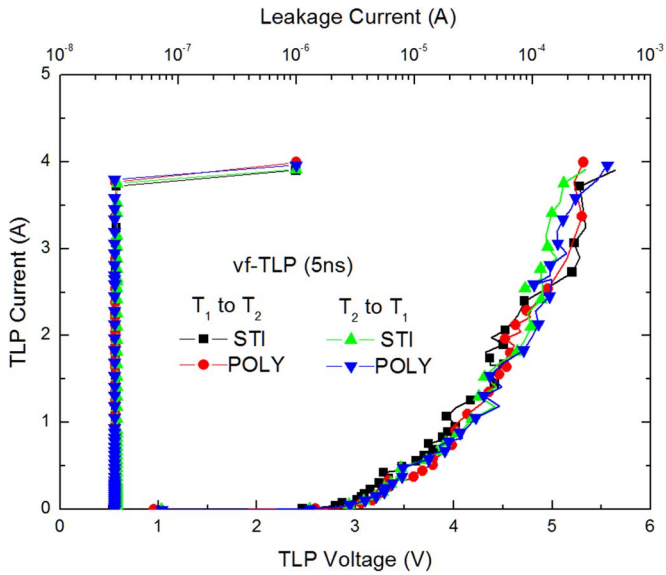

Fig. 9. vf-TLP I–V measurement results for the implemented devices.

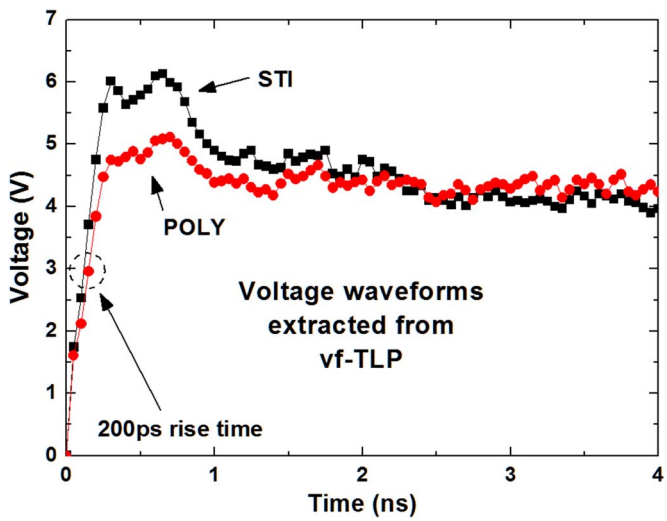

Fig. 10. Extracted voltage waveforms from vf-TLP measurements.

was used to measure the TLP IV curves of the proposed devices. TLP measurement results are shown in Fig. 8. All devices have holding voltage of ∼3 V, and there is no snapback observed. This is attributed to an excessive trigger current, which means the trigger pMOS transistors width could be further reduced with no significant impact on the TLP results, and further reducing the leakage current. I_{t2} is ∼2.7 A for all devices.

In addition, very-fast TLP (vf-TLP) was also performed with 200 ps rise time and 5ns pulse width. The measured IV curves are shown in Fig. 9. The vf-TLP test shows that the proposed designs can turn-on in short time. Fig. 10 shows the extracted voltage waveforms from the vf-TLP measurements for the verified devices. The STI design shows a slightly larger overshoot voltage.

C. ESD Robustness

In order to test the ESD robustness of the proposed ESD protection circuits, a set of demo circuits were designed. The demo internal circuits to be protected consist of an inverter chain made with thin-oxide transistors with dimension W/L = 90 μm/120 nm. The first demo case is built with the standard ESD protection approach, as shown in Fig. 11(a), using the power-rail ESD clamp circuit provided by the foundry. The input resistor is 300Ω the ESD diodes (D_{P1}, D_{N1},D_{P2}, and D_{N2}) are 90 μm × 20 μm, and the ESD clamp transistor (M_{ESD}) dimension is W/L = 2324 μm/130 nm. The area of the power-rail ESD clamp circuit is 100 μm × 60 μm, and has a leakage current of 2.64 μA at 0.9 V bias and 25 °C.

The demo case with the ESD protection design proposed in this work is shown in Fig. 11(b). The diodes and power-rail ESD clamp circuit were replaced by the DSCR devices. Since the DSCR is bidirectional, only one device is required per each pad, although the input pad has an additional DSCR (DSCR D) connected to VDD to guarantee good ESD protection to the input pMOS gate for input-to-VDD stresses, since otherwise

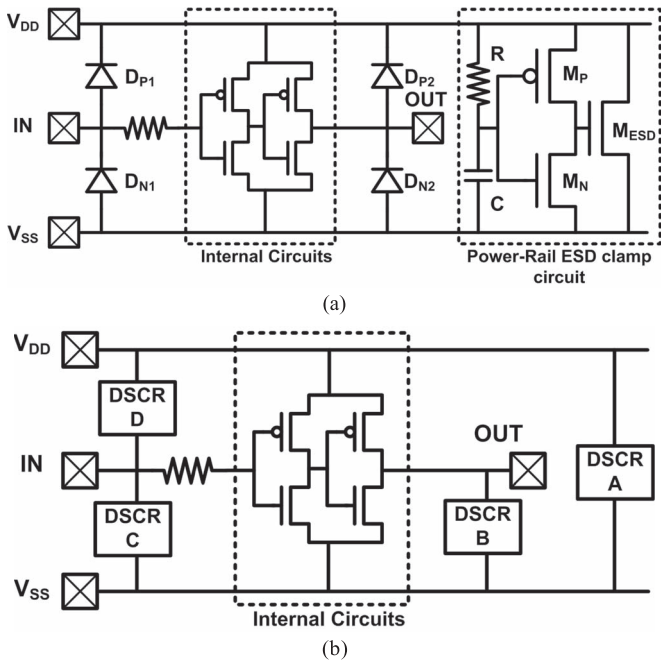

Fig. 11. Circuits used for ESD robustness measurement. (a) Circuit using the standard whole-chip ESD protection. (b) Circuit using the proposed DSCR-based whole-chip ESD protection.

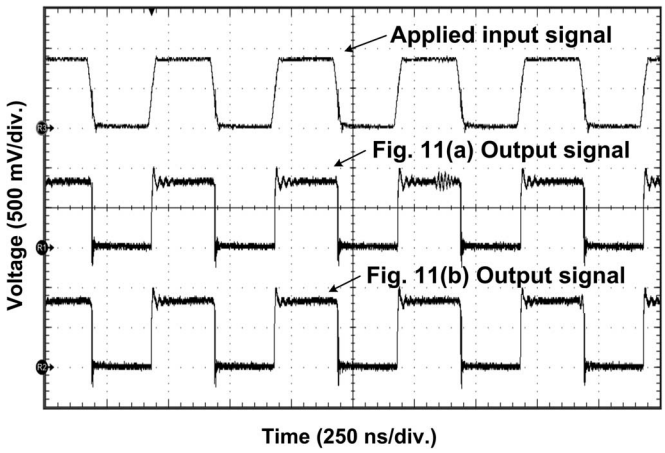

Fig. 12. Observed output waveforms of the circuits in Fig. 11 for an applied 0.9-V 2-MHz square pulse at the input pad.

the ESD current would flow though DSCR A and DSCR C, thus having a large holding voltage. For some real applications, this extra DSCR may not be needed. Such whole-chip ESD protection design has the advantage of using the same device for every pad, simplifying the design process. This demo case was built with all proposed DSCR devices (STI and POLY).

In order to verify the DSCR does not add excessive load to the input inverter, the circuit is tested by applying a signal at the input pad and measuring the output waveform. An Agilent 8110 A pulse generator is used to feed a 2 MHz signal to the demo circuits. Results are shown in Fig. 12, comparing the outputs of the circuit of Fig. 11(a) with one of the circuits of Fig. 11(b) (the two implemented circuits have similar results, so only one is shown). Results shown no signal degradation,

TABLE II
HBM MEASUREMENT RESULTS AND FAILURE LOCATION

Circuits	Positive to V_{SS}	Positive to V_{DD}	Negative to V_{SS}	Negative to V_{DD}
Fig. 11(a)	3.25kV	4.5kV	4.5kV	3.25kV
	circuit	D_{P1}	D_{N1}	circuit
Fig. 11(b) STI	3.75kV	4.25kV	3.75kV	4.25kV
	circuit	DSCR D	circuit	DSCR C
Fig. 11(b) POLY	3.75kV	4.25kV	3.75kV	4.25kV
	circuit	DSCR D	circuit	DSCR D

TABLE III
MM MEASUREMENT RESULTS AND FAILURE LOCATION

Circuits	Positive to V_{SS}	Positive to V_{DD}	Negative to V_{SS}	Negative to V_{DD}
Fig. 11(a)	250V	350V	350V	250V
	circuit	D_{P1}	D_{N1}	circuit
Fig. 11(b) STI	250V	275V	250V	275V
	circuit	circuit	circuit	circuit
Fig. 11(b) POLY	350V	350V	350V	350V
	DSCR C	DSCR D	DSCR C	DSCR D

thus the proposed DSCR can be safely used to protect IO pins. Although, for higher frequency operations some special ESD protection devices may be needed [19], [20].

The demo circuits were tested with the HBM [21] and MM [22] models using a ESD tester, including positive-to-V_{SS} (PS), negative-to-V_{SS} (NS), positive-to-V_{DD} (PD), and negative-to-V_{DD} (ND) combinations. After ESD stress, the failure locations were observed with Scanning Electron Microscopy (SEM). Results for stresses at the input pads are shown in Tables II and III for HBM and MM results, respectively. The tables also list the failure location for each measurement. The HBM results for the proposed designs are the same for both STI and POLY designs, although the POLY design shows an improvement in the MM levels. Moreover, the failure location changes from the internal circuits to the DSCR. This is attributed to the lower overshoot voltage (as observed in Fig. 10). Fig. 13 shows the SEM images with the failures after PS mode MM stress for the STI and POLY designs. The higher MM level of the POLY design is attributed to the lower overshoot voltage (as seen in Fig. 10).

The demo circuits were also tested with the vf-TLP. Table IV shows the measured vf-TLP I_{t2} for the PS, PD, NS, and ND combinations. The proposed design using POLY DSCR has higher I_{t2} than the STI design.

D. Comparison

A comparison is shown in Table V. The circuit of Fig. 11(a) ESD protection elements area is the power-rail ESD clamp circuit plus the four ESD diodes, which totals 13200 μm^2. The area of the ESD protection elements in the circuit of Fig. 11(b) is the sum of the four DSCR devices, which totals 5200 μm^2. The proposed design can achieve slightly higher ESD robustness than the traditional design with significant smaller area and much lower standby leakage current. The proposed design

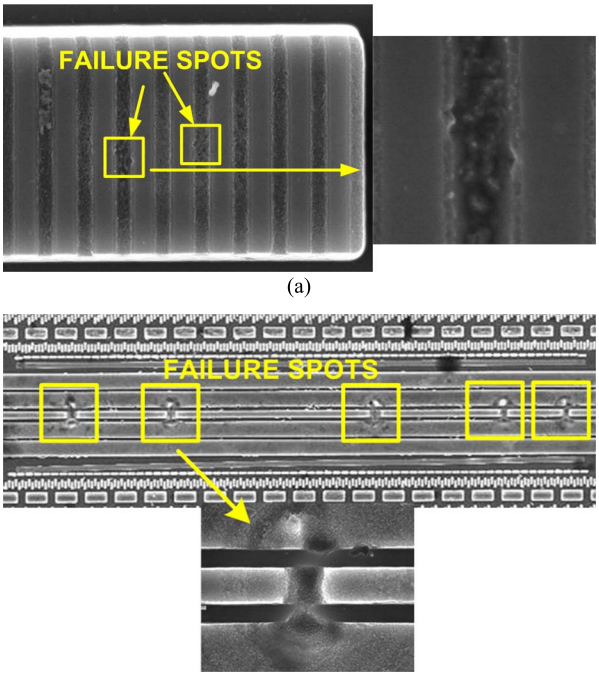

Fig. 13. (a) Failure location on the STI design after 275-V MM stress is located in the gate of the internal circuit. (b) Failure location on the POLY design after 375-V MM stress is located on the DSCR structure.

TABLE IV
VF-TLP MEASURED I_{t2} FOR THE DEMO CIRCUITS

Circuits	Positive to V_{SS}	Positive to V_{DD}	Negative to V_{SS}	Negative to V_{DD}
Fig. 11(a)	2.0A	4.8A	1.7A	4.2A
Fig. 11(b) STI	1.5A	2.0A	1.6A	2.1A
Fig. 11(b) POLY	2.8A	3.8A	2.9A	3.7A

TABLE V
CIRCUITS COMPARISON

Circuit	HBM	MM	Area
Fig. 11(a)	3.25kV	250V	13200μm^2
Fig. 11(b) STI	3.75kV	250V	5200μm^2
Fig. 11(b) POLY	3.75kV	350V	5200μm^2

also causes some leakage current at the IO pins, although it can be neglected since current handling of IO circuits is typically several orders of magnitude higher. On the other hand, if the leakage current is of concern, the DSCRs at the IO pad could be replaced by the traditional dual diodes [as that shown in Fig. 11(a)] at the expense of extra area, since 2 diodes require an total area of 3600 μm^2 but 1 DSCR only requires 1300 μm^2.

IV. DISCUSSIONS

The device holding voltage allows for operation with core and IO voltages up to 2.5 V without latch-up risk. Although

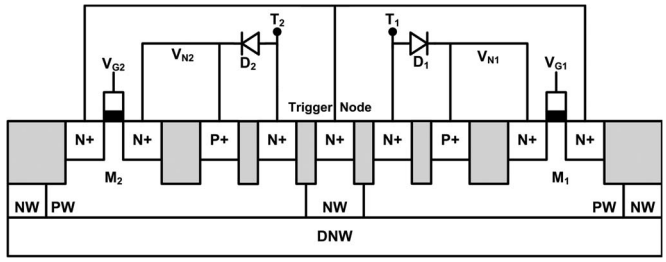

Fig. 14. Proposed modified circuit using a p-well-based DSCR structure. The connection to the RCR circuit (not shown) is identical to the one in Fig. 1(b).

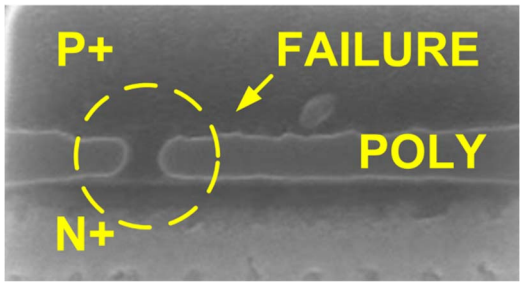

Fig. 15. FA image after vf-TLP failure of the proposed DSCR. Failure is located on D_2.

the leakage current for core voltage is very low, its exponential grow would cause very large leakage for IO voltages. In order to further reduce the leakage current, the transistors M_1 and M_2 could be replaced by thick-oxide devices, but the addition of extra masks would increase fabrication costs. Another solution would be to add extra diodes between the trigger transistors drain terminals and the trigger node [23]. These extra diodes would reduce drastically the leakage current, at the expense of extra silicon area.

It was mentioned in Section II the decision of the DSCR layout was in order to reduce leakage current, at the expense of having the trigger node tied to the substrate. The proposed device can be adapted to the NPNPN type DSCR layout with little modification. A proposed modification is shown in Fig. 14. The DSCR is realized with two p-wells and surrounded by an n-well isolation ring and deep n-well below. The embedded transistors are nMOS type, and the external diodes D_1 and D_2, connections are inverted since the wells types are changed.

It was noticed that the vf-TLP I_{t2} level of the proposed DSCR was lower than expected. Failure analysis has indicated that the failure after vf-TLP stress is located at the external diodes (D_1 and D_2). Fig. 15 shows the damage on D_2 after the positive vf-TLP stress from T_1 to T_2. Increasing the device size of diodes would increase the I_{t2} level.

V. CONCLUSION

A new dual silicon controlled rectifier (DSCR) was proposed and verified in a 40-nm CMOS process. By using the RCR trigger and embedding the trigger transistors in the DSCR n-wells, the circuit achieves symmetrical characteristics. In addition, the floating well technique allows to simultaneously triggering all parasitic bipolars in the DSCR, thus ensuring

fast turn-on speed. Moreover, the DSCR structure has holding voltage larger that the power-supply voltage, which eliminates latch-up issues. The proposed device was capable of protect the weak gate of the thin-oxide devices with the same ESD protection level than the traditional BIGFET, but required less silicon area and having much lower standby leakage current. In addition, a whole-chip ESD protection scheme was realized and verified using only the proposed DSCR structure. Such scheme would also benefit from lower design complexity.

ACKNOWLEDGMENT

The authors would like to thank Vanguard International Semiconductor Co. for measurement equipment support.

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