國立陽明交通大學

前瞻半導體研究所

碩 士 論 文

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Master Thesis

具有電源重啟功能的過流閂鎖防護電路

Latch-up Over-current Protection Circuit with Power Restarted Function

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摘要

在 CMOS 積體電路中，閂鎖效應是一個常見的可靠度問題，由電路內部的寄生矽控整流器結構所引起。當這個結構意外被觸發時，會在電源和接地之間產生一個低阻抗路徑，造成大電流流動。如果無法及時關閉，高電功率累積的熱量可能導致矽晶片造成損壞及燒毀，從而影響晶片的正常運作。

在本研究中，提出了一種過流保護設計，當電路發生閂鎖時，此設計可以檢測閂所導致的過流事件的發生，並通過關閉電源來讓閂鎖效應停止，隨後在一段可設定的延遲後，重新啟動電源。若是重啟電源後仍處於過流狀態，則會不斷地進行關斷直到過流現象解除。此設計的目的為減輕由閂鎖引發的硬體故障，並透過及時的電源恢復電路的正常運作。

此設計利用 0.18 微米的製程實現，電路中包含了保護電路及內部電路。內部電路用於模擬 CMOS 積體電路中容易發生閂鎖的區塊，而保護電路則是負責保護內部電路避免被閂鎖燒毀。並且，晶片的總面積為 0.349 平方毫米，其中保護電路僅占了 0.0135 平方毫米。此設計獨立於電源管理積體電路，此外晶片面積非常小且能控制電源關斷的時間，使得此設計具有相當大的應用彈性。最後，本論文驗證了此保護電路的可靠性。在保護電路運作的過程中，當有過流事件發生時，保護電路能及時的關閉電源，以避免閂鎖事件導致晶片發生不可逆的損壞。

關鍵詞/字 — 閂鎖、寄生矽控整流器、電路解決方案、過流保護、電源重啟、打嗝電路

Latch-up Over-current Protection Circuit with Power Restarted Function

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Abstract

Latch-up is a common reliability issue in CMOS integrated circuits caused by the parasitic silicon-controlled rectifier (SCR) structure within the circuit. When this structure was accidentally triggered on, it creats a low-impedance path between the power supply (VDD) and the ground (VSS), causing a large current flow. If not promptly deactivated, the accumulated heat from high electrical power can irreversibly damage and burn out the silicon die, affecting its normal operation.

In this study, an over-current protection design is proposed to mitigate latch-up events in circuits. This design detects over-current incidents triggered by latch-up and halts the effect by cutting off the power supply. After a programmable delay, the power is restored. If the over-current condition persists after restart, the design repeatedly shuts down until the over-current issue is resolved. The purpose of this design is to prevent hardware failures caused by latch-up events and to restore normal circuit operation through timely power restarts.

The design is implemented using a 0.18-μm process, comprising both a protection circuit and an internal circuit. The internal circuit simulates areas susceptible to latch-up within CMOS integrated circuits, while the protection circuit safeguards the internal circuit against latch-up-

induced damage. The total chip area is 0.349 square millimeters, with the protection circuit occupying only 0.0135 square millimeters. This design operates independently of the power management integrated circuits and requires minimal chip area, offering flexible control over power turn-off time and broad application versatility. Finally, this paper validates the reliability of the protection circuit. During operation, the protection circuit promptly shuts down the power supply upon detecting an over-current event, effectively preventing irreversible damage to the chip from latch-up incidents.

Keywords — Latch-up, Silicon-controlled Rectifier (SCR), Circuit Solution, Over-current Protection (OCP), Power Restart, Hiccup Circuit