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碳化矽高壓元件之靜電放電與浪湧能力調查

Investigation of ESD and Surge Robustness of SiC HV Devices

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摘要

隨著寬能隙半導體技術的快速發展，4H 型碳化矽(4H-SiC)元件因其高溫、高電壓及高功率處理能力，在功率電子應用中受到廣泛關注。相較於傳統矽(Si)元件，碳化矽在特定應用場景下展現出更優異的性能，使其成為更具競爭力的選擇。為了進一步提升碳化矽功率元件的效能，將低壓驅動電路與高壓垂直雙植入電晶體 (VDMOSFET) 集成於同一碳化矽晶圓上，可有效減少寄生效應、提高功率模組密度，並提升整體系統效能。然而，確保整合型碳化矽電路與獨立碳化矽功率元件在靜電放電 (ESD) 與浪湧 (Surge) 事件下的可靠性，仍然是關鍵挑戰之一。

本研究分析了碳化矽 PMOSFET 和 VDMOSFET 的 ESD 耐受能力，以及 VDMOSFET 的浪湧耐受能力，以開發適用於單獨 VDMOSFET 元件與整合閘極驅動電路和 VDMOSFET 於同一片晶圓上的整合晶片的 ESD 防護策略。透過傳輸線脈衝（TLP）及人體模式（HBM）測試來評估 ESD 耐受能力，對於 PMOSFET，研究針對傳統寄生二極體特性(GDPMOS)與閘極氧化層崩潰電壓進行測試，提供 SiC CMOS ESD 設計限制條件的關鍵參數，如元件在 ESD 情況下的閘極氧化層崩潰電壓。

對於 VDMOSFET 的研究，結果顯示在閘極-源極模式下的 ESD 耐受能力最差，其主要失效機制為 ESD 電流充電導致閘極氧化層跨壓增加，最終造成閘極氧化層崩潰，其中失效分析顯示閘極-源極間的對打損壞位置集中於主動區域邊緣，而汲極-閘極間的

施打損壞位置位於主動區內。由於 VDMOSFET 結構的特性，當施打正 ESD 於汲極-閘極(+DG)時，空乏區會形成保護作用，使電壓不會直接施加於氧化層上，因此+DG 模式下的 ESD 耐受性高於-DG 模式。此外，研究發現增加 VDMOSFET 的主動面積能夠有效提升所有模式下的 ESD 耐受能力。針對單獨 VDMOSFET，提出了一種利用晶片外瞬態電壓抑制二極體(TVS diode)來提升元件 ESD 耐受能力的防護方案，在不影響元件正常操作的情況下，顯著提升 ESD 可靠性。

在 VDMOSFET 的浪湧耐受能力方面，研究顯示閘極氧化層崩潰是主要的失效機制，且浪湧耐受能力並不會隨著元件主動區增加而增加。測試結果表明，當施加 50V 以上的重複浪湧脈衝時，元件的電性會發生衰退(如閾值電壓下降)，但 40V 以內的浪湧則不會導致顯著影響。此外，雖然 ESD 在充電過程中比浪湧事件更快達到電壓峰值，但實際放電時間量測結果顯示可達微秒等級，在較大的元件中甚至更長。因此，為確保長期可靠性，靜電放電及浪湧防護裝置應將瞬態電壓限制在 40V 以下。

為了提升碳化矽功率元件的 ESD 耐受能力，本研究提出適用於整合電路(閘極驅動電路 ＋VDMOSFET)及單獨 VDMOSFET 元件的晶片上(On-chip)全晶片 ESD 防護策略。針對單獨 VDMOSFET，提出雙向自偏壓矽控整流器(Self-Biased Dual-Directional SCR)，可在不影響正常操作電壓範圍(−5V 至+20V)的條件下提供有效的 ESD 防護。此外，本研究亦詳細說明整合碳化矽電路的各個 ESD 防護元件的設計細節與應用。

本研究的結果為碳化矽功率元件在靜電放電及浪湧防護設計上的可靠性評估提供了重要的設計參數與應用策略，有助於提升碳化矽高功率模組的可靠性與長期穩定性。

關鍵詞/字 — 靜電放電、氧化層擊穿、人體放電模型、低電壓觸發矽控整流器、P 型金屬氧化物半導體場效應電晶體、可靠度、碳化矽、矽控整流器、基板觸發矽控整流器、浪湧、傳輸線脈衝、垂直雙重植入金屬氧化物半導體場效應電晶體。

Investigation of ESD and Surge Robustness of SiC HV Devices

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Abstract

With the rapid advancement of wide bandgap (WBG) semiconductor technology, 4H-SiC devices have garnered significant attention in power electronics applications due to their high-temperature, high-voltage, and high-power handling capabilities. Compared to traditional silicon (Si) devices, SiC exhibits superior performance in specific applications, making it a more competitive alternative. To further enhance the efficiency of SiC power devices, integrating low-voltage gate driver circuits with high-voltage vertical double-implanted MOSFETs (VDMOSFETs) on the same SiC wafer has emerged as a viable approach to reduce parasitic effects, increase power module density, and improve overall system efficiency. However, ensuring the reliability of both monolithic integrated SiC circuits and standalone SiC power devices under electrostatic discharge (ESD) and surge stress remains a critical challenge.

This study analyzes the ESD robustness of SiC PMOSFETs and VDMOSFETs and the surge robustness of SiC VDMOSFETs to develop effective ESD protection strategies for both discrete VDMOSFETs and monolithic integrated VDMOSFET and gate driver circuit. Transmission Line Pulse (TLP) and Human Body Model (HBM) testing were conducted to assess ESD robustness. For PMOSFETs, the study focuses on the conduction characteristics of

parasitic diodes (GDPMOS) and gate oxide breakdown voltage, providing key design constraints for SiC CMOS ESD protection, particularly in determining the breakdown voltage of gate oxides under ESD conditions.

For VDMOSFETs, the results indicate that the GS mode (Gate-to-Source) exhibits the lowest ESD robustness, with the primary failure mechanism being oxide breakdown caused by ESD current charging, leading to increased gate oxide stress and eventual breakdown. The failure analysis indicated that the GS mode ESD-induced failures were predominantly observed at the edges of the active region, while the DG mode (Drain-to-Gate) ESD-induced failure occurred within the active region. Due to the structural characteristics of VDMOSFETs, positive DG (+DG) ESD pulses induce a depletion region, which prevents the direct application of voltage to the gate oxide, resulting in higher ESD robustness for +DG mode compared to -DG mode. Furthermore, increasing the active area of VDMOSFETs effectively enhances ESD robustness across all modes. For standalone VDMOSFETs, this study proposes an ESD protection scheme utilizing an off-chip transient voltage suppression (TVS) diode, which significantly improves ESD resilience without affecting normal device operation.

Regarding the surge robustness of VDMOSFETs, the study confirms that gate oxide breakdown is the primary failure mechanism, and that increasing the active area does not enhance surge robustness. Experimental results indicate that repeated 50V surge pulses lead to threshold voltage degradation, whereas 40V surge pulses do not cause noticeable deterioration. Additionally, although ESD events reach peak voltage more rapidly than surge events during the charging phase, actual discharge times were measured in the microsecond range, and in larger devices, even longer durations were observed. To ensure long-term reliability, it is recommended that transient voltages be limited to below 40V for both ESD and surge protection mechanisms.

To improve the ESD robustness of SiC power devices, this study proposes a comprehensive on-chip ESD protection strategy for both integrated circuits (gate driver + VDMOSFET) and standalone VDMOSFET devices. For discrete VDMOSFETs, a Self-Biased Dual-Directional Silicon-Controlled Rectifier (SBDDSCR) is introduced, providing effective ESD protection without interfering with operational voltage range of -5V to +20V. Additionally, this study provides a detailed analysis of various ESD protection devices for integrated SiC circuits, covering their design considerations and applications.

The findings of this study contribute to the reliability assessment and optimization of ESD and surge protection strategies for SiC power devices, providing crucial design parameters and implementation strategies. These insights will aid in enhancing the reliability and long-term stability of high-power SiC modules.

Keywords — electrostatic discharge (ESD), gate oxide breakdown, human-body-model (HBM), low-voltage triggered SCR (LVTSCR), PMOS, reliability, silicon carbide (SiC), silicon control rectifier (SCR), substrate triggered SCR (STSCR), surge, transmission line pulse (TLP), vertical double-implanted MOSFET (VDMOSFET).