國立陽明交通大學

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碩士論文

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Master Thesis

鰭狀製程晶片中靜電放電與浪湧防護之電源線箝位電路

Power-Rail Clamp Circuit for ESD and Surge Protection in FinFET Integrated Circuits

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摘要

本研究專注於在 FinFET 技術中實現靜電放電（ESD）的穩健性和過度電性應力（EOS）浪湧免疫力之間取得平衡。由於有效矽體積減少、散熱變差和擊穿電壓降低，FinFET 元件對長脈衝 EOS 事件的敏感性日益增加。目前在業界中主要依賴電路設計的方法來減輕 EOS 的浪湧事件。然而，在電路設計中面臨幾個關鍵挑戰，包括設計複雜性、響應延遲和功耗等問題，這些都需要謹慎考量。為了克服這些挑戰，本論文全面探討了元件層面人體模型(HBM)的穩健性和浪湧免疫力的綜合分析策略。

傳統上，全矽化的閘極驅動（fully silicide gate-driven）NMOS 經常被使用作為電源線箝位電路以增強人體模型的穩健性；然而，它並不適合用來處理長脈衝 EOS 的浪湧事件。尤其是在 FinFET 製程的結構中，有效的矽體積變小，使這些元件對此類事件更為脆弱，造成損壞的面積更大。

本論文探索了一種針對浪湧免疫力同時提升人體模型性能，提出的創新解決方案，通過幾項利用 FinFET 工藝的設計規則和佈局技術實現了平衡的結構設計，以及有效應用該工藝來增強元件的穩健性。因此，在電源線箝位電路中使用汲極平衡 (drain-ballasted) 的結構來增強浪湧免疫力，並且插入帶有輕摻雜（lightly doped drain）植入的虛擬閘，有效降低汲極表面的串聯電阻，有助於改善 HBM 性能。這種改善方式需搭配指定的設

計規則，以降低汲極端的電阻並將驅動電流提高從 0%至 40%。而此論文探討汲極電阻的降低至關重要，不僅僅提升 HBM 性能最高可達 6.8kV 以及浪湧免疫力最高可達 22V 以上的能力，且能夠允許更高效的均勻電流流動，使驅動電流增加，進一步增強了元件的整體驅動能力。

重要的是，這些改進是在不需要額外光罩及製程步驟的情況下實現的，從而簡化了製造過程，並降低了製造成本及其複雜性。整體而言，這種方法不僅增強了元件對 ESD 和浪湧事件的穩健性，還優化了其電氣性能，代表了 FinFET 技術的一項重大進展。這一創新設計已進入專利申請過程，顯示出其新穎性和在該領域的潛在重要性。

此論文中的所有數據，包括實驗結果、測量數據及研究中討論的發想及概念，均通過使用聯華電子（UMC）14nm FinFET 技術的驗證過程中獲得，這一驗證確保了數據的可靠性及其與所研究特定技術的相關性，為研究獲得的結論提供了堅實的基礎。

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Abstract

The study focuses on achieving a balance design between Electrostatic Discharge (ESD) robustness and Electrical Overstress (EOS) Surge immunity enhancement for FinFET technology. FinFET devices become increasingly susceptible to long pulse EOS events due to reduced effective silicon volume, worse thermal dissipation, and lower breakdown voltage. Currently, industry practices primarily depend on circuit design methodologies to mitigate EOS Surge events. However, several critical challenges must be addressed in circuit design, including design complexity, response delay, and power consumption. To overcome these issues, this paper provides a comprehensive analysis of strategies to enhance HBM robustness and Surge immunity at the component level.

Traditionally, a fully silicide gate-driven NMOS has been employed as a power-rail clamp circuit to enhance Human Body Model (HBM) robustness; however, it is not suitable for handling long pulse EOS Surge events. Especially, the smaller effective silicon volume in FinFET structures makes these devices more vulnerable to such events, resulting in a larger area of damage.

This paper explores an innovative solution aimed at enhancing Surge immunity while improving HBM robustness. It achieves a balanced structural design through several design rules and layout techniques utilizing FinFET technology, along with effective applications to enhance component robustness. Therefore, a drain-ballasted structure is used in the power rail clamp circuit to enhance Surge immunity, and a dummy gate with lightly doped drain (LDD) implantation is introduced to effectively reduce the surface series resistance at the drain, which helps improve HBM performance. This improvement requires specific design rules to lower the resistance at the drain and increase the driving current from 0% to 40%. The paper discusses the critical importance of reducing drain resistance, not only enhancing HBM performance up to 6.8kV and achieving Surge immunity up to 22V, but also to allow for more efficient uniform current flow, thereby increasing the driving current and further enhancing the overall driving capability of the device.

Importantly, these improvements were achieved without the necessity for additional masks and process steps, simplifying the fabrication process and reducing both manufacturing costs and complexity. Overall, this approach not only enhances the robustness of the components against ESD and Surge events but also optimizes their electrical performance, representing a significant advancement in FinFET technology. The innovative design has entered the patent application process, indicating its novelty and potential significance in the field.

All data presented in this paper, including experimental results, measurement data, and the concepts discussed, were obtained through validation processes using United Microelectronics Corporation (UMC) 14nm FinFET technology. This verification ensures the reliability of the data and its relevance to the specific technology studied, providing a solid foundation for the conclusions drawn from the research.