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Master Thesis

650-V 氮化鎵金屬－絕緣層－半導體高電子遷移率電晶體與 1700-V 碳化矽垂直雙擴散金氧半場效電晶體之靜電放電保護設計與驗證

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摘要

本研究針對 650-V 氮化鎵金屬－絕緣層－半導體高電子遷移率電晶體（650-V GaN MIS-HEMTs）及 1700-V 碳化矽垂直雙擴散金氧半場效電晶體（1700-V SiC VDMOSFETs）進行元件級 ESD 研究，涵蓋不同施加模式及極性，並使用人體模型（Human Body Model, HBM）、傳輸線脈衝（Transmission Line Pulse, TLP）、靜電槍（ESD gun）及浪湧（Surge）測試，分析兩類功率元件在實際放電下的行為特性。

對於耗盡型（D-mode）及級聯式增強型（E-mode, cascode）GaN MIS-HEMTs，結果顯示兩類元件在閘極－源極(GS)模式下最為脆弱，而汲極－源極(DS)模式較為穩健。失效分析指出，D-mode 元件損壞集中於多指閘極至源極的絕緣層，cascode 結構則於低壓 MOSFET 主動區邊界的氧化層角落發生擊穿，皆與局部電場集中相關。施加不同條件的測試結果顯示，元件耐受度受施打極性及模式影響明顯。本研究提出在電路板層級的單向瞬間電壓抑制器(TVS)保護電路，可提升 cascode GaN MIS-HEMT 之 ESD GS 模式下之耐受度至 8 kV 以上，同時保持正常操作與漏電特性，因此進一步提出共封裝雙向 TVS 設計，有助於節省電路板面積並降低封裝寄生效應，該 co-packaged 設計仍在製作階段，未來將持續完成測試以驗證 ESD 耐受度與高頻開關條件下的性能。

根據過去的研究指出，1700-V SiC VDMOSFET 在 GS 及汲極－閘極(DG)模式下的 ESD 耐受度較差，其中 GS 模式最為關鍵，閘極氧化層在 TLP 測試下僅能承受約 62 V，需透過保護電路及時觸發以避免擊穿。為此，本研究提出在離散型 VDMOSFET 內嵌整合 20-V CMOS 區的保護電路設計，包含了矽控整流器(SCR)結合高濃度 P 型摻雜區以降低觸發電壓，以及動態基底偏壓(Dynamic Body Bias)電路。透過交叉耦合 NMOS 將基底電位在工作電壓為+20 V 與-5 V 時，皆鉗位至系統最低電壓，確保所有 PN 接面不會導通而發生漏電。測試結構設計涵蓋多種 SCR 結構，以優化觸發電壓、維持電壓及 ESD 放電能力，達成>2 kV 耐受度、<62 V 觸發電壓與>20 V 維持電壓。該架構可改善 GS 與-DG 模式的 ESD 耐受度，並兼容負閘極偏壓操作。保護電路設置於 VDMOSFET 閘極焊墊(PAD)下方，以減少電路布局面積。由於測試晶片仍在製作中，未來將持續完成 ESD 相關及雙脈衝測試，驗證元件的 ESD 保護能力、整合元件的正常工作性能，以及 PAD 下電路設計的有效性。

本研究系統性分析氮化鎵與碳化矽功率元件在不同 ESD 與 Surge 應力下的耐受度，並提出相對應的元件層級 ESD 保護設計，為後續提升功率元件 ESD 耐受度的研究提供重要依據。

關鍵詞/字 — 氮化鎵金屬－絕緣層－半導體高電子遷移率電晶體、碳化矽垂直雙擴散金氧半場效電晶體、靜電放電、人體模型、傳輸線脈衝、耗盡型、級聯式增強型、瞬間電壓抑制器、共封裝、矽控整流器、動態基底偏壓電路、焊墊下電路設計。

Design and Verification on ESD Protection for 650-V GaN MIS-HEMTs and 1700-V SiC VDMOSFETs

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Abstract

This study conducts device-level ESD investigations on 650-V GaN metal–insulator–semiconductor high-electron-mobility transistors (MIS-HEMTs) and 1700-V SiC vertical double-diffused MOSFETs (VDMOSFETs) under various stress modes and polarities, employing human body model (HBM), transmission line pulse (TLP), ESD gun, and surge testing to analyze device behavior under actual discharge conditions.

For both depletion-mode (D-mode) and cascode enhancement-mode (E-mode) GaN MIS-HEMTs, the results indicate that the devices are most vulnerable in the Gate-to-Source mode (GS mode), whereas the Drain-to-Source mode (DS mode) is more robust. Failure analysis shows that D-mode devices fail predominantly in the multi-finger Gate–Source (G–S) insulation layer, while the cascode structure exhibits breakdown at the oxide corners of the low-voltage n-MOSFET (LVNMOS) active region, both associated with local electric field concentration. The test results under different conditions reveal that device robustness is significantly influenced by stress polarity and mode. A unidirectional transient voltage suppressor (TVS) protection circuit at the PCB level is proposed, which enhances the GS mode ESD robustness of cascode GaN MIS-HEMTs to over 8 kV while preserving normal operation

and leakage characteristics. Furthermore, a co-packaged bidirectional TVS design is proposed to save PCB area and reduce parasitic effects; this co-packaged design is currently under fabrication, with future testing planned to validate ESD robustness under high-frequency switching conditions.

Previous studies have indicated that 1700-V SiC VDMOSFETs exhibit lower ESD robustness in GS mode and Drain-to-Gate mode (DG mode), with the GS mode being most critical. The gate oxide can withstand only approximately 62 V under TLP testing, necessitating timely protection circuit triggering to prevent breakdown. To address this, a protection circuit integrating a 20-V CMOS region within the discrete VDMOSFET is proposed, including a silicon-controlled rectifier (SCR) with a high-concentration P-type doped region to lower the trigger voltage and a dynamic body bias (DBB) circuit. Through cross-coupled NMOS devices, the body potential is clamped to the system's lowest potential at both operating voltages of +20 V and -5 V, ensuring that all PN junctions remain non-conductive and preventing leakage. The test structure incorporates various SCR configurations to optimize trigger voltage, holding voltage, and ESD discharge capability, achieving >2 kV robustness, <62 V trigger voltage, and >20 V holding voltage. This architecture improves ESD robustness in both GS and -DG modes and is compatible with negative gate bias operation. The protection circuit is placed beneath the VDMOSFET gate PAD to reduce layout area. As the test chips are still under fabrication, further ESD and double-pulse test (DPT) will be conducted to validate device protection, integrated device performance, and the effectiveness of circuit-under-PAD design.

This study systematically analyzes the ESD and surge robustness of GaN and SiC power devices under various stress conditions and proposes corresponding device-level ESD protection designs, providing a critical reference for future research on improving the ESD robustness of power devices.

Keywords — GaN MIS-HEMT, SiC VDMOSFET, electrostatic discharge, human body model, transmission line pulse, depletion-mode, cascode enhancement-mode, transient voltage suppressor, co-packaged, silicon-controlled rectifier, dynamic body bias circuit, circuit-under-PAD design.