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互補式金氧半積體電路之後段製程連線可靠度與晶片內浪湧
防護研究
Study on Back-End-of-Line Interconnection Reliability and On-
Chip Surge Protection in CMOS Integrated Circuits

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互補式金氧半積體電路之後段製程連線可靠度與晶片內浪湧防護研究

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摘要

隨著消費性電子產品朝向高速傳輸、高功率充電與小型化系統整合發展，外部輸入介面與充電連接埠在製造、組裝與實際使用過程中，容易受到靜電放電與浪湧等暫態事件衝擊，進而造成介面電路劣化或永久性損壞。對 CMOS 積體電路而言，晶片內暫態防護能力不僅取決於前段製程 ESD 防護元件的觸發電壓、箝制特性與導通阻抗，亦受到後段製程金屬連線、接觸孔與通孔之載流能力，以及 I/O 防護元件於不同脈衝寬度下失效行為的影響。因此，本論文針對 CMOS 積體電路之後段製程連線可靠度與晶片內浪湧防護設計考量進行研究。

首先，本研究於 0.18- μm CMOS 製程中實作金屬線、接觸孔與通孔測試結構，並分別施加傳輸線脈衝與浪湧脈衝，以比較短脈衝與長脈衝暫態應力下之失效特性。實驗結果顯示，後段製程連線結構之損傷機制與脈衝寬度密切相關。傳輸線脈衝容易造成局部快速升溫與熔毀，而浪湧脈衝則因脈衝時間較長，受總輸入能量、熱擴散與熱機械應力影響更為明顯。此結果說明，在進行晶片內浪湧防護設計時，不能僅以短脈衝 ESD 測試結果推估後段製程連線於浪湧條件下的可靠度。

接著，本論文於 0.18- μm 5-V CMOS 製程中，針對多種常見與改良式 ESD 防護元件進行浪湧耐受度評估。測試結構包含 GGNMOS、GDPMOS，以及具觸發輔助、電流路徑調變與串聯阻抗設計之元件。實驗結果顯示，元件尺寸與結構設計皆會影響浪湧耐受度，而部分以改善 ESD 觸發特性為目的的結構，在長脈衝浪湧條件下並不一定具有較佳的浪湧耐受度。其中，具有 N-well ballast resistance 之 NMOS 元件展現較高的表觀浪湧耐受度，然而其較大的導通阻抗可能導致較高的箝制電壓，進而產生無法有效保護內部

電路的疑慮。因此，浪湧防護元件的評估不應僅考慮元件本身是否失效，也必須同時考慮箝制電壓與受保護電路之耐壓能力。

此外，本論文進一步探討 PESD 摻雜對靜電放電防護設計在浪湧條件下耐受特性之影響。實驗結果顯示，PESD 摻雜雖可提升部分輸出入介面元件之 HBM 靜電放電耐受度，卻可能降低其浪湧耐受能力，顯示 ESD 強化設計與浪湧防護能力之間存在潛在權衡關係。此結果說明，製程或佈局上的 ESD enhancement option 在導入高可靠度輸出入介面前，應同時評估其對浪湧耐受度與實際箝制行為之影響。

綜合上述結果，本論文指出晶片內浪湧防護不能僅由靜電放電耐受度保證，而必須同時考慮後段製程連線、ESD 防護元件、製程與佈局選項、箝制電壓、內部電路耐受能力以及全晶片放電路徑。相關研究結果可作為未來輸出入介面與電源箝制電路於浪湧需求下進行共同設計之參考。

關鍵字： 靜電放電、浪湧、傳輸線脈衝、後段製程、金屬連線可靠度、晶片內浪湧防護、PESD 摻雜、CMOS 積體電路

Study on Back-End-of-Line Interconnection Reliability and On-Chip Surge Protection in CMOS Integrated Circuits

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Abstract

With the development of consumer electronics toward high-speed transmission, high-power charging, and compact system integration, external input/output interfaces and charging connectors are increasingly exposed to transient events, such as electrostatic discharge and Surge stresses, during manufacturing, assembly, and field operation. These transient events may induce degradation or permanent damage in interface circuits. For CMOS integrated circuits, the on-chip transient protection capability is not only determined by the triggering voltage, clamping characteristics, and turn-on resistance of front-end ESD protection devices, but is also directly affected by the current-handling capability of back-end-of-line metal interconnections, contacts, and vias, as well as the failure behavior of I/O protection devices under different pulse durations. Therefore, this thesis investigates the reliability of back-end-of-line interconnections and the design considerations of on-chip Surge protection in CMOS integrated circuits.

First, metal-line, contact, and via test structures were fabricated in a 0.18- μm CMOS technology and characterized using transmission-line-pulse (TLP) and Surge stresses. The results show that failure mechanisms strongly depend on pulse duration. TLP stress mainly causes rapid local heating and melting, whereas long-pulse Surge stress is more strongly influenced by total input energy, heat diffusion, and thermomechanical stress. Therefore, Surge reliability of BEOL interconnections cannot be directly predicted from short-pulse ESD results alone.

Second, conventional and modified ESD protection devices were evaluated under Surge stress in a 0.18- μm 5-V CMOS technology. The tested structures included GGNMOS, GDPMOS, and devices incorporating trigger assistance, current-path modulation, or series-impedance designs. The results show that Surge immunity is affected by device dimensions and structural design. However, structures designed to improve ESD triggering do not necessarily provide better long-pulse Surge immunity. Among the tested devices, the NMOS device with N-well ballast resistance exhibited a higher measured Surge level. However, its increased turn-on resistance may raise the clamping voltage and reduce protection effectiveness for internal circuits. Thus, Surge-protection evaluation must consider device failure current, clamping voltage, and the voltage tolerance of protected circuits.

Furthermore, the influence of PESD implantation on Surge immunity was investigated. Although PESD implantation can improve HBM ESD robustness for certain I/O devices, it may degrade Surge performance, revealing a trade-off between ESD enhancement and Surge immunity.

In summary, on-chip Surge protection cannot be ensured by ESD robustness alone. BEOL interconnections, protection devices, process and layout options, clamping voltage, internal-circuit tolerance, and whole-chip discharge paths must be co-optimized. These results provide design references for Surge-tolerant I/O interfaces and power-clamp circuits.

Keywords: Electrostatic Discharge, Surge, Transmission-Line Pulse, Back-End-of-Line, Metal Interconnection Reliability, On-Chip Surge Protection, PESD Implant, CMOS Integrated Circuits