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Doctoral Dissertation

寬能隙半導體積體電路之靜電放電防護, 閂鎖效應防治, 及安全操作區域提升之設計與驗證

Design and Verification on ESD Protection, Latchup Prevention, and SOA Enhancement for Wide-Bandgap Semiconductor-Based Integrated Circuits

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摘　要

本論文探討寬能隙半導體技術中關鍵的可靠度與設計挑戰，特別聚焦於氮化鎵（GaN）與 SiC（碳化矽）兩種半導體材料。由於這兩種材料具備優異的電性特性，已逐漸被廣泛應用於高功率系統中。隨著高功率系統對可靠度的要求日益嚴格，迫切需要發展對應的設計方案，以提升寬能隙半導體積體電路的穩健性。因此，本論文聚焦於三項關鍵議題：靜電放電（ESD）、閂鎖效應（Latchup）以及安全操作區域（SOA），以確保寬能隙半導體元件與電路在實際應用中的可靠性。針對上述挑戰，本論文進行了一系列元件層級與電路層級的研究與分析。

關於 GaN 技術方面，本研究針對 1200-V 離散型（Stand-alone）金屬絕緣物半導體高電子遷移率電晶體（MIS-HEMT）的 ESD 耐受度進行評估。實驗結果顯示，即使元件面積已相當大，其閘極到源極之間的 ESD 防護能力仍偏低。此外，傳輸線脈衝系統（transmission line pulse system, TLP）量測結果與 人體放電模型（human-body model, HBM）測試水準之間缺乏一致性，凸顯了針對此種 GaN 元件，需要直接進行 HBM 測試以評估其 ESD 能力的重要性。此外，本論文亦於 0.5 微米 GaN-on-Si 製程中設計並驗證多款電源軌間靜電放電防護電路(Power-rail ESD clamp circuit)。每種設計都將在各小節中逐一探討研究動機以及設計考量。藉由重要的指標參數進行各個設計的比較，可

以得知各個設計的優缺點。最終，由實驗結果得到，一種具備動態時間與電壓偵測功能之設計，展現出優異的 HBM 保護能力、高面積效率與低功耗，極具應用潛力。

關於 SiC 技術，本論文分析了四種典型的 ESD 防護元件，包括 Gate-grounded NMOS（GGNMOS）、Gate-V_{DD} PMOS（GDPMOS）、N+/PW 二極體與 P+/NW 二極體。研究顯示，無論是增加 MOS 類元件的手指數量（Finger number），或是擴大二極體的周長，均僅提升順向導通之 ESD 耐受度。比較效能指標（Figure of merit, FoM），二極體之效能優於 MOS 類元件，更適合做為該製程中的 ESD 防護元件。此外，為實現全晶片 ESD 防護設計，本論文提出數種適用於 SiC 製程之電源軌間靜電放電防護電路。

本論文亦進一步研究了 SiC 互補式金屬氧化物半導體（Complementary Metal-Oxide-Semiconductor, CMOS）結構中之閂鎖效應。經由實驗證實，SiC CMOS 結構中寄生的矽控整流器（SCR）路徑具有閂鎖效應的風險。透過增加陽極與陰極之間的距離，可有效提升維持電壓（Holding voltage），進而增強抗閂鎖效應之免疫力。此研究同時強調，未來應為 SiC 之晶片製程建立明確的防閂鎖效應設計規範，以提升積體電路系統之抗閂鎖效應之免疫力，並確保其穩定運作。

此外，本論文亦分析了 4H-SiC 垂直雙植入金氧半場效應電晶體（Vertical Double-implantation MOSFET, VDMOSFET）之電性安全操作區域（eSOA）與非箝位電感性切換（UIS）之可靠度。從 TLP 量測到的電壓電流曲線中可觀察到驟回（snapback）現象，顯示寄生雙極性電晶體（BJT）已被觸發。在 UIS 測試中，寄生 BJT 亦會因過高的 V_{DS} 瞬間突波電壓而被觸發，進而導致元件燒毀並失效。為提升切換操作時的可靠度，本研究提出一種改良型的 1700-V VDMOSFET 元件結構，藉由延伸 P+ 區域來降低寄生 BJT 之基極電阻（Base resistance），以抑制寄生 BJT 的導通。該結構在不影響切換速度與切換損耗的前提下，顯著提升了 eSOA 與 UIS 表現。

總結而言，本論文提出多項全面性的設計策略，致力於提升 GaN 與 SiC 半導體元件與電路的可靠度，研究焦點涵蓋靜電放電防護、閂鎖效應防治以及安全操作區域提升。透過元件與電路層級的深入分析與實作，本研究為提升寬能隙半導體及積體電路之可靠度提供具體設計參考。

關鍵詞：寬能隙半導體、積體電路、氮化鎵、碳化矽、靜電放電、閂鎖效應、安全操作區域。

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Abstract

This dissertation investigates critical reliability and design challenges in wide-bandgap semiconductor technologies, with a particular focus on GaN and SiC. These materials have been increasingly applied in high-power systems due to their superior electrical properties. Due to the stricter reliability requirements of high-power systems, the corresponding method to enhance the robustness of wide-bandgap semiconductor integrated circuits is urgently needed. Hence, this dissertation focuses on three critical issues: electrostatic discharge (ESD), latchup, and the safe operating area (SOA). To address these challenges, a series of studies was conducted across device-level analysis and circuit-level design to ensure the robustness of wide-bandgap semiconductor devices and circuits.

For GaN-based devices, the ESD robustness was evaluated on a 1200-V MIS-HEMT. It was observed that the device exhibited a low ESD level in the gate-to-source region even with a large device size. Transmission line pulse (TLP) results did not correlate with human-body model (HBM) ESD robustness, highlighting the importance of direct HBM testing. In addition, several power-rail ESD clamp circuits were designed and verified in a 0.5-μm GaN-on-Si

process. The design motivation and considerations for each circuit are discussed in detail in the corresponding subsections. By comparing key performance metrics, the advantages and limitations of each design can be clearly identified. Finally, based on the experimental results, the proposed design with a dynamic timing-voltage detection function provided robust HBM level, higher area efficiency, and lower power consumption.

In SiC-based technology, four typical ESD devices were characterized, including Gate-grounded NMOS (GGNMOS), Gate-V_{DD} PMOS (GDPMOS), N+/PW diode, and P+/NW diode. It was found that increasing the number of fingers in MOS-based devices or enlarging the perimeter of the diodes enhanced ESD robustness only under forward-conduction conditions. The diodes demonstrated a higher figure of merit than MOS-based devices, making them more suitable for ESD protection in this process. Moreover, to realize the whole-chip ESD protection, some designs of the power-rail ESD clamp circuit for the SiC process were also proposed.

Latchup characteristic in the SiC CMOS structure was also studied. Experimental results confirmed the presence of latchup risk caused by the parasitic silicon-controlled rectifier (SCR) path. It was shown that increasing the anode-to-cathode spacing raised the holding voltage and improved latchup immunity. This study emphasized the need to define design rules of latchup prevention for SiC-based integrated circuits.

Furthermore, the electrical SOA (eSOA) and unclamped inductive switching (UIS) robustness of 4H-SiC VDMOSFETs were analyzed. The snapback phenomenon can be observed from the TLP measured *I-V* curves, which indicate that the parasitic BJT was triggered. Under the UIS test, the parasitic BJT was triggered due to high overshooting V_{DS} voltage, which could cause device failure. To enhance switching reliability, an improved 1700-V device structure with an extended P+ region was proposed. A longer P+ region will result in a lower base resistance, which will restrain the parasitic BJT from triggering. This modification significantly enhanced eSOA and UIS performance without compromising switching speed or

switching loss. The improved method will not increase manufacturing costs or complexity.

In summary, this dissertation provides comprehensive strategies for improving the reliability of GaN and SiC semiconductor devices and circuits, with a particular focus on ESD protection, latchup prevention, and SOA enhancement. Through in-depth analysis and implementation at the device and circuit levels, this research provides concrete design references for improving the reliability of wide bandgap semiconductor technology.

Keywords — Wide-Bandgap Semiconductor, Integrated Circuit (IC), Gallium Nitride (GaN), Silicon Carbide (SiC), Electrostatic Discharge (ESD), Latchup, Safe Operating Area (SOA).