IEEE CAS Distinguished Lecture in Microelectronics

Language: English

Date and Time: 29 June 2007 14:00 ~ 16:00 p.m.

Venue: Auditorium II, International Library, University of Macau

Topic : Introduction to On-Chip ESD Protection Design in CMOS Integrated Circuits

Speaker: : Prof. Morris (Ming-Dou) Ker, Taiwan National Chiao-Tung University

Abstract: As the increase of applications with more integrated circuits (ICs) products in our life, the reliability of IC products has become one of the most important issues. In the CMOS technology developed into nanometer scale to realize most of VLSI/SoC for electronic systems, the gate-oxide thickness of MOSFET is only 10~15Å for application with sub-1V power supply. Such thinner gate oxide is very easily ruptured by electrostatic discharge (ESD) events, which frequently happen in our environments with the voltage level of hundreds or even thousands volts. The electronics products are typically weaker to sustain such ESD stresses during the assembly, testing, package, and the applications in our life.

To verify the reliability and quality of IC products to ESD robustness for safe applications in our life, there are already some industry ESD standards developed, such as Human Body Model (HBM) and Charged Device Model (CDM), to verify the ESD robustness of IC products. However, how to design the on-chip ESD protection circuits to effectively protect the integrated circuits realized by the nano-scale CMOS devices with very thin gate oxide is a quite difficult challenge. The on-chip ESD protection circuit must be included into the chip design phase, and the ESD robustness must be verified among the IC products those will be used in all electronic systems. In the SoC or giga-scale electronics systems, the power pins to support many circuit blocks in a single chip are often separated into a lot of power domains or groups. With those separated power domains, the interface circuits between the circuit blocks are also often damaged by the ESD stresses zapping on the input, output, or power pins to cause the internal ESD failures beyond the I/O circuits. Such internal ESD damages are quite trouble to be fixed when the electronics systems become more complex or bigger.

In this DLP talk, a brief introduction on ESD issue and standards to IC products is presented with some failure analysis pictures to demonstrate the impact of ESD on IC products. The basic design concept for on-chip ESD protection circuit will be presented. Some state-of-the-art ESD protection techniques, gate-driven design and substrate-triggered design, will be shown with real circuit implementations in I/O circuits of ICs. ESD protection for CMOS ICs is not only the process issue but stronger dependent to the design issue, which has been an important topic that the circuit designers must to watch.

Biography: Ming-Dou Ker received the B.S. degree from the Department of Electronics Engineering and the M.S. and Ph.D. degrees from the Institute of Electronics, National Chiao-Tung University (NCTU), Hsinchu, Taiwan, R.O.C., in 1986, 1988, and 1993, respectively.

He was ever worked as the Department Manager in the VLSI Design Division of the Computer and Communication Research Lab.(CCL), Industrial Technology Research Institute (ITRI), Taiwan. Now, he has been a Full Professor in the Dept. of Electronics Engi., NCTU. He also serves as the Director of Master Degree Program in the College of Electrical Engineering and Computer Science, NCTU; as well as the Associate Executive Director of National Science and Technology Program on SoC, Taiwan. In the field of reliability and quality design for circuits and systems in CMOS technology, he has published over 290 technical papers in international journals and conferences. He has proposed many inventions to improve reliability and quality of integrated circuits, which have granted with 120 U.S. patents and 132 ROC (Taiwan) patents. His current research topics include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, and on-glass circuits for system-on-panel applications in TFT LCD display. Prof. Ker had been invited to teach or to consult reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC Industry.

Dr. Ker has served as member of the TPC and Session Chair of numerous international conferences. He is the Organizer of the Special Session on ESD Protection Design for Nanoelectronics and Gigascale Systems in ISCAS 2005. He taught the Tutorial Course on the topic of ESD Protection Design for Nanoelectronics in CMOS Technology in ISCAS 2006. He was selected as the Distinguished Lecturer in IEEE CAS Society for year 2006-2007. He also served as Associate Editor of IEEE Trans. on VLSI Systems. He was the President of Foundation in Taiwan ESD Association. In 2003, he was selected as one of the Ten Outstanding Young Persons in Taiwan by Junior Chamber International (JCI). In 2005, one of his patents on ESD protection design has been awarded with the National Invention Award in Taiwan.

ALL ARE WELCOME

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CAS/COM Joint-Chapter

DLP Talk in University of Macau

Introduction to On-Chip ESD Protection Design in CMOS Integrated Circuits

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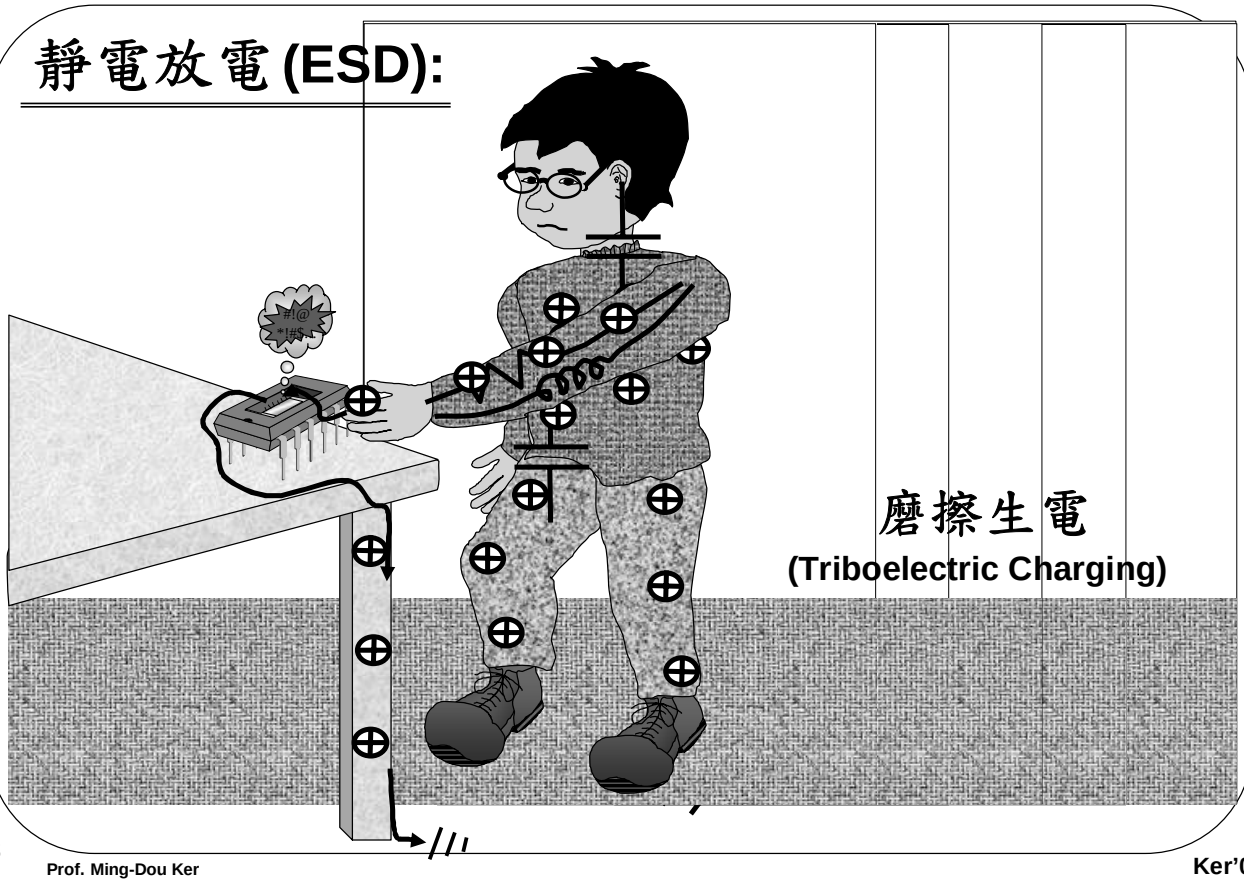
June 29, 2007

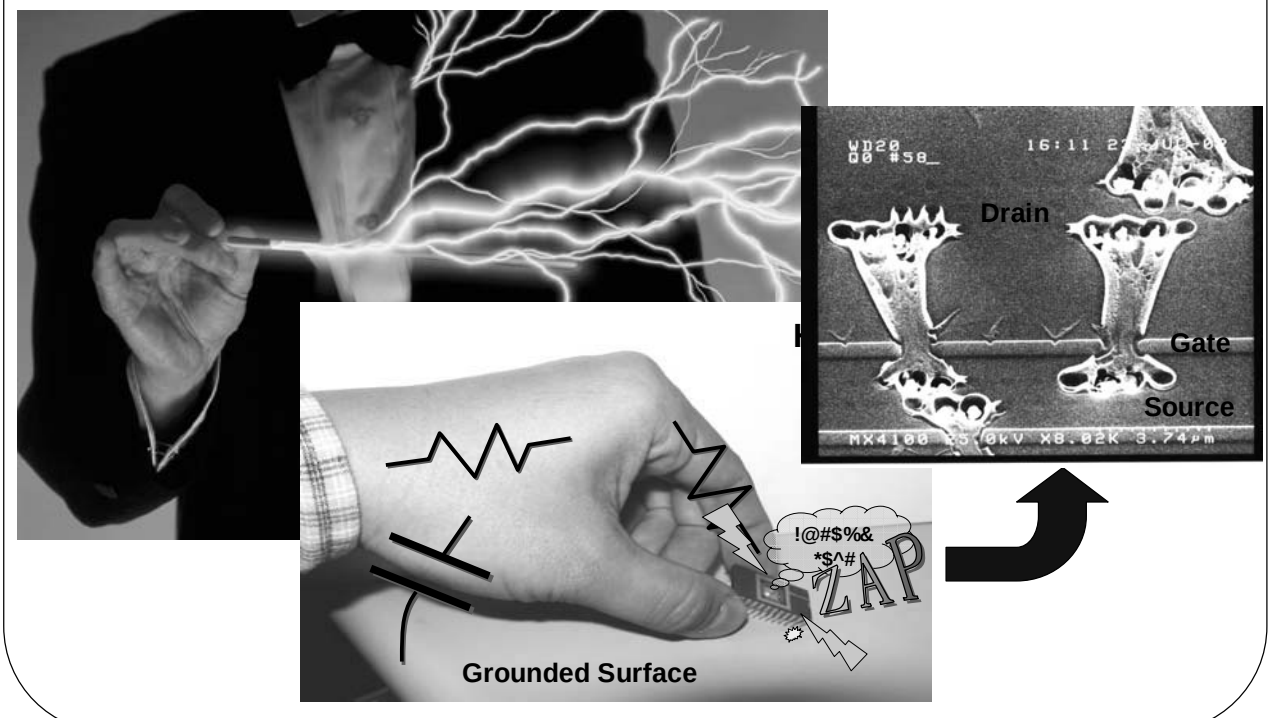
ESD = Electrostatic Discharge

- **The discharge current generated from the static charges often burned out the junction, contact, gate oxide, and even the metal lines in CMOS integrated circuits.**

靜電放電 (ESD):



Is ESD so worse in IC Indutsry ?

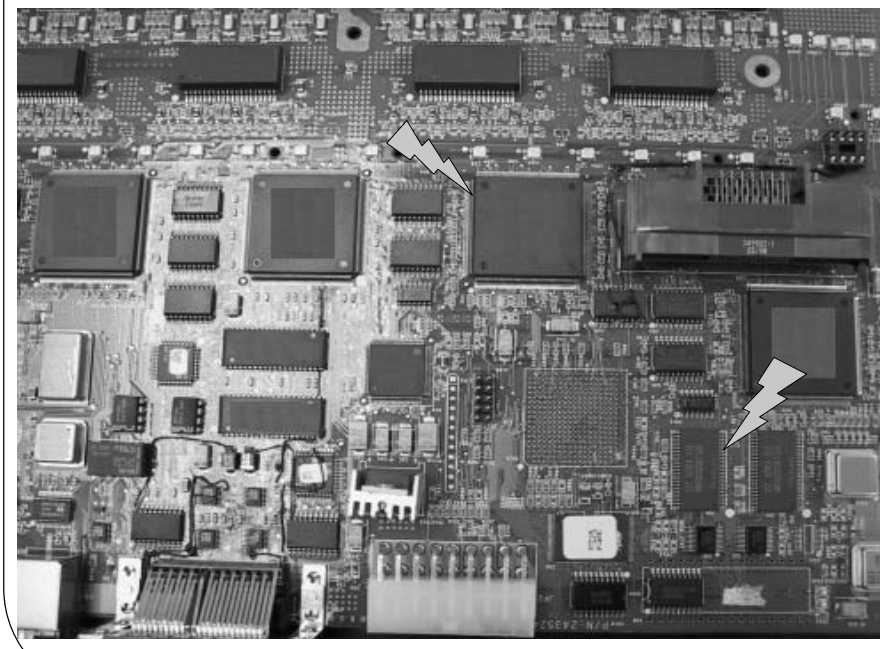


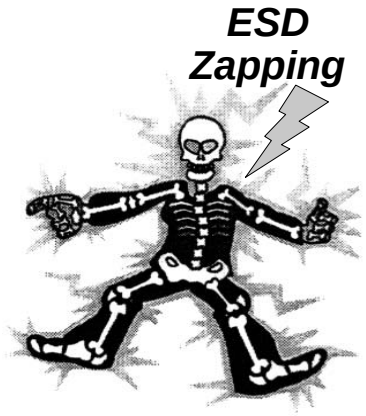
Yes, ESD is even worse than you expected !

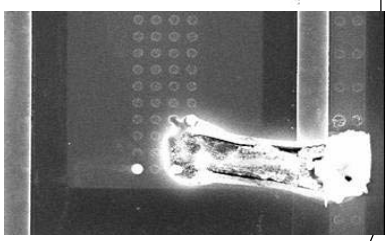
Means of Static Generation	Electrostatic Voltage		
	10% R.H.	40% R.H.	55% R.H.
Person walking across Carpet	35,000 V	15,000 V	7,500 V
Person walking across Vinyl Floor	12,000 V	5,000 V	3,000 V
Worker at a Bench	6,000 V	500 V	400 V
Ceramic DIP in Plastic Tube	2,000 V	700 V	400 V
Ceramic DIP in Vinyl Set-up Trays	11,500 V	4,000 V	2,000 V
IC Packs as Bubble Plastic Cover is removed	26,000 V	20,000 V	7,000 V
IC Packs as Packed in Foam Lined Shipping Box	21,000 V	11,000 V	5,500 V

(R.H.= relative humidity)

ESD Could induce Serious Yield Loss in Microelectroincs

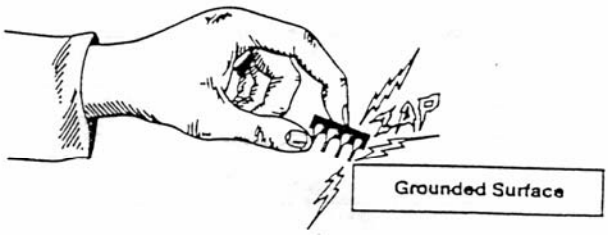


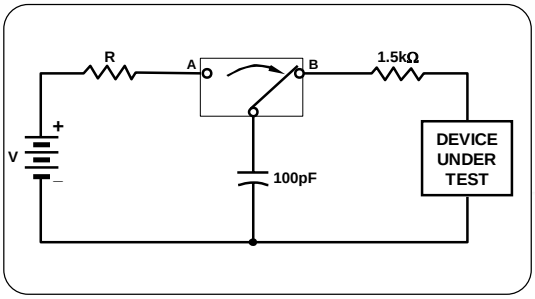




Models of ESD (Electrostatic Discharge) Events

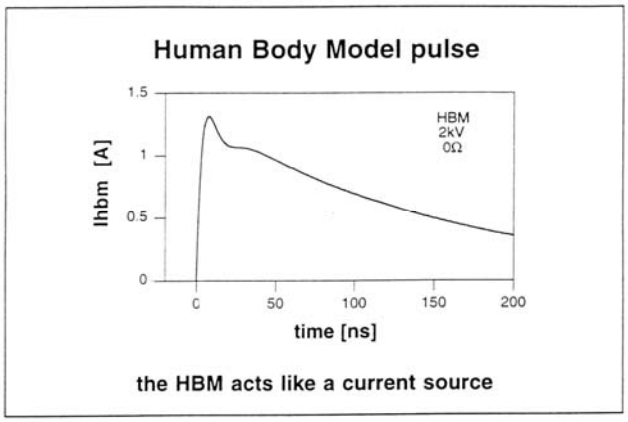
(1). Human Body Model (HBM)





Standards :

1. **MIL-STD-833C Method 3015.7**
2. **EIA/JESD22-A114-A (JEDEC, 1997)**
3. **ESD STM 5.1 (EOS/ESD, 1998)**



C_{HBM}= 100pF; R_{HBM}= 1.5kΩ

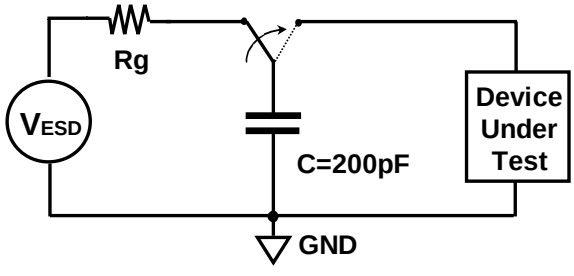
Ipeak = ~ 1.3A (for 2000V HBM)
tr = 2 ~ 10 ns

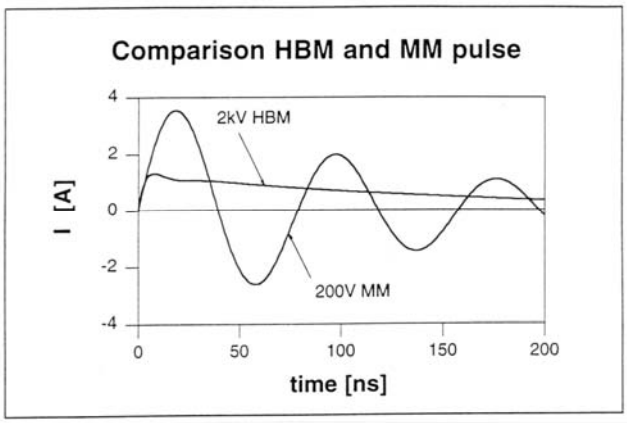
Models of ESD (Electrostatic Discharge) Events

(2). Machine Model (MM)

Standards :

1. **EIAJ-IC-121 Method 20**
2. **EIA/JESD22-A115-A (JEDEC, 1997)**
3. **ESD STM 5.2 (EOS/ESD, 1999)**





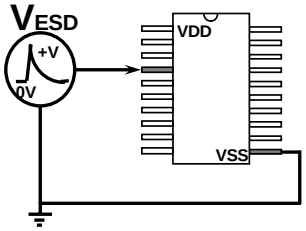
C_{MM}= 200pF
R_{MM}= 0Ω

Ipeak = ~ 3.8A (for 200V MM)
Resonance Freq. = ~ 16 MHz

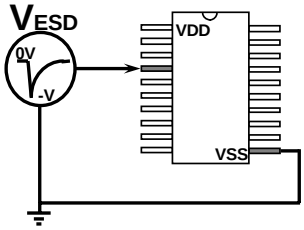
Pin Combination in HBM / MM ESD Testing (I)

- ESD stress on the input or output pins with the VDD or VSS pins relatively grounded :

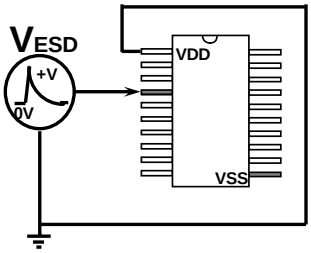
(1) PS-mode



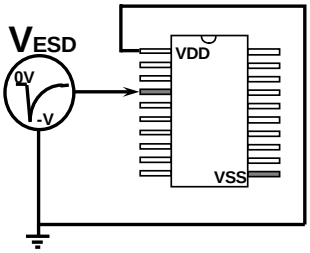
(2) NS-mode



(3) PD-mode



(4) ND-mode



Test Report of a CMOS IC in HBM ESD Testing

- ESD levels of the input / output pins in the PS-, NS-, PD-, and ND-modes ESD stresses :

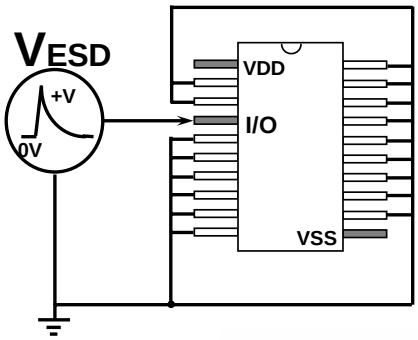
Zapping Mode / Test Pin	VDD(+) PD-Mode	VDD(-) ND-Mode	VSS(+) PS-Mode	VSS(-) NS-Mode
Pin #2	2500	-1000	500	OK
Pin #3	1750	-500	500	OK
Pin #4	7250	OK	7000	OK
Pin #5	4250	-500	4000	-5750
Pin #6	5000	-2500	4500	-3000
Pin #7	3000	OK	4500	-7000
Pin #8	7250	OK	7250	OK
Pin #9	2000	-1000	500	OK
Pin #10	2250	OK	750	OK
Pin #11	6500	-750	500	OK
Pin #12	1500	OK	500	OK

OK: > 8000

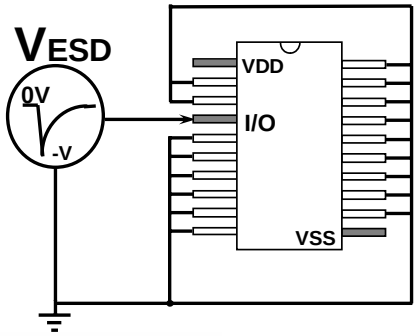
Pin Combination in HBM / MM ESD Testing (II)

- **Pin-to-Pin ESD Stress :**

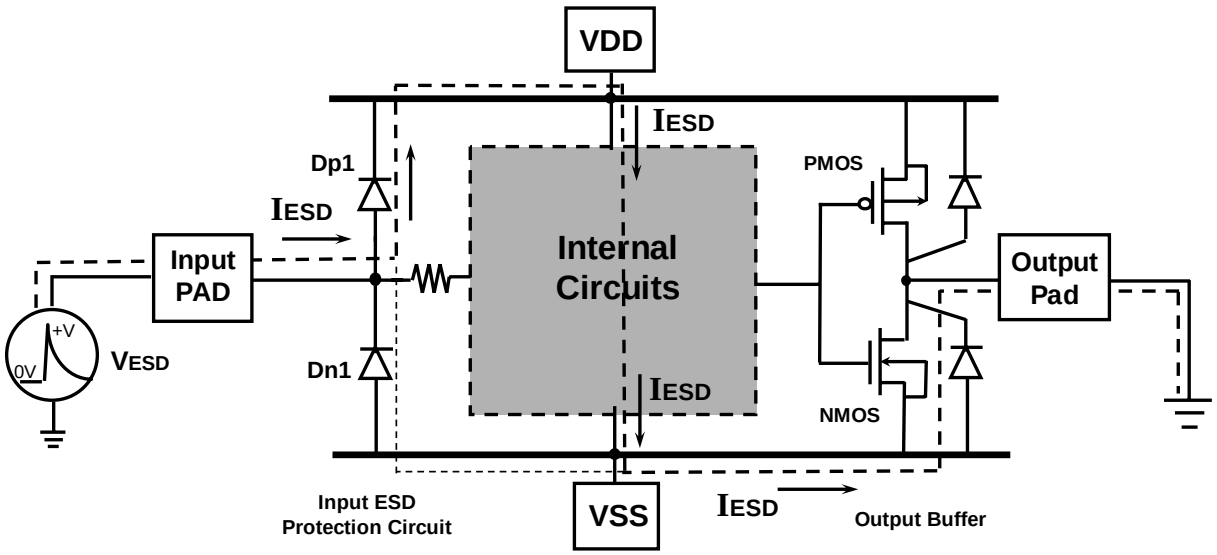
(1) Positive-mode



(2) Negative-mode



Internal ESD Damage Due to Pin-to-Pin ESD Stress



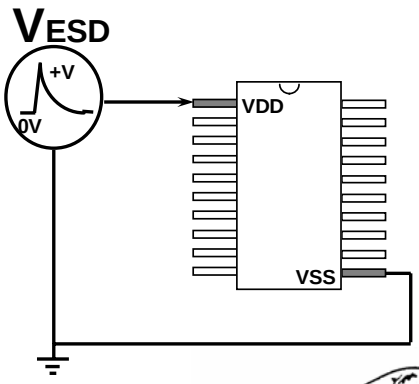
Pin-to-pin ESD stress

➡ **easy to cause ESD damage located at the internal circuits.**

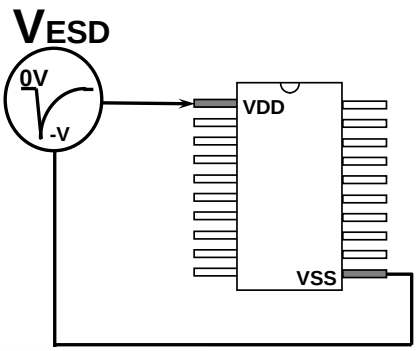
Pin Combination in HBM / MM ESD Testing (III)

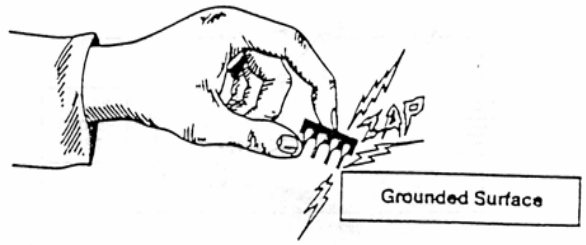
- **VDD-to-VSS ESD Stress :**

(1) Positive-mode

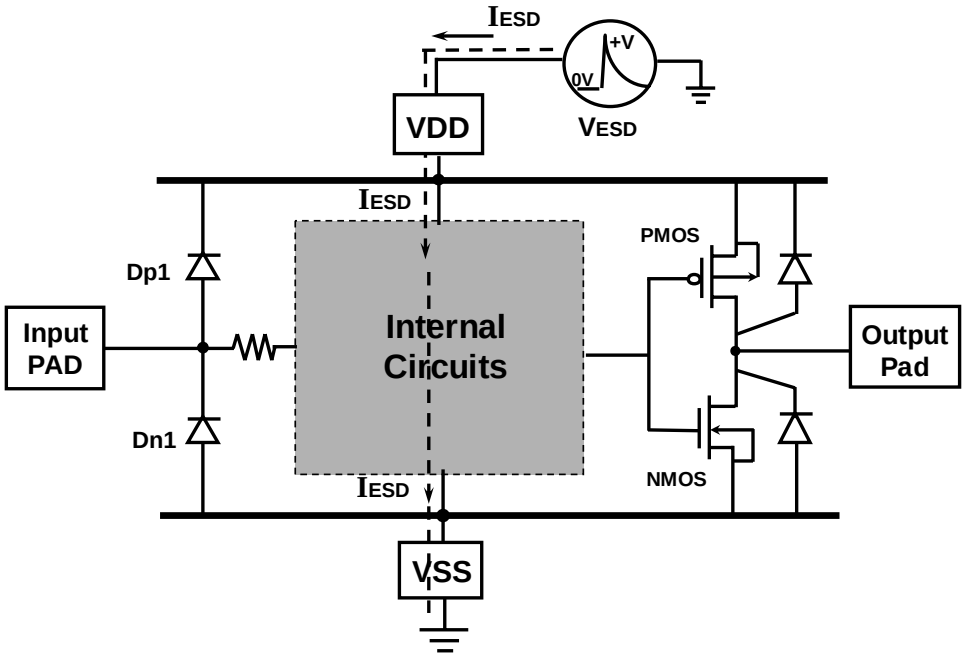


(2) Negative-mode





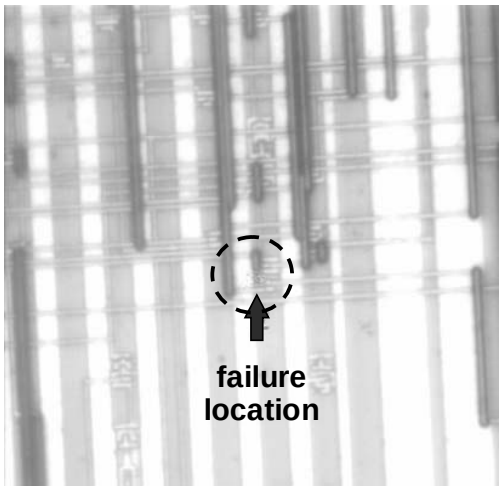
Internal ESD Damage Due to VDD-to-VSS ESD Stress

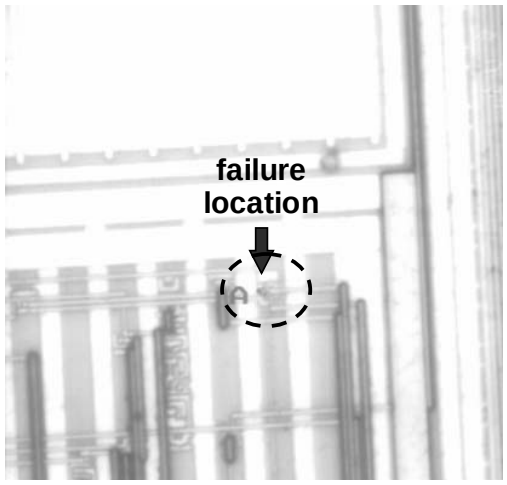


The internal circuits are more vulnerable to ESD damage in this VDD-to-VSS ESD-stress condition.

Failure Analysis (EMMI) -- Internal Damage

Examples of internal failure after HBM ESD stress

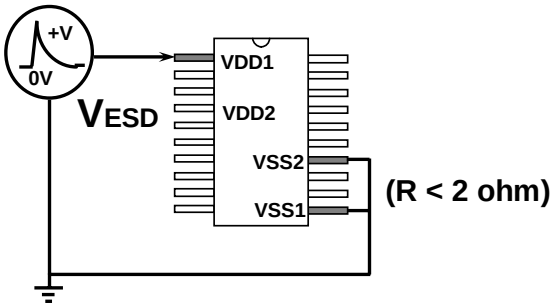




Pin Combination in HBM / MM ESD Testing (IV)

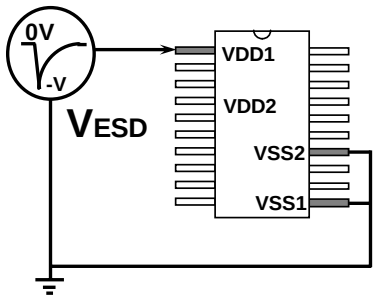
- **VDD-to-VSS ESD Stress for the IC having multiple power pins :**

(1) VDD1 to all VSS pin (+ Zapping)

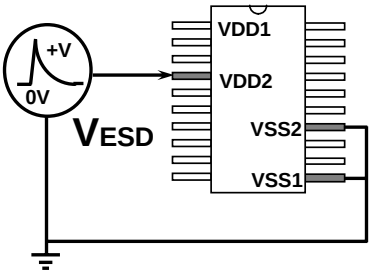


(R < 2 ohm)

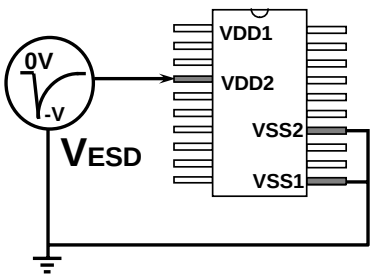
(3) VDD1 to all VSS pin (- Zapping)



(2) VDD2 to all VSS pin (+ Zapping)



(4) VDD2 to all VSS pin (- Zapping)



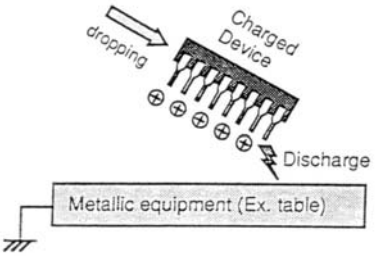
Models of ESD (Electrostatic Discharge) Events

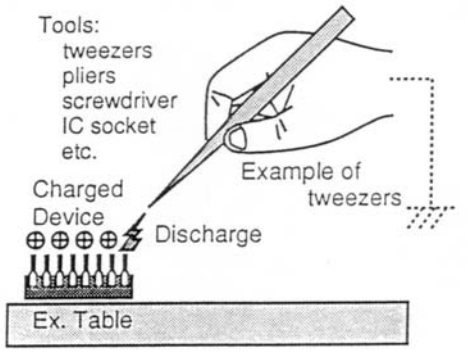
(3). Charged Device Model (CDM)

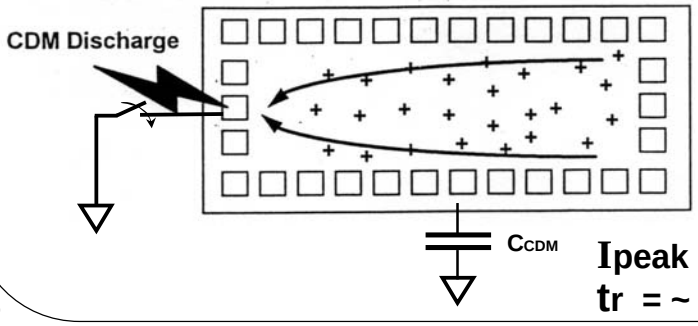
Standards :

1. JESD22-C101 (JEDEC, 1997)

2. ESD STM 5.3 (EOS/ESD, 1999)







$$Q = C \times V$$

$$i = dQ/dt$$

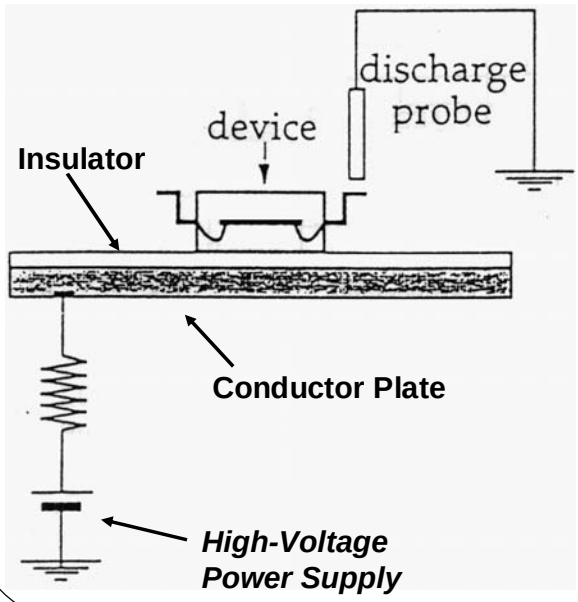
Ipeak = ~ 15A (for 1000V CDM @ 4pF)

tr = ~ 200 ps

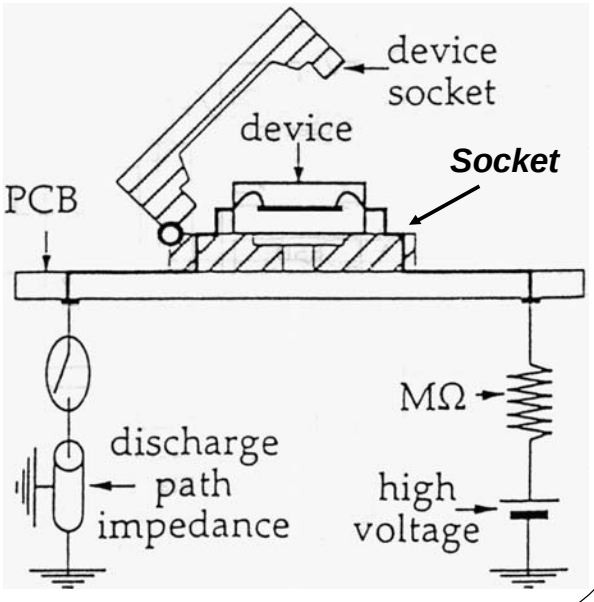
Available CDM ESD Tester

- **Two types of CDM testers with or without Socket :**

Non-Socketed (ns-) CDM

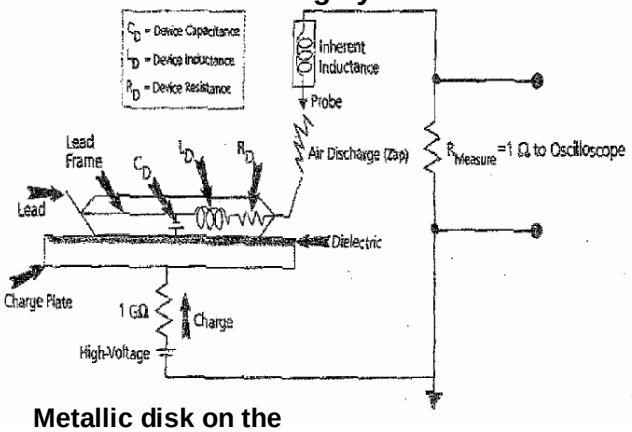


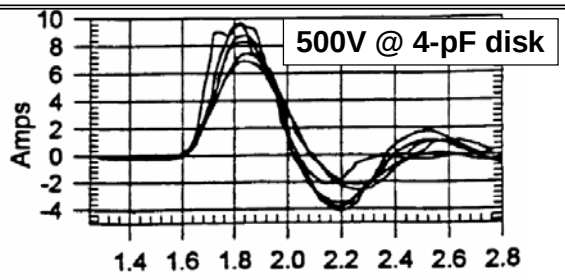
Socketed (s-) CDM

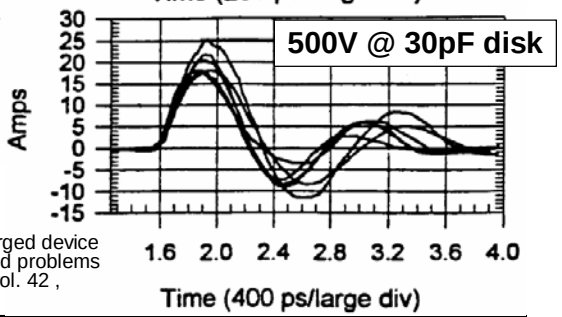


Measured Current Waveform of CDM ESD Event

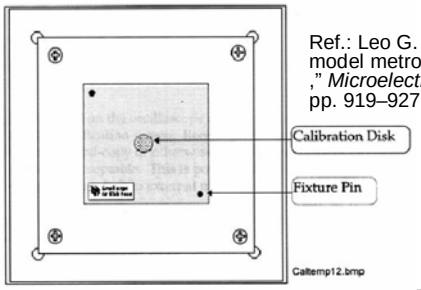
CDM ESD measuring system







Metallic disk on the PCB FR-4 dielectric



Ref.: Leo G. Henry *et al*., "Charged device model metrology: limitations and problems ," *Microelectronics Reliability*, vol. 42 , pp. 919–927, 2002.

Capacitance (pF)	Voltage	I_p for six test heads (A)
4	500	6.0–10.0
4	1000	11–19.0
30	500	17–25

CDM ESD by Field Induction

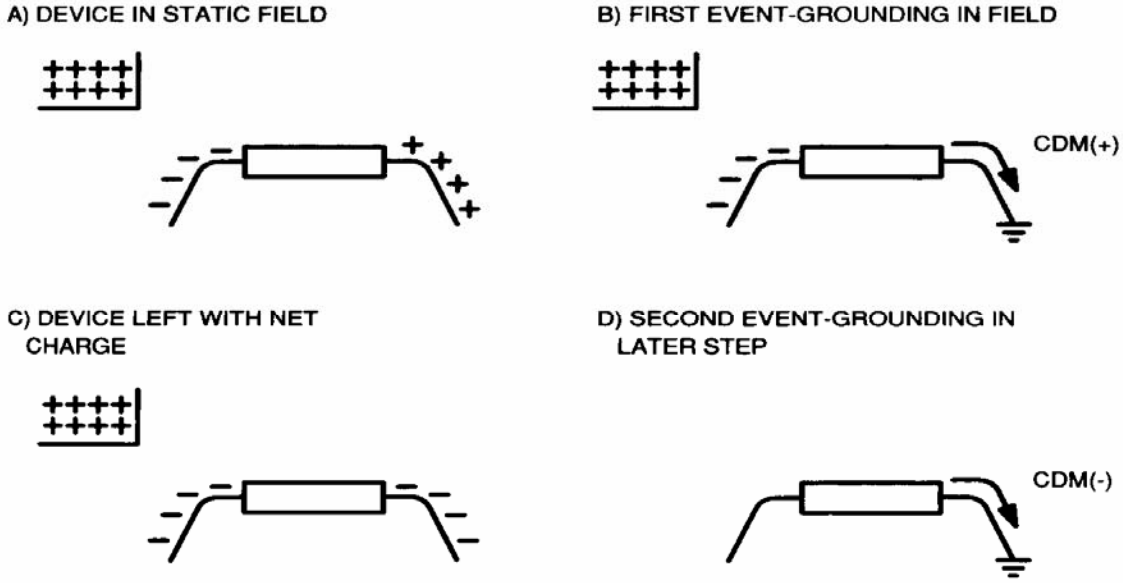
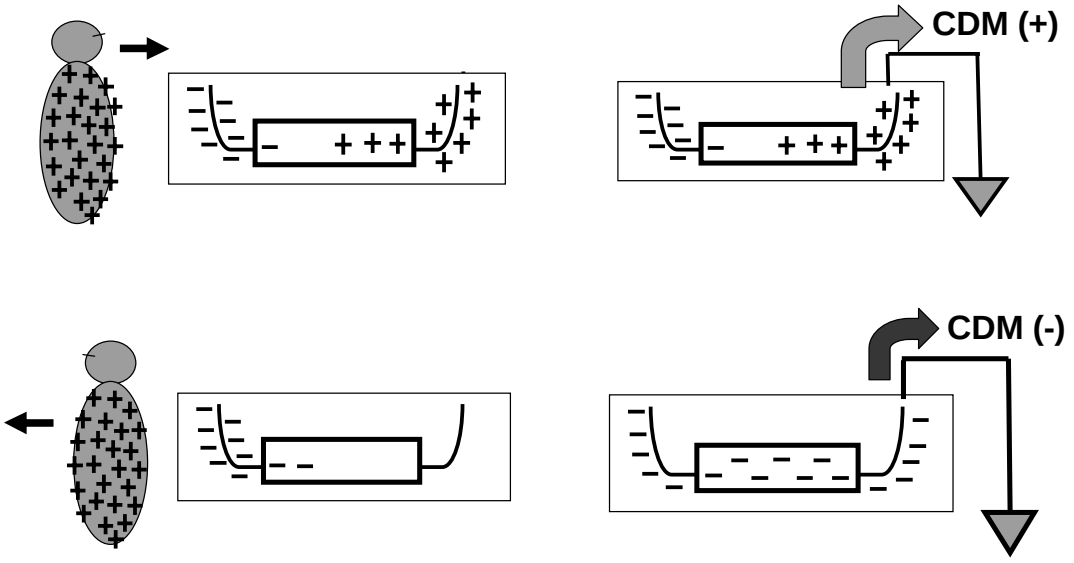


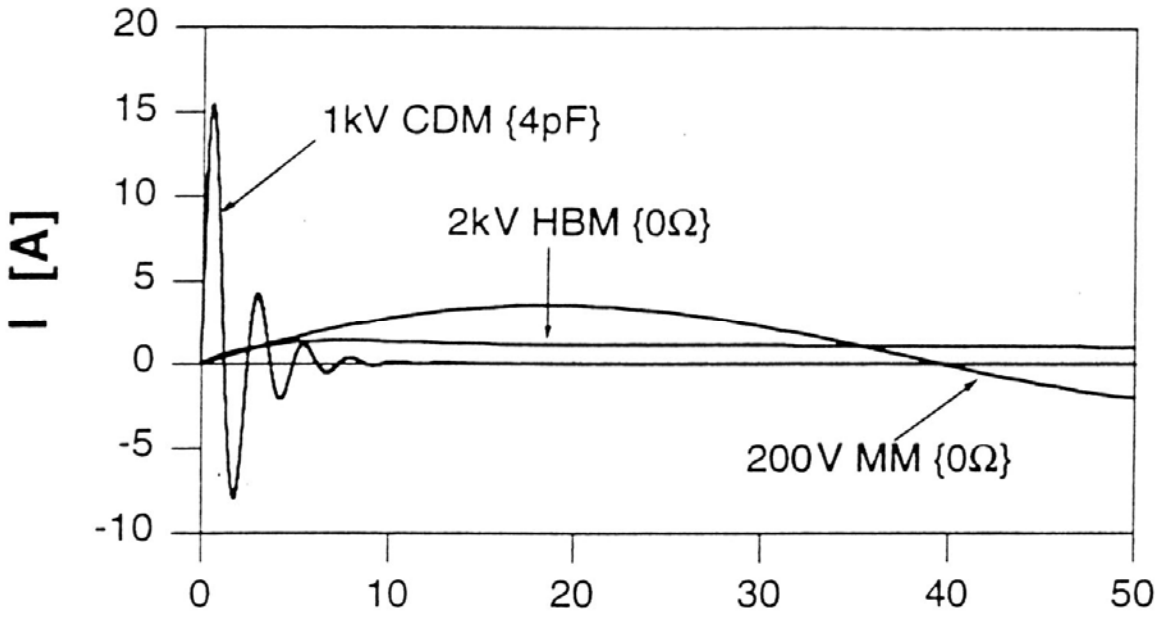
Figure 3-10. ESD by induction

Field-Induced CDM ESD Events



CDM ESD event by field induction !!

Comparisons among the ESD Models



ESD Events During Package Assembly

Step of PLCC trim-and-form :

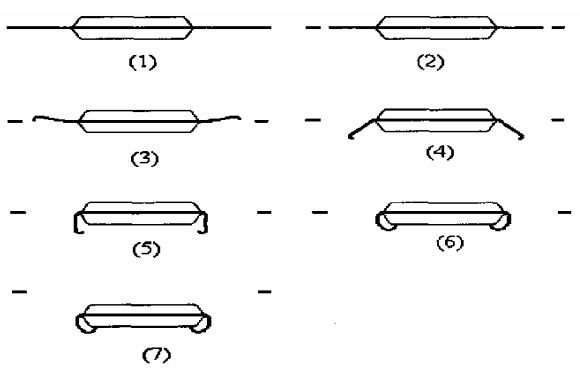


Figure 11: PLCC Lead Forming Steps.

ESD event :

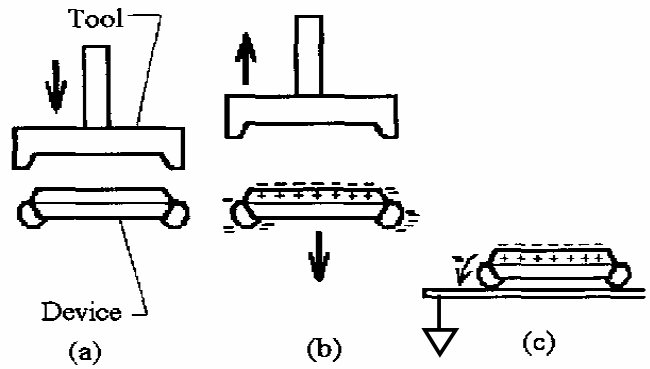
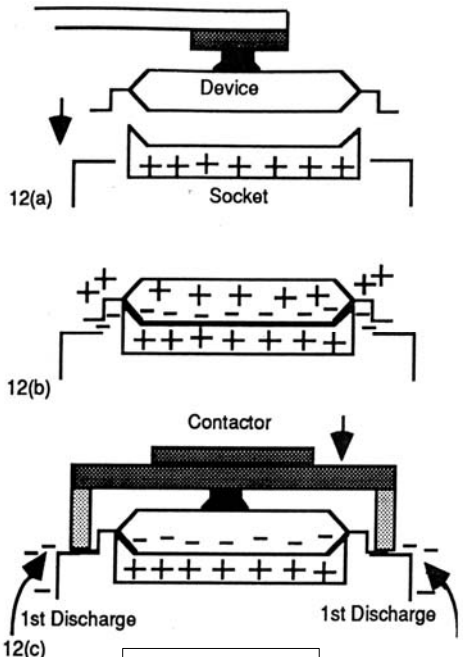


Figure 12: CDM event at trim-and-form.

Ref.: W. Tan, "Minimizing ESD hazards in IC test handlers and automatic trim/form machines," *Proc. of EOS/ESD Symp.*, 1993, pp. 57-64.

ESD Events During IC Function Testing



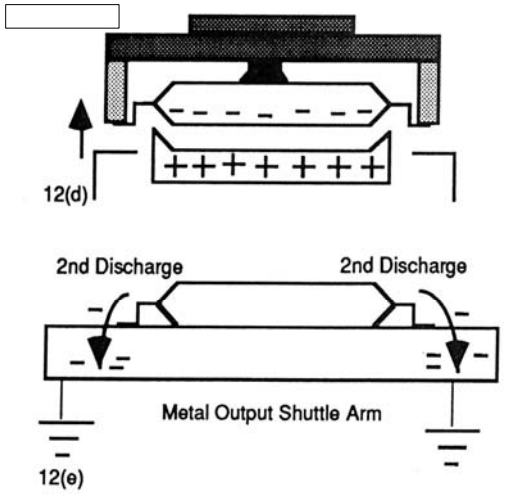


Figure 12. Field Induced CDM ESD event due to tester socket charging.

Ref.: H. Sur, C. Jiang, and D. Josephs, "Identification of charged device ESD induced IC parameter degradation due to tester socket charging," *Proc. of Int. Symp. for Testing and Failure Analysis*, 1994, pp. 219-227.

ESD Events During the IC Back-End Process

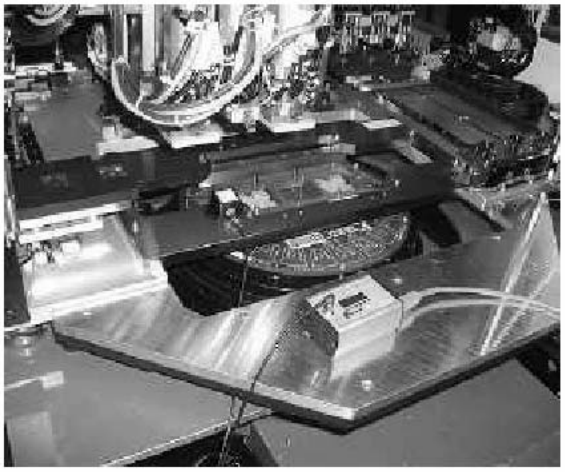
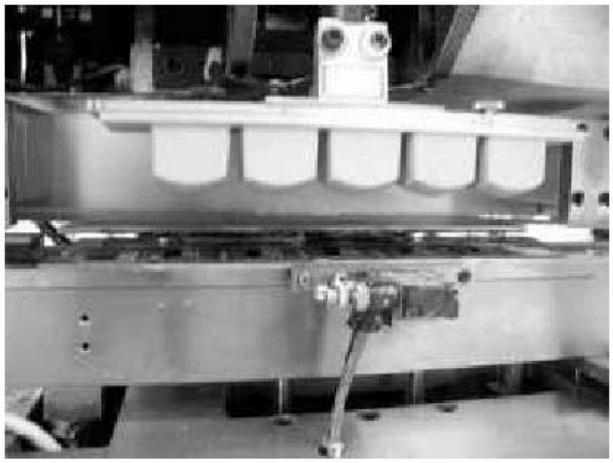


Figure 4 shows experimental data collected at the test pad. As seen from the chart, observed ESD Events were as strong as 400V CDM.

Ref.: J. Marley, D. Tan, and V. Kraz, "Controlling ESD damage of ICs at various steps of back-end process," *Proc. of EOS/ESD Symp.*, 2001, pp. 120-124.

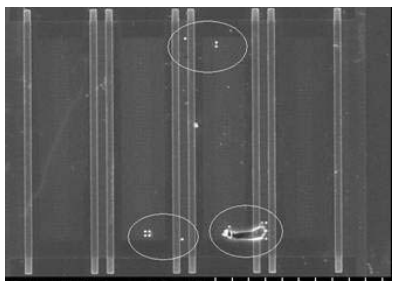
The IC marking process is capable of generating substantial ESD Events. A typical marker is shown in Figure 7.

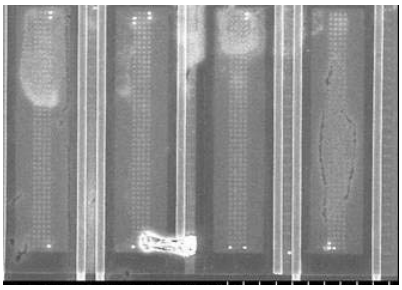


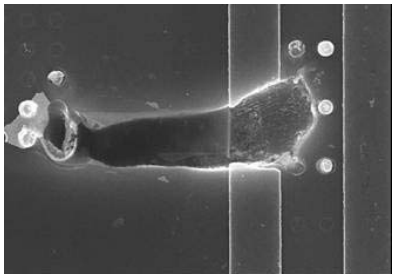
Discharge strength can reach as high as equivalent of 500V CDM but often is kept at approximately 120V CDM level.

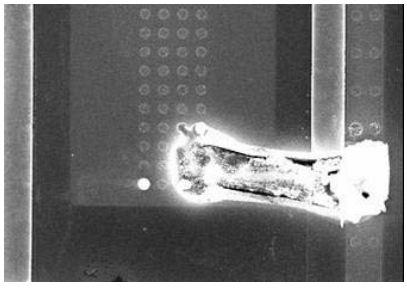
HBM ESD Failure on the Output Buffer

- **Failure after 2-kV HBM ESD stress on output buffer in a 0.5-μm CMOS process**







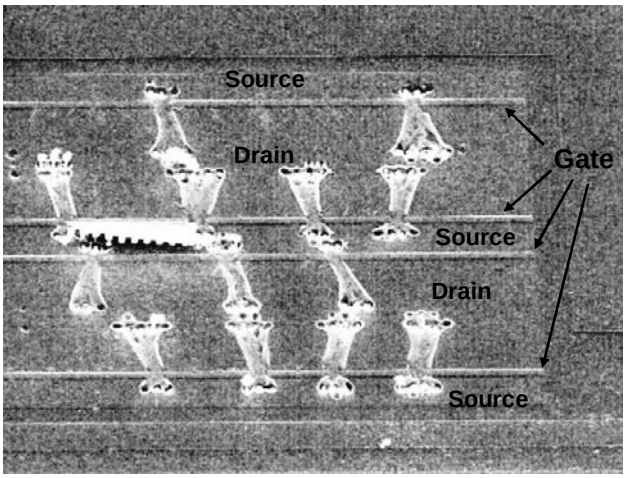


Serious Contact spiking !!

Ref.: M.-D. Ker, *IPFA 2005.*

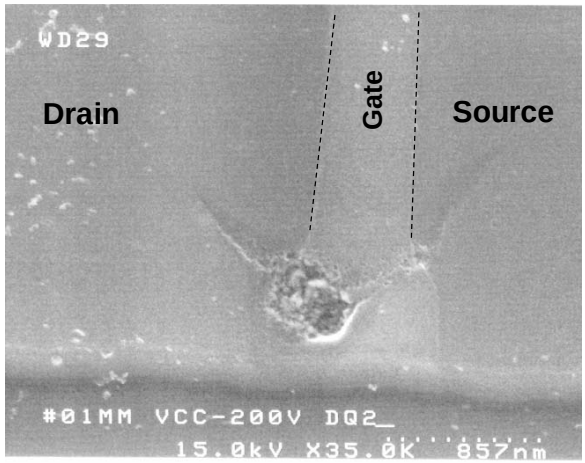
Pictures of HBM / MM ESD Failures on I/O Devices

HBM Failure
after HBM 3kV Zapping



Output PMOS in a 0.25-μm CMOS Process
Each finger PMOS : W/L= 50/0.5 (μm/μm)

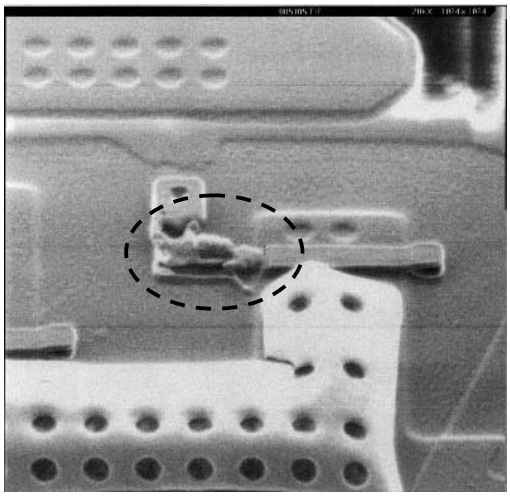
MM Failure
after MM 200V Zapping



NMOS in a 0.18-μm CMOS Process

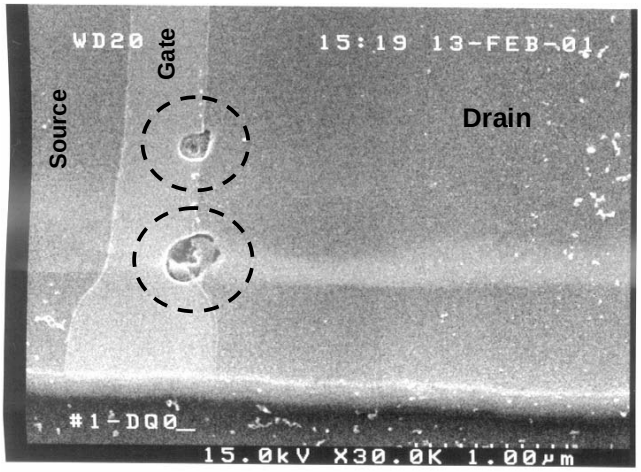
Pictures of CDM Failures on CMOS IC

CDM Failure Located
on the First Input Stage



after field return
(0.5-μm CMOS Process)

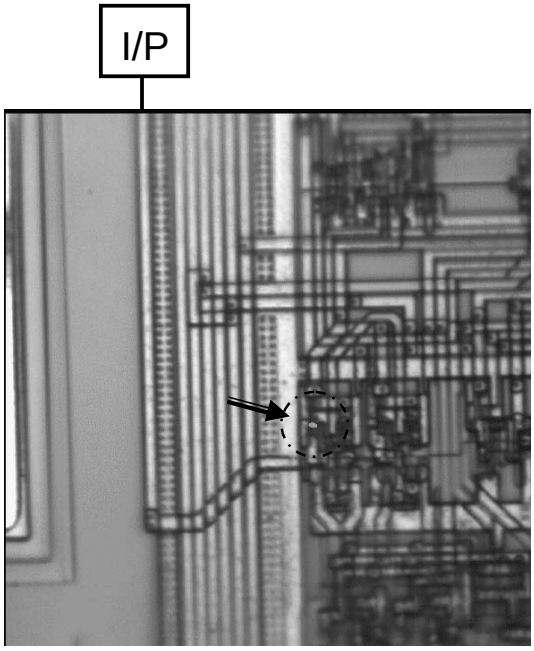
CDM Failure Located
on the output NMOS

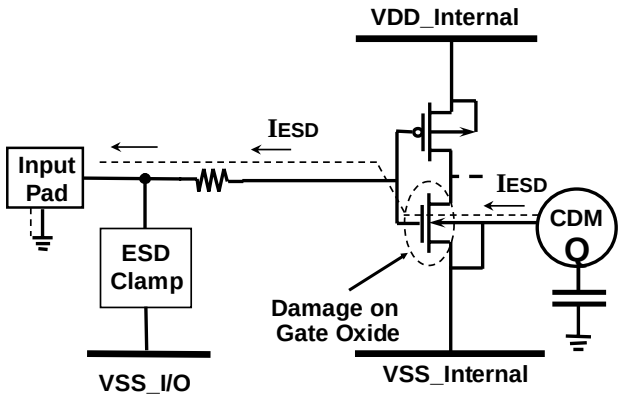


after CDM 500V Zapping
(0.18-μm CMOS Process)

EMMI Pictures of CDM Failure on IC Product #1

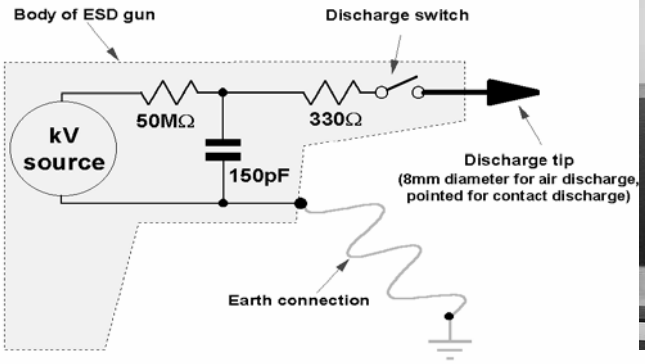
(0.8-μm CMOS process)

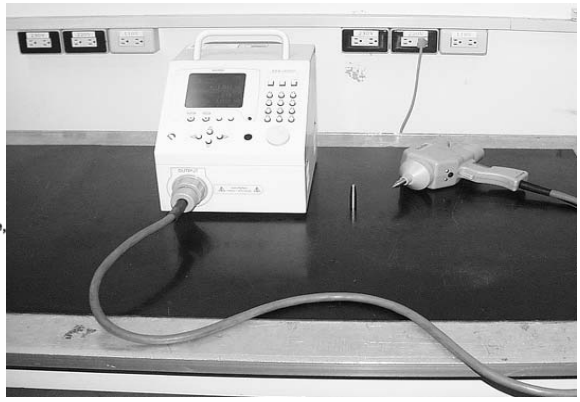




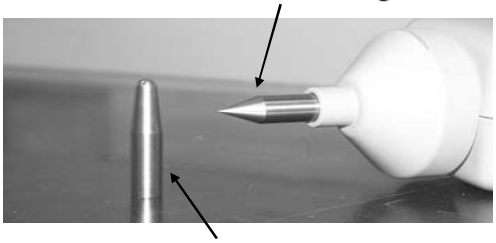
System-Level ESD Gun (IEC/EN 61000-4-2)

Basic circuit of ESD 'gun' for personnel ESD testing to EN 61000-4-2





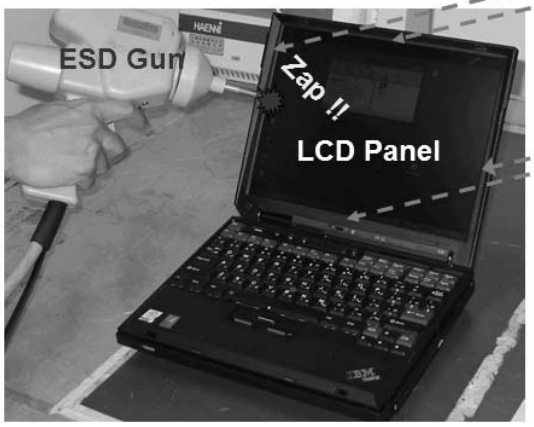
Contact discharge head

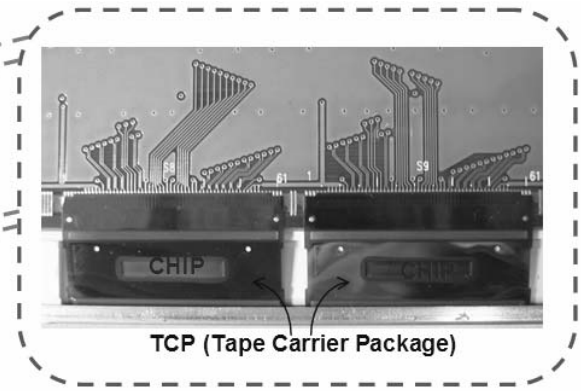


Air discharge head

System-Level EMC/ESD Test on LCD Panel of Notebook by An ESD Gun

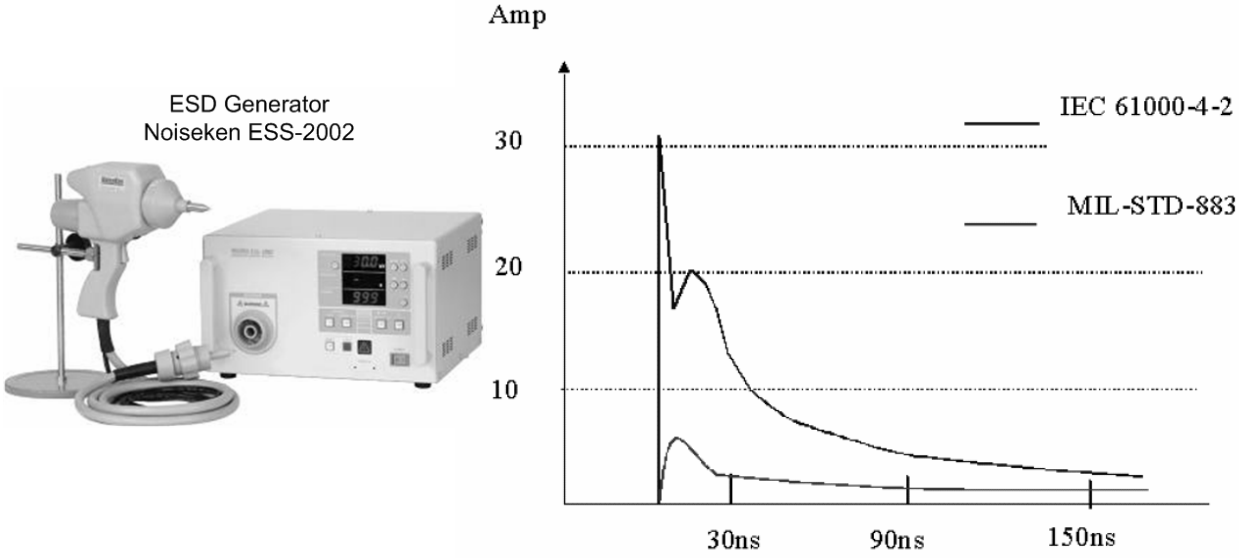
System-Level EMC/ESD Test
(Standard IEC 61000-4-2)





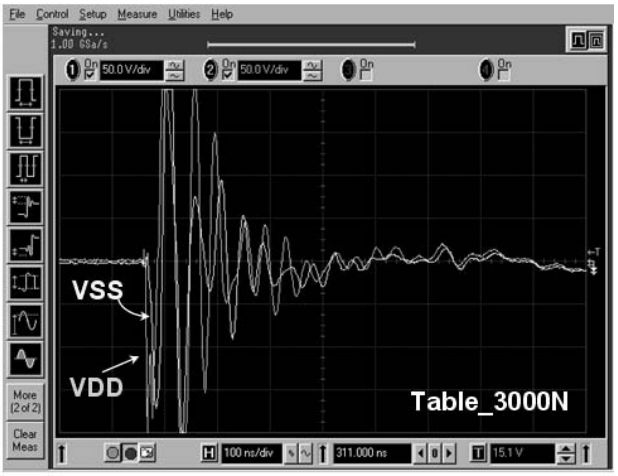
IEC 61000-4-2 : Electromagnetic Compatibility (EMC)
Part 4 : Testing and measurement techniques –
Session 2: Electrostatic discharge immunity Test .

Comparison between System-Level and Component-Level ESD Tests



➡ **Under 8 kV ESD zapping, the peak current in system-level ESD is about 5 times larger than that in component-level ESD.**

System-Level ESD Zapping on the Table to Cause the Keyboard Upset

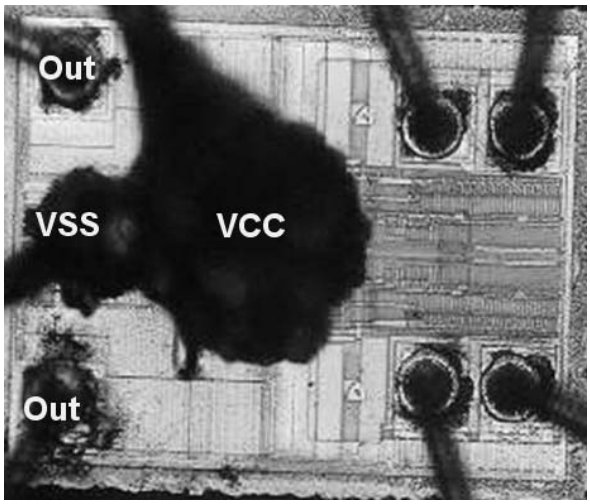


MiniZap
ESD Simulator

Contact-Discharge Test zapping on the Table.

Transient-Induced Latchup due to System-Level ESD Zapping

Output P-N Spacing	Air-Discharge ESD Zapping
~20 μm	pass 12kV, failed at 15kV
~150μm	pass 20 kV



ESD Specifications

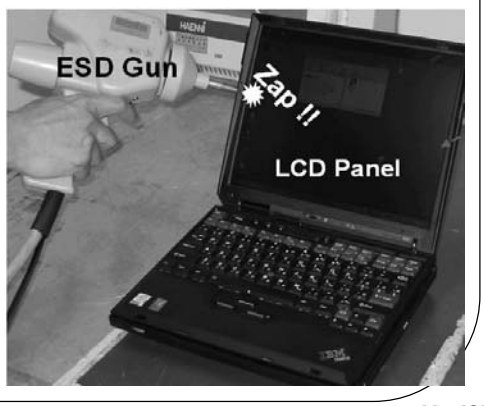
Chip-Level ESD:

	HBM	MM	CDM
Okay	+/- 2kV	+/- 200V	+/- 1kV
Safe	+/- 4kV	+/- 400V	+/- 1.5kV
Super	+/- 10kV	+/- 1kV	+/- 2kV

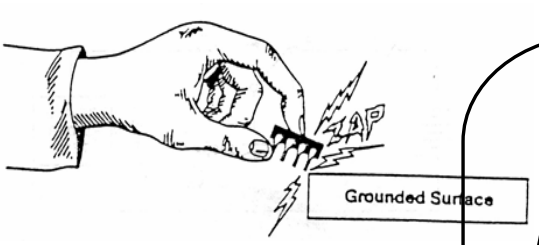
⬅ basic request

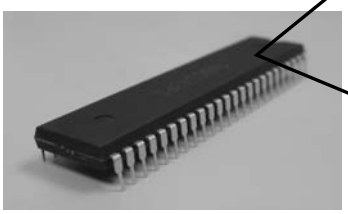
System-Level ESD: (IEC 61000-4-2)

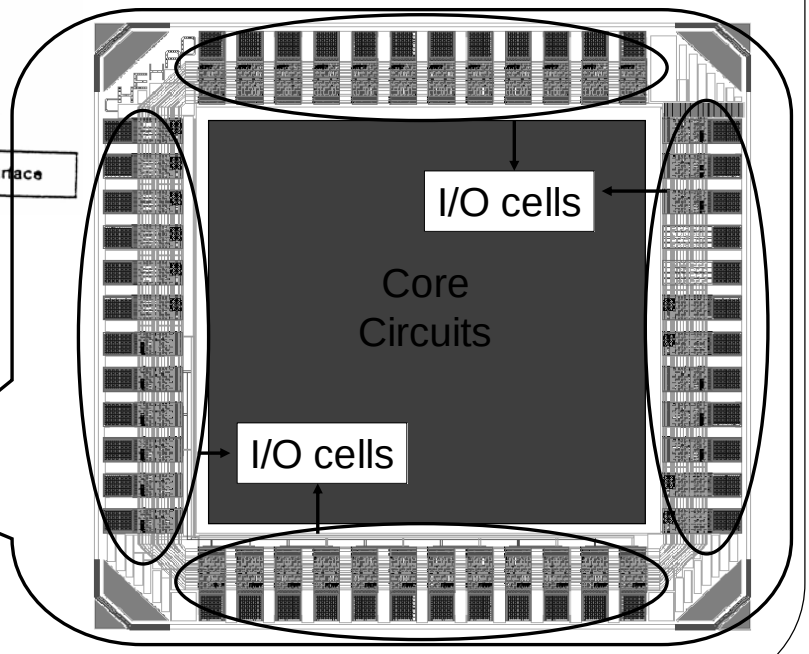
Level	Contact Discharge	Air Discharge
1	+/- 2 kV	+/- 2 kV
2	+/- 4 kV	+/- 4 kV
3	+/- 6 kV	+/- 8 kV
4	+/- 8 kV	+/- 15 kV



I/O Cell Library with ESD Protection Design

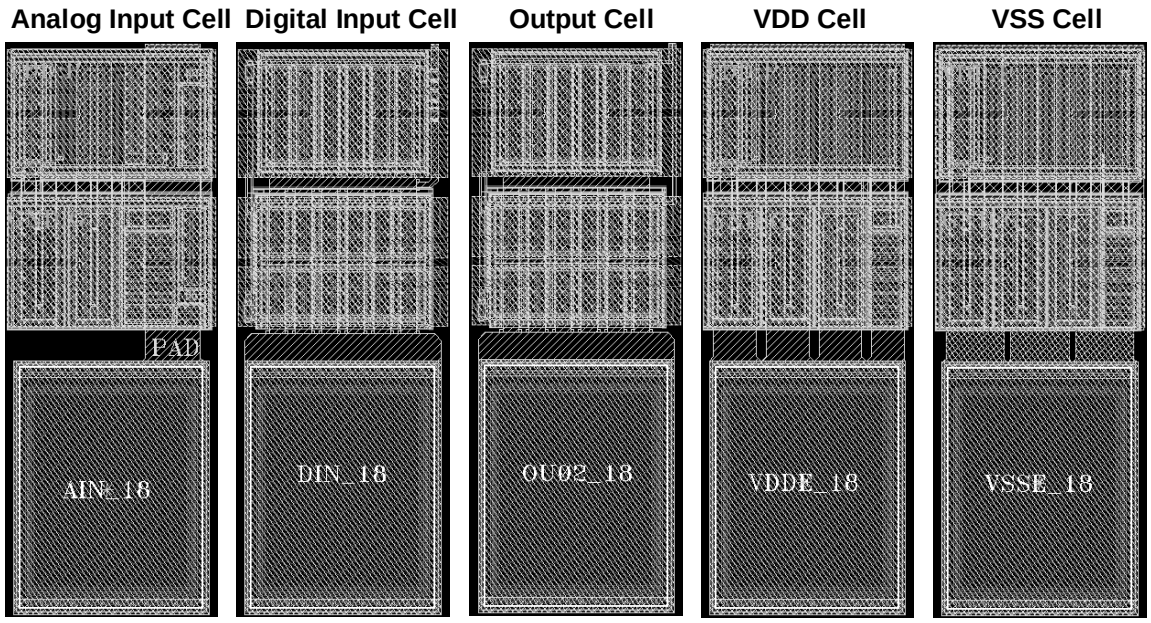




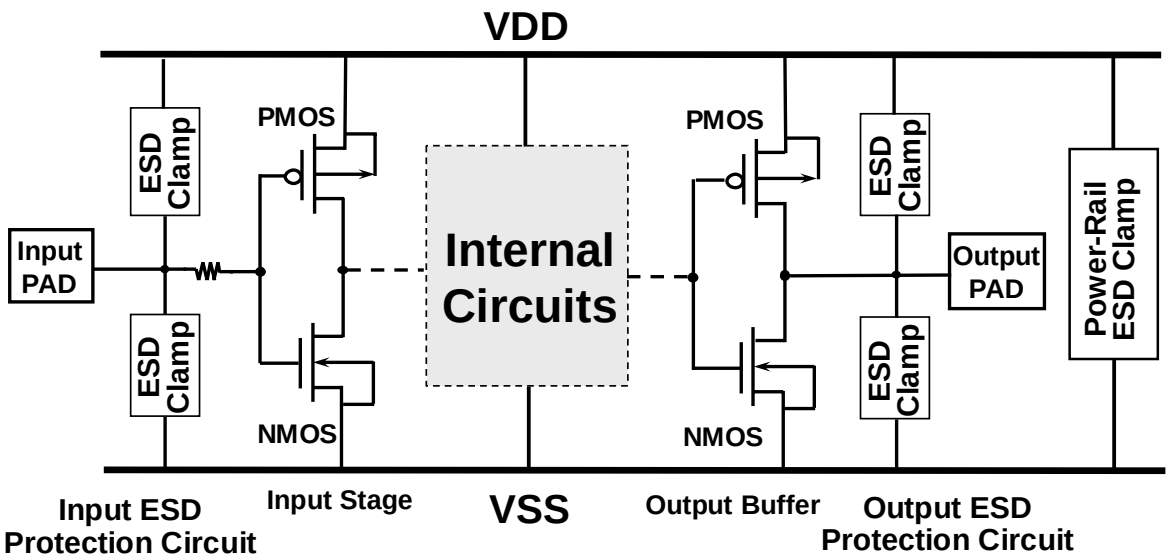


Examples of I/O Cells in 0.18-μm CMOS Process

Applicable to IC products fabricated in a 0.18-μm CMOS process (e.g. digital IC, analog IC, mixed-mode IC, …)



Design Concept of On-Chip ESD Protection



Devices in CMOS Technology for Using in the On-Chip ESD Protection Circuits

(1). Resistor (diffusion, well, poly resistors);

(2). Diode (p-n junction);

(3). Thin-oxide (Gate-oxide) NMOS/PMOS;

(4). Thick-oxide (Field-oxide) devices;

(5). Parasitic vertical / lateral bipolar junction transistor;

(6). Parasitic SCR device (p-n-p-n structure);

(7). Capacitor / Inductor.

Advanced On-Chip ESD Protection Solutions

(1). ESD-Implantation Mask or Silicide-Blocking Mask (Process);

(2). Low-Voltage-Triggered SCR (Device);

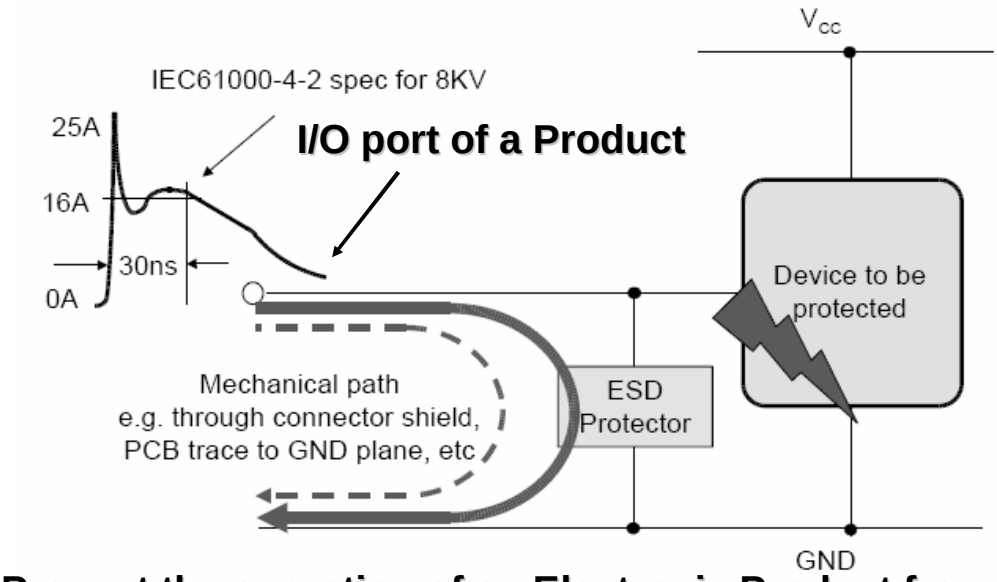
(3). Layout Style (Layout);

(4). Gate-Driven Technique (Circuit);

(5). Substrate-Triggered Technique (Circuit);

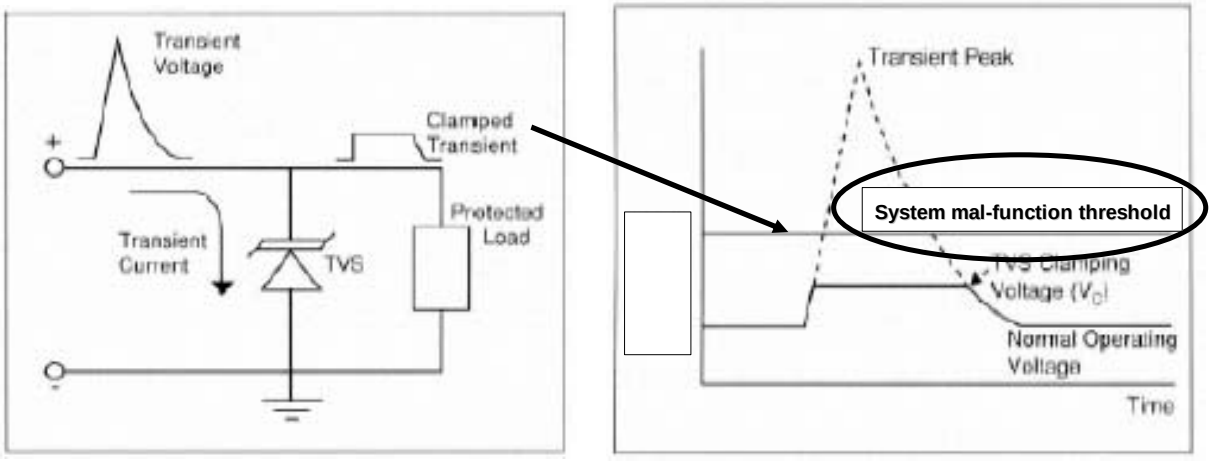
(6). ESD Buses (Scheme).

System-Level (Board-Level) ESD Protection



- **Prevent the operation of an Electronic Product from the disturbance of ESD event. → Bypass the ESD current and *Clamp the voltage at a low value.***

Protection by Transient Voltage Suppressors (TVS)

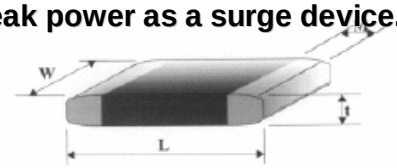


Prevent System from Malfunction!

TVS's Clamping Voltage is the most important parameter.

Types of ESD Protection devices

- Transient Voltage Suppressors (TVS)
  - Varistors
  - Zener diodes
  - Diodes
- The main function of TVS is to absorb high peak power as a surge device.
- It also can be an ESD protector.

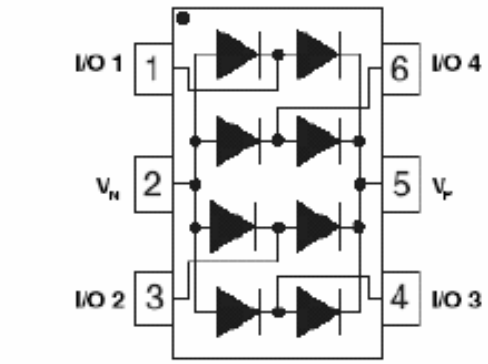


- Advantages
  Single channel, 2 terminals, easy to use.
  Cheap.
- Disadvantages
  C load is big, not suitable for high speed application

Size	0402	0603	0805	1206	1210	3225
L(mm)	1.0 ± 0.10	1.6 ± 0.15	2.0 ± 0.2	3.2 ± 0.3	3.2 ± 0.3	8.0 ± 0.5
W(mm)	0.5 ± 0.10	0.8 ± 0.15	1.25 ± 0.2	1.6 ± 0.3	2.5 ± 0.3	6.3 ± 0.5
M(mm)	0.25 ± 0.15	0.35 ± 0.15	0.4 ± 0.2	0.5 ± 0.25	0.5 ± 0.25	0.5 ± 0.25

Types of ESD Protection devices *(cont'd)*

- Integrated ESD protection array
  - Zener diode array
  - Regular Diodes array
  - Special designed array

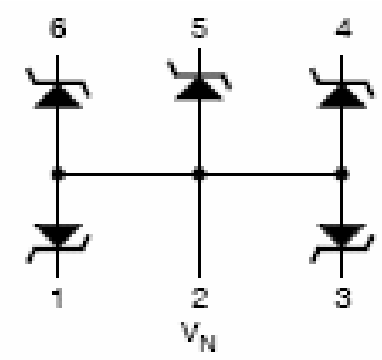


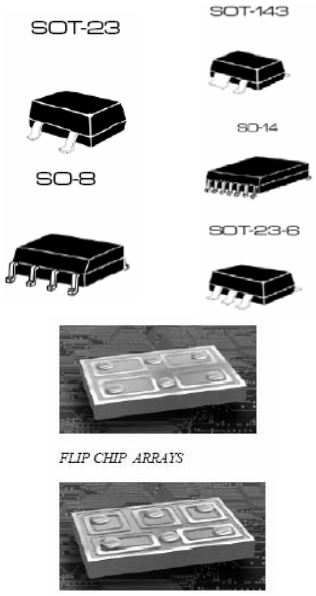
Steering diode array

- Advantages
  Multiple channels.
  Small size.
  C load could be low, suitable for high speed applications.
- Disadvantages
  Cost is a little of higher than TVS.
  Board has to be pre-designed for use.

TVS Diodes Array

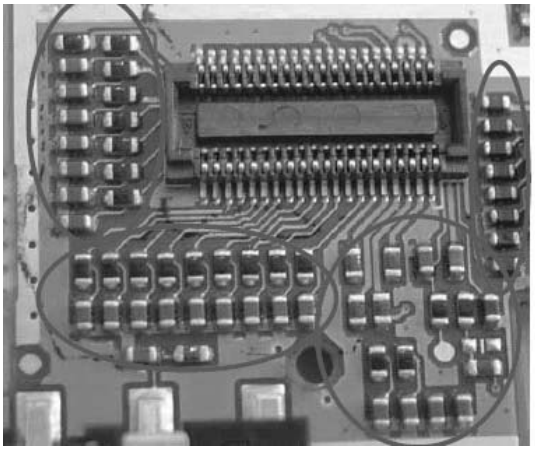
TVS Diodes Array is an integrated multi-channels ESD protection device



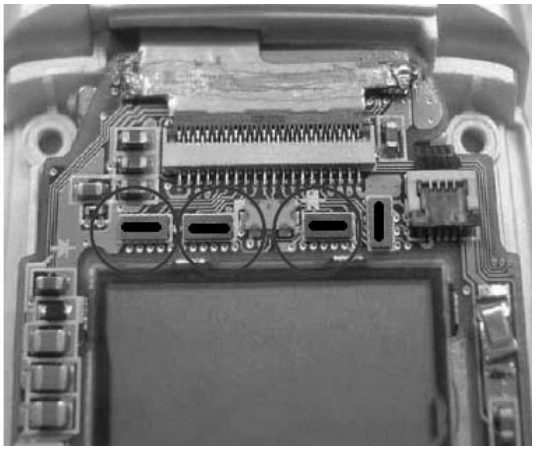


- **Advantages**
  Multiple channels.
  Let System size be small.
  C load could be low, suitable for high speed applications.

Application Examples of TVS Diodes Array



Varistor

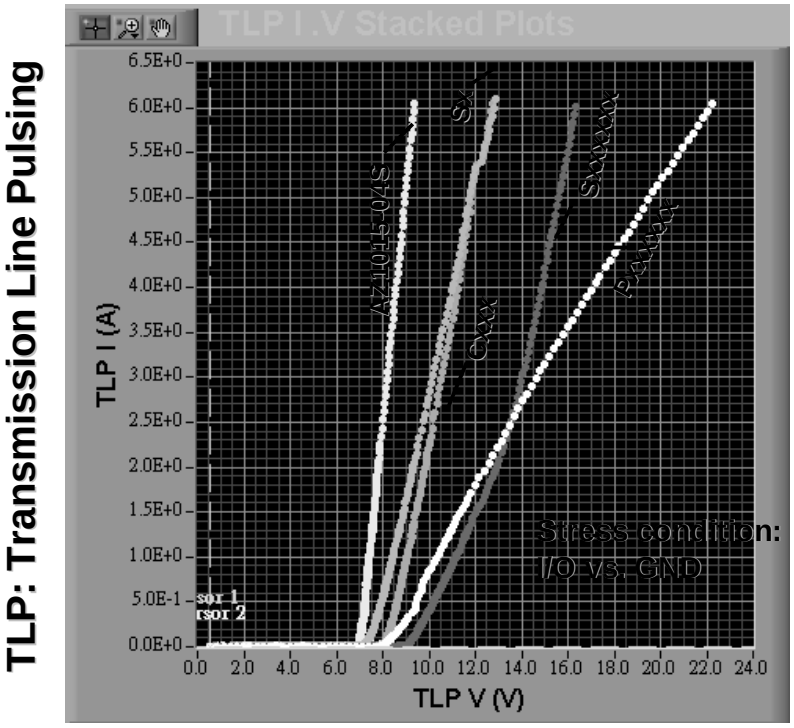


TVS Arrays

The Main Concerned Parameters of ESD Protection Devices

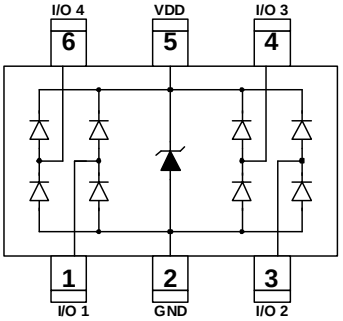
- **Cost (as low as possible)**
- **Package (as small as possible)**
- **ESD Level (as high as possible)**
- **C load (as low as possible, can not affect the normal function of system)**
- **Turn on Voltage (as low as possible, but should be > VDD)**
- **Clamping Voltage (as low as possible, but should be > VDD)**
- **Leakage Current (as low as possible)**

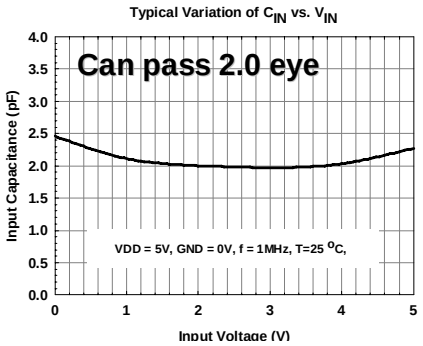
Clamping Voltage Comparison by TLP Measurement

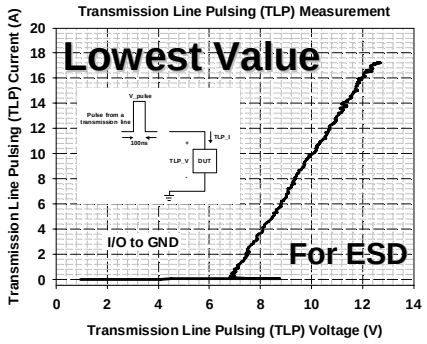


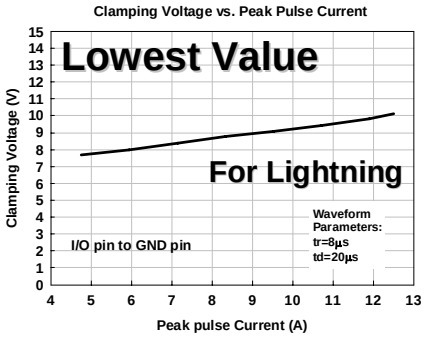
Help USB ports to pass System-Level 8kV contact Mode

AZ1015-04S
(SOT23-6L)



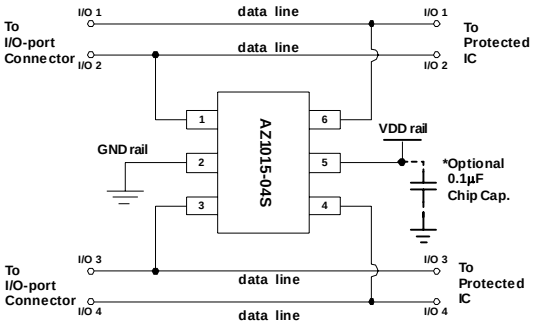




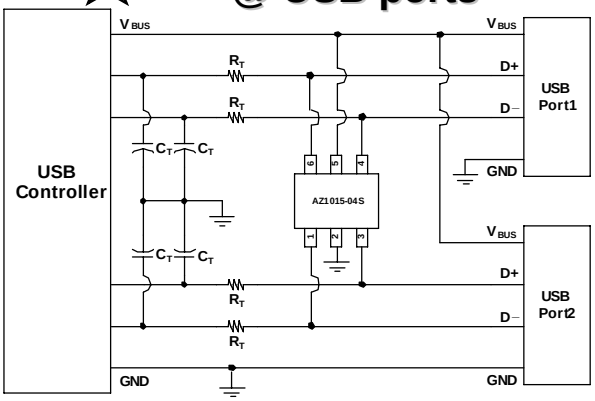


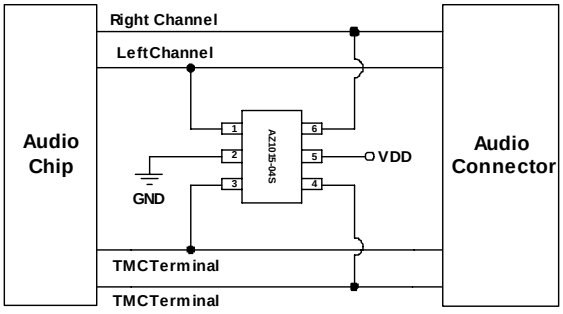
Applications of AZ1015-04S

@ I/O ports

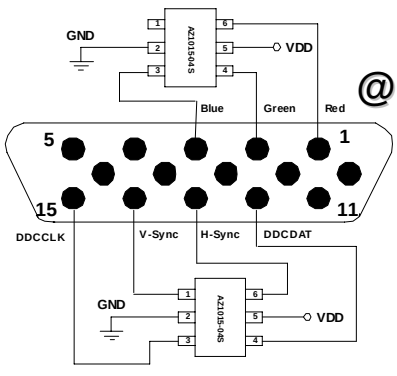


@ USB ports





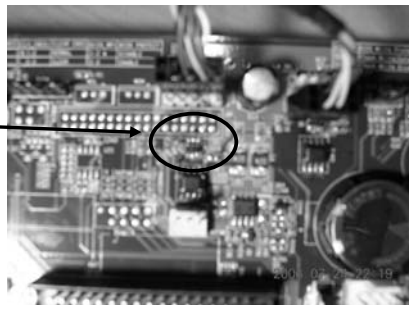
@ Audio Ports



@ VGA ports

Direct Pin Injection Contact Discharge Protection

Put ESD Protect IC @ USB Port



Contact Discharge @ USB ports of PCB

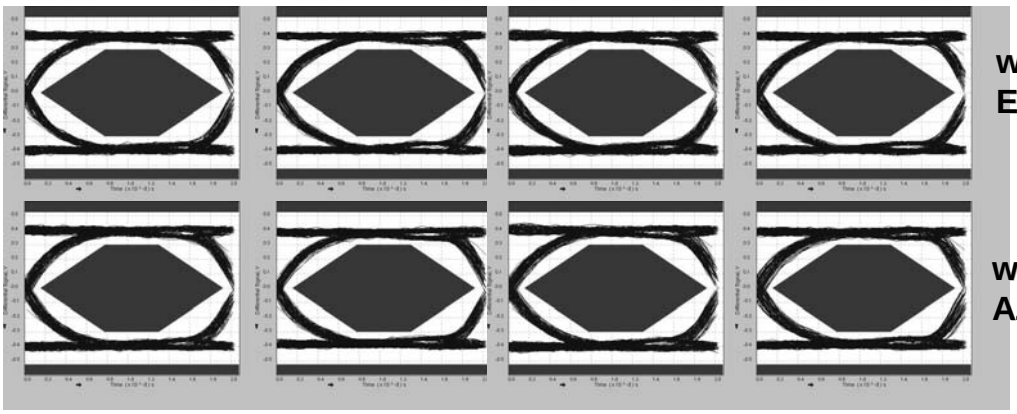
	Self Recover Errors(Class-A) (X: error happened, V: pass)			
Parts	**±600V (contact)**	**±1kV (contact)**	**±2kV (contact)**	**±8kV (contact)**
Cxxxx	**X**	**---**	**---**	**---**
Pxxxxxx	**X**	**---**	**---**	**---**
Sx	**V**	**V**	**X**	**---**
AZ1015-04S	**V**	**V**	**V**	**V**

Helps USB ports to pass 8KV contact Mode

USB 2.0 Eye Diagram Measurement Result

@ High Speed Operation Mode

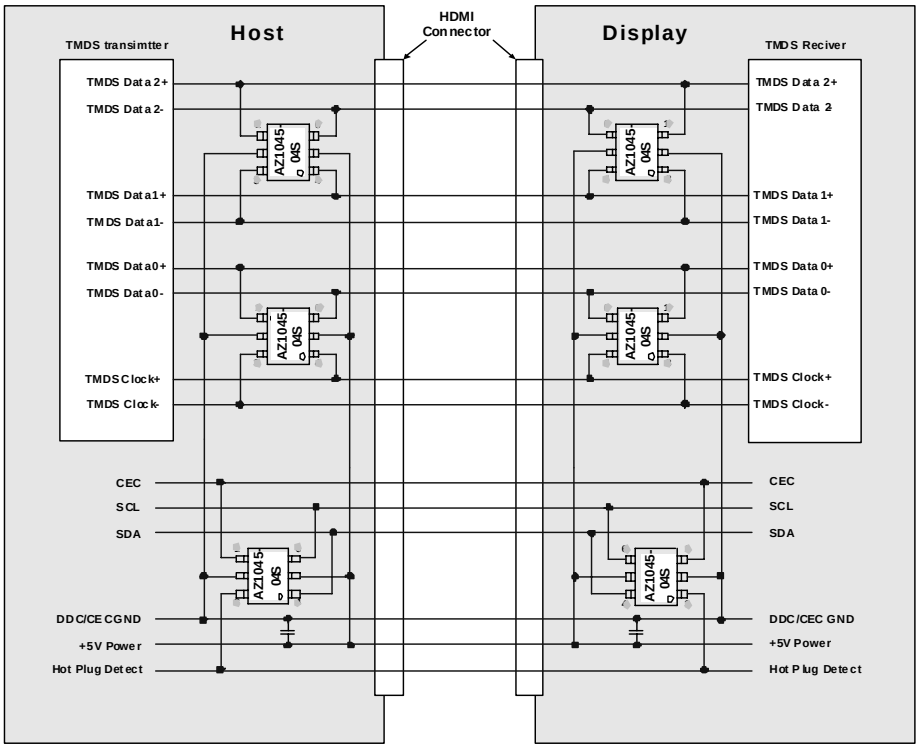
Port 1 **Port 2** **Port 3** **Port 4**



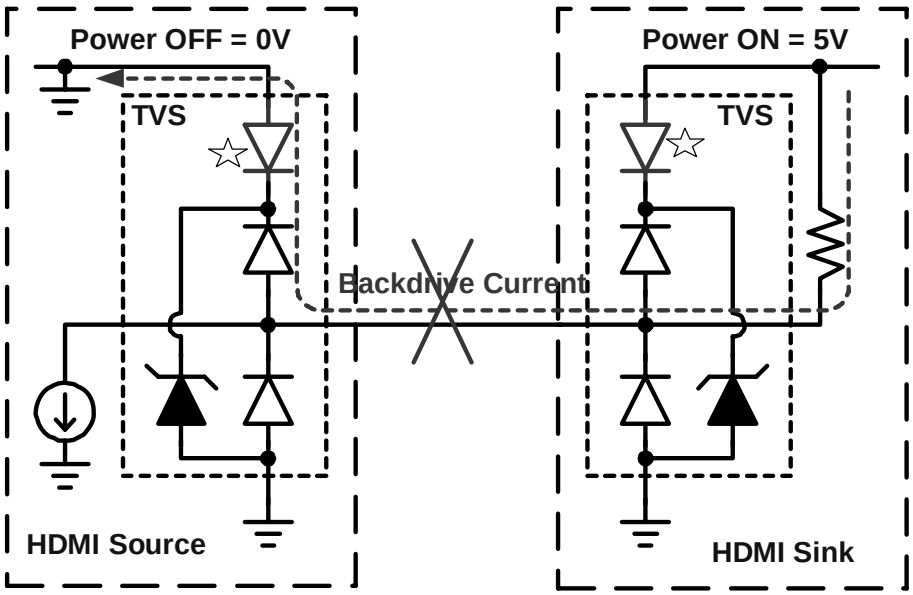
w/o ESD Device

w/ AZ1015-04S

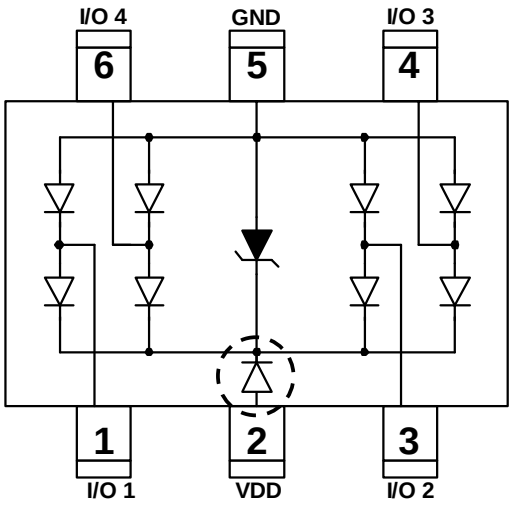
System-Level ESD Protection Design for HDMI Interface



Solve Backdrive Current Problem in HDMI Interface

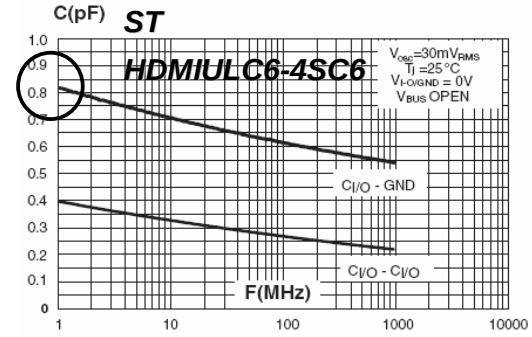


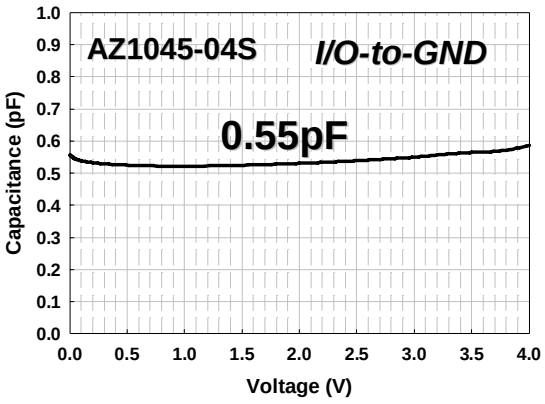
Helps HDMI port to pass 8KV contact Mode



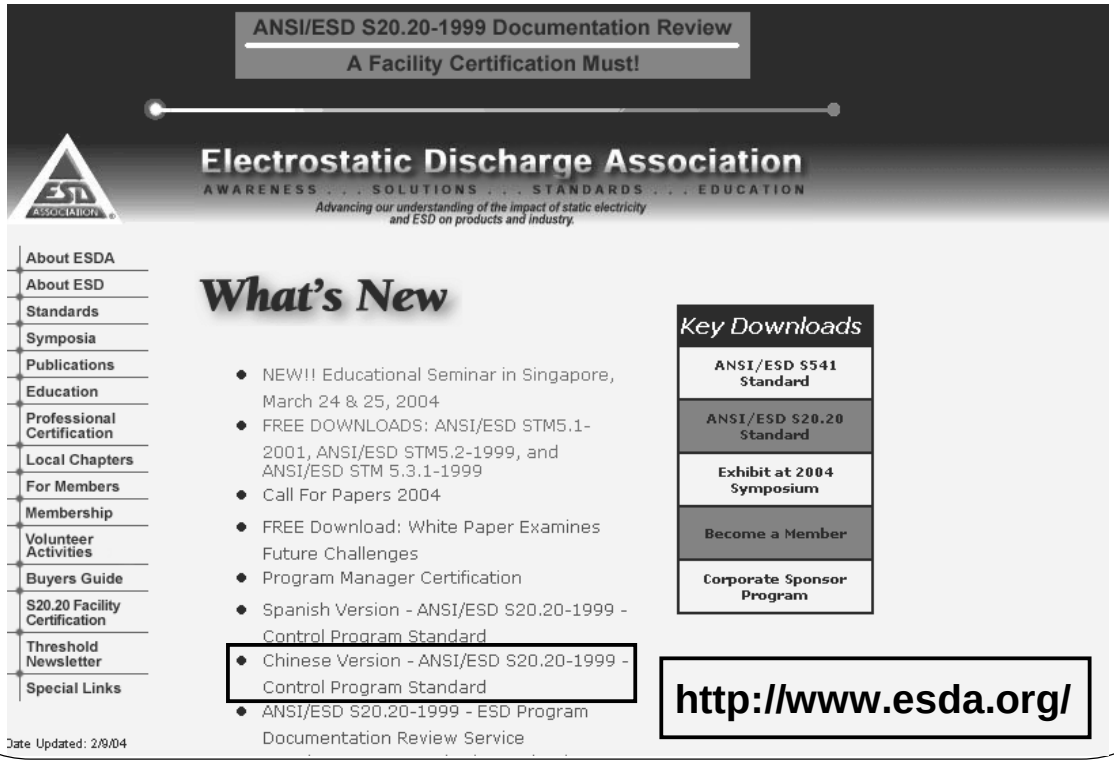
AZ1045-04S

(SOT23-6L)





Electrostatic Discharge Association (ESDA)



Taiwan ElectroStatic Discharge Association

Suggestion / Summary

- **What is the future of nanoscale CMOS IC products :**
  - **(1) Thinner gate oxide (< 20Å)**
  - **(2) Smaller device dimension**
  - **(3) Much larger die size (die capacitance is larger)**
  - **(4) Higher speed I/O interface or GHz RF Signal (limit to adding larger ESD device to the I/O pad)**

➡ **having much lower robustness to ESD events !!!**

- **What we can do :**
  - **(1) Reduce the ESD level generated during manufacturing, assembly, and testing.**
  - **(2) Enhance the on-chip ESD protection robustness of IC products, especially for CDM ESD events.**
  - **(3) System-level ESD solutions should be adopted in microelectronics.**