On-Chip Solution in CMOS Integrated Circuits for System-Level Electrostatic Discharge (ESD) Protection

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Abstract – Recently, the reliability issue of system-level electrostatic discharge (ESD) events is attracting more attention in CMOS integrated circuits (ICs) and microelectronic systems. This tendency results from not only the progress of more integrated functions into a single chip but also from the strict requirements of reliability test in Industry, such as the system-level ESD test standard of IEC 61000-4-2. The electrical/electronic product must sustain the ESD level of ±8 kV (± 15 kV) under contact-discharge (air-discharge) test mode to achieve the immunity requirement of "level 4" in the IEC 61000-4-2 test standard. Such high-energy ESD-induced noise often causes damage or malfunction to CMOS ICs inside the microelectronic systems. For microelectronic systems with CMOS ICs, system-level ESD tests often cause soft errors, including upset or locked states in the system. Traditional on-chip ESD protection circuits in CMOS ICs can protect the internal circuits against ESD damage in component level, but they can not release the locked or frozen states in the microelectronic system under system-level ESD tests. To meet the system-level ESD specifications, two major methods have been used in the past. One method is to add some discrete noise-decoupling components or board-level noise filters on the circuit board to decouple, bypass, or absorb the electrical transient voltage (energy) under system-level ESD test, such as the capacitor filter, ferrite bead, transient voltage suppressor (TVS), and LC filters. The other method is to regularly check any abnormal system condition in CMOS ICs by using an external hardware timer, such as retriggerable monostable multivibrator. However, with more circuit functions integrated into a single chip for system-on-chip (SOC) design, such additional discrete noise-bypassing components may not be integrated into the chip due to the limitation of silicon-based CMOS technology and the substantial increase in the cost of microelectronic products.

In this talk, a new on-chip transient detection circuit for system-level electrostatic discharge (ESD) protection is presented which can detect and memorize the fast electrical transients during the system-level ESD test. Furthermore, a novel on-chip transient-to-digital converter composed of four transient detection circuits and four different RC filter networks has been successfully designed and verified in a 0.18-μm CMOS process with 3.3-V devices, which can detect the fast electrical transients and

convert them into digital thermometer codes after system-level ESD stresses. The output digital thermometer codes of the on-chip transient-to-digital converter linearly correspond to different ESD voltages under system-level ESD tests. Such output digital codes can be used as the firmware index to execute different auto-recovery procedures in microelectronic systems. The on-chip transient-to-digital converter can be further combined with firmware co-design to provide an effective solution to solve the system-level ESD protection issue in microelectronic systems equipped with CMOS integrated circuits.

Biography of Speaker:

Morris (Ming-Dou) Ker received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1993. He was ever worked as the Department Manager in the VLSI Design Division of the Computer and Communication Research Laboratories (CCL), Industrial Technology Research Institute (ITRI), Taiwan. Since 2004, he has been a Full Professor in the Department of Electronics Engineering, National Chiao-Tung University, Taiwan. He ever served as the *Director of Master Degree Program* in the College of Electrical Engineering and Computer Science, National Chiao-Tung University; as well as the *Associate Executive Director* of National Science and Technology Program on System-on-Chip (NSoC Office), Taiwan. In 2008, he was rotated to I-Shou University, Kaohsiung, Taiwan, as Chair Professor and Vice President. In the field of reliability and quality design for circuits and systems in CMOS technology, he has published over 330 technical papers in international journals and conferences. He has proposed many inventions to improve reliability and quality of integrated circuits, which have been granted with 134 U.S. patents and 142 Taiwan patents. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent prosthesis. Prof. Ker had been invited to teach or to consult reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC Industry.

Prof. Ker has served as member of the Technical Program Committee and Session Chair of numerous international conferences. He was selected as the *Distinguished Lecturer* in IEEE Circuits and Systems Society for 2006-2007, and in IEEE Electron Devices Society since 2008. He ever served as Associate Editor in *IEEE Trans. on VLSI Systems*. He was the President of Foundation in *Taiwan ESD Association*. In 2005, one of his patents on ESD protection design has been awarded with the National Invention Award in Taiwan. In 2008, Prof. Ker has been elevated as an IEEE Fellow with the citation of "***for contributions to electrostatic protection in integrated circuits, and performance optimization of VLSI micro-systems***".

Technical talk to *tsmc*

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Outline

- System-Level ESD Test
- On-Chip Transient Detection Circuit
- Board-Level Noise Filter Network
- On-Chip Transient-to-Digital Converter
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