



International Conference on IC Design & Technology

May 18 – May 20, 2009

<http://www.ICICDT.org>

Freescale Semiconductor

7700 W Parmer Lane, Austin, TX 78729



Conference Vision

Global collaboration among professionals engaged in the multi-disciplinary fields of advanced IC design, device design, design tools/technology and process technology development enables accelerated product time-to-market, particularly for high-performance products which incorporate advanced management of power, leakage, device degradation and yield.

Conference overview

ICICDT provides a forum for engineers, researchers, scientists, professors and students to explore the interactions of design and process technology on product / IC development & manufacturing. The unique workshop style of the conference and the unusual opportunity for technologists and product designers to interact enables the exchange of breakthrough ideas and creative collaboration. Two days of technical presentations and workshops will be preceded by a one-day tutorial program of value to both the expert and the beginner.

Close collaboration amongst professionals in the multi-disciplinary technical fields - design/device/process - accelerates the implementation of new designs and new technologies into manufacturing. The separation of system/IC design and manufacturing in the semiconductor industry - leading to the emergence of specialized fabless design houses, wafer foundries, design automation tool/software companies, and semiconductor processing tool suppliers - creates a need for collaboration among individuals with technical skills across these multiple fields. Further, advanced IC technology can no longer offer the same level of control as earlier over many parameters that

have a direct adverse impact on circuit behavior. New IC designs also push the limit of technology, and in some cases, require specific fine-tuning of certain process modules in manufacturing.

Thus the communities of design and technology are increasingly intertwined. The issues which require close interaction and collaboration for trade-off and optimization across the design/device/process fields are addressed in this conference. Hence, this conference is organized in a single session format (with no parallel sessions) with 58 invited and contributed talks, to provide opportunities for a direct interaction among the attendees and presenters, to participate in discussions across multiple disciplines of design/device/process issues during the two days of 14 plenary & workshop sessions. Each session is organized with short oral presentations followed by a one-hour workshop to facilitate interactive discussion of questions & answers. In addition, on the first day, five in-depth tutorial courses have been organized.

Who Should Attend?

This conference is intended for IC design, circuit, device, process, integration, and reliability engineers and managers working to accelerate the product time-to-market through the implementation of new designs and new technologies into manufacturing, including the design and development of advanced devices and materials, and IC and device reliability.

Conference Venue

The venue for the 2009 Conference is Freescale Semiconductor at Austin, Texas, U.S.A.



Central Texas Section



The Japan Society
of Applied Physics



IEEE Circuits and Systems Society

For registration, please go to www.icicdt.org Conference pre-registration deadline is April 20th, 2009

International Conference on IC Design & Technology

May 18 – May 20, 2009, Freescale Semiconductor, Austin, TX, U.S.A.; <http://www.ICICDT.org>

Committee Members

- Amara Amara, ISEP (General Chair)
- Koji Eriguchi, Kyoto University (Conference Chair)
- Tanay Karnik, Intel (Conference Past Chair)
- Marc Belleville, LETI (2010 Chair elected)
- Chua-Chin Wang, National Sun Yat-Sen University (2011 Chair elected, I/O Circuits and ESD Protection Chair)
- Thuy Dao, Freescale Semiconductor (Conference Executive Committee Chair, IEEE ED CTS Chair)
- Dina Triyoso, Freescale Semiconductor (Conference Treasurer, IEEE ED CTS Vice Chair)
- Jean-Luc Leray, CEA (Conference Secretary)
- Thomas Ea, ISEP (Publication chair)
- Terrence Hook, IBM (Publicity Chair)
- Chris Kim, University of Minnesota (Tutorials Chair)
- Ali Keshavarzi, TSMC (Tutorials Chair)
- David Pan, University of Texas at Austin (Award Chair)
- Dac Pham, Freescale Semiconductor (Local Arrangements Chair, SOC Chair)
- Aurangzeb Khan, Everspin, Inc. (SOC Chair)
- Toshinari Takayanagi, Apple (Low Power Chair)
- Geoffrey Yeap, Qualcomm (Low Power Chair)
- Jan Ackaert, On Semiconductor (High Power Devices Chair)
- Susumu Shuto, Toshiba Corporation (Advanced Memory Devices Chair)
- Hideto Hidaka, Renesas (Advanced Memory Devices Chair)
- Yuuichiro Mitani, Toshiba Corporation (PID/Reliability Chair)
- Keith Bowman, Intel (DFM/DFT/DFR/DFY Chair)
- Ruchir Puri, IBM (CAD Chair)
- Dong-Won Kim, Samsung Electronics (Advanced Transistors Chair)
- Arnaud Pouydebasque, CEA (Advanced Transistors Chair)
- Phillip Christie, NXP Semiconductor (Technology Pathfinding Chair)
- Didier Berlot, STMicroelectronic (RF/Analog Chair)
- Andrea Mazzanti, Universita di Modena e Reggio (RF/ Analog Chair)
- Ming-Dou (Morris) Ker, I-Shou University (I/O Circuits and ESD Protection Chair)
- Eishi Ibe, Hitachi (SER Chair)
- Simon Deleonibus, CEA (Emerging Technologies)
- Garrett Polhamus, SWBell (IEEE CTS Chair)
- Andrea Scarpa, NXP Semiconductors
- Atsuki Inoue, Fujitsu
- Bart Keppens, Sarnoff Europe
- Bich-Yen Nguyen, Soitec
- Charles Slayman, Sun Microsystems
- David Duarte, Intel
- David Tremouilles, LAAS/CNRS
- Himansu Arora, Duke University
- Ingo Aller, IBM
- Jason Stinson, Intel
- John Robertson, Cambridge University
- Kin P. (Charles) Cheung, NIST
- Linten Dimitri, IMEC
- Manfred Engelhardt, Qimonda
- Masaya Sumita, Panasonic
- Nobuyuki Mise, Hitachi
- Paul Tong, Pericom Semiconductor
- Philippe Royannez, TI
- Prashant Majhi, SEMATECH
- Rouwaida Kanj, IBM
- Salvatore Lombardo, IMM of the CNR
- Shrikanth Krishnan, TI
- Shui-Ming Cheng, TSMC
- Toshiro Hiramoto, University of Tokyo
- Veronique Ferlet, CEA
- Ya-Hsin Hsueh, National Yunlin University of Science and Technology

International Conference on IC Design & Technology

May 18 – May 20, 2009, Freescale Semiconductor, Austin, TX, U.S.A.; <http://www.ICICDT.org>

ICICDT Tutorials

Tutorial Chair: Prof. Chris H. Kim, University of Minnesota

May 18, 2009

“Technology-Circuit-Architecture Optimization for Energy Efficient Integrated Systems”

**Tutorial Chair: Prof. Chris H. Kim, University of
Minnesota**

On this first day of ICICDT, five in-depth tutorial courses have been organized, to provide a head-start learning opportunity in IC design & technology. This year's tutorial will discuss the interaction between technology, circuit, and architecture for designing robust energy efficient integrated systems. With Moore's law approaching its limit and the mounting pressure to deliver new products with advanced features, such interaction between different levels of design abstraction is becoming indispensable. Topics will range from advanced memory circuits and wireless transceivers to VLSI signal processing for medical/communication applications and mixed-signal I/Os. Specific design examples will be presented to highlight real world implications. This tutorial is targeted for both experienced researchers and a general engineering audience.

08:30 a.m. **Registration & Breakfast (Included)**

09:00 a.m. **Technology, Circuits, and Systems: Can't
We All Just Get Along?**

Presenter: Dr. Leland Chang, IBM TJ
Watson Research Center

Abstract: As challenges mount in the continued advancement of microelectronics, a broad perspective is needed to assess the tradeoffs involved in overcoming or circumventing current limits to CMOS technology scaling. Device technologists, circuit designers, and systems architects can no longer focus solely on their own realms of expertise, but must also understand the issues faced by the other communities to achieve an overarching goal of robust, high-performance, and power-efficient computing systems. In this tutorial, specific examples of such interaction will be cited from recent areas of research, including new materials and device structures, embedded memory scaling and bandwidth, and

overall system power efficiency. Future research directions will be discussed, with a particular emphasis on the search for post-CMOS device options, which further underscores the need to assess benefits and tradeoffs across technology, circuits, and systems perspectives.

Bio: Leland Chang received the B. S., M. S., and Ph.D. degrees in electrical engineering and computer sciences from the University of California, Berkeley and joined the IBM T. J. Watson Research Center in 2003, where he is now Manager of Design and Technology Solutions. His early research focused on pioneering work in ultra-thin body and double-gate MOSFETs for CMOS scaling, including fabrication of the FinFET double-gate structure down to record gate lengths. More recently, he has pursued SRAM scaling issues, which has resulted in the demonstration of SRAM cells down to record sizes and the proposal and demonstration of 8T-SRAM for variability tolerance and low voltage operation. His current work focuses on interactions between technology and circuit design, with a particular emphasis on embedded memory and power efficiency. He holds 9 patents and has authored more than 45 technical articles.

10:15 a.m. **Coffee Break**

10:30 a.m. **Design of Ultra-Low Power Transceivers for
Wireless Sensors**

Presenter: Prof. Brian Otis, University of
Washington

Abstract: Emerging applications of wireless sensors require new levels of system integration, functionality, and lifetime. Body area networks, implantable devices, and small animal tracking research are a few examples that will be discussed. These applications place increasingly severe demands on RFIC designers. Miniaturization and power concerns, already important considerations in portable radio design, are amplified in these emerging wireless sensor applications. Additionally, there are several needs on the horizon that will demand completely thin-film integration of RF

International Conference on IC Design & Technology

May 18 – May 20, 2009, Freescale Semiconductor, Austin, TX, U.S.A.; <http://www.ICICDT.org>

transceivers, prohibiting surface-mount components of any kind. This talk will discuss various RF transceiver design techniques, including miniaturized MEMS-based radios, frequency-multiplying transceiver architectures, and wirelessly-powered sensor data links. Test chip architectures will be presented and measured results described.

Bio: Brian Otis received the B.S. degree in electrical engineering from the University of Washington and the M.S. and Ph.D. degrees from the University of California at Berkeley. He joined the faculty of the University of Washington as Assistant Professor of Electrical Engineering in August 2005. His primary research interests are ultra-low power RFIC design and bioelectrical interface circuits and systems. He has previously held positions at Intel Corporation and Agilent Technologies. Dr. Otis is an Associate Editor of the IEEE Transactions on Circuits and Systems Part II. He was the recipient of the 2003 U.C. Berkeley Seven Rosen Funds award for innovation and was co-recipient of the 2002 ISSCC Jack Raper Award for Outstanding Technology Directions Paper.

11: 45 p.m.

Lunch

01: 00 p.m.

Low-power VLSI Signal Processing for Medical and Communication Systems

Presenter: Manish Goel, Texas Instruments

Abstract: In this talk, we will present low-power signal processing techniques used in energy-constrained medical applications and high data-rate wireless communication systems. For the wireless communication systems, we will discuss two OFDM systems including terrestrial digital TV DVB-H receiver and next-generation LTE wireless cellular modem. We will look at the trade-offs between flexibility and power consumption for physical layer signal processing including implementation trade-offs for a few components such as FFT, MIMO decoder and forward error correction decoder. For medical applications, we will consider a system built around an ultra low-power 16-bit microcontroller platform and show trade-offs for choosing the optimum design parameters such as flexibility, parallelism, clock frequency and voltage. For this application, implementation trade-offs for common building blocks such as FFT and

filtering will be considered.

Bio: Manish Goel joined Texas Instruments in 2000 and holds position of senior member of technical staff in Signal Processing systems R&D center at Texas Instruments. Manish's research interests are in low-power, signal processing, wireless communication and medical systems. Manish has led and contributed to several wireless R&D efforts at TI including mobile digital TV receiver, 4G WiMAX/LTE modem, multi-antenna wireless LAN and fixed-wireless access. He is currently managing an R&D team involved in low-power signal processing VLSI for medical and communication applications. Manish received his bachelor's degree from India Institute of technology in Delhi, and a master's degree and Ph.D. from the University of Illinois at Urbana-Champaign.

02: 30 p.m.

Integrated Sensors for Measuring Noise Processes in Modern Microprocessors

Presenter: Alan Drake, IBM Austin Research Labs

Abstract: Noise is the enemy of efficiency. Within the complexity of modern microprocessors are the seeds of the noise that increase timing margins and that reduce efficiency. Microprocessors are a marvel of integration with a mix of processing cores and support circuitry, but shifting workloads between cores coupled with process variation and other environmental factors increases timing noise and hence the design margin. Much work has been done to improve microprocessor efficiency from work-load balancing policies in the software to dynamic voltage and frequency scaling, but multi-core microprocessors complicate any kind of operating point response as each core will be unique. Designing circuits that function as integrated sensors which can be used to select the correct operating point is the topic of this talk. Included are sensors that measure temperature, voltage, process variation, timing margin, and other noise processes. With these integrated sensors incorporated into an appropriate feedback loop, the data needed can be provided to increase the efficiency of microprocessors, or of any integrated circuit.

Bio: Alan Drake received his B.S. degree from

International Conference on IC Design & Technology

May 18 – May 20, 2009, Freescale Semiconductor, Austin, TX, U.S.A.; <http://www.ICICDT.org>

the University of Arizona and his M.S. and Ph.D. degrees from the University of Michigan, all in Electrical Engineering. In 2004 he joined the research staff at IBM's Austin Research Lab. His research is focused on low-power circuit design and integrated timing sensors. Included in this is work on using resonant clocking to reduce local clock power, adaptive body-biasing techniques for SOI circuits, and more recently designing critical path monitors to provide feedback to dynamic voltage and frequency scaling systems.

03: 45 p.m. **Coffee Break**
04:00 p.m. **Mixed-Voltage I/O Circuits and ESD Protection Design in CMOS ICs**

Presenter: Prof. Morris (Ming-Dou) Ker, I-Shou University, Kaohsiung, Taiwan

Abstract: To improve circuit operating speed and performance, the device dimension of MOSFET has been shrunk in the advanced CMOS integrated circuits (ICs). With the scaled-down device dimension and thin gate oxide in the advanced nanoscale CMOS technology, the power supply voltage of normal circuit operation is also scaled down to reduce the power consumption and to meet the gate-oxide reliability. However, most microelectronic systems nowadays still consist of the semiconductor chips fabricated in different CMOS technologies. Therefore, the microelectronic systems often require the I/O interface circuits between semiconductor chips or sub-systems which have different power supply voltages. With the different power supply voltages in a microelectronic system, chip-to-chip I/O circuits must be designed to avoid electrical overstress across the gate oxide, to avoid hot-carrier degradation on the output devices, and to prevent the undesired leakage current paths between the chips. Therefore, some advanced mixed-voltage I/O circuits had been developed to handle the I/O signals of higher voltage level but only realized with low-voltage CMOS devices.

Besides the different voltage levels of I/O signals in the mixed-voltage I/O circuits, such mixed-voltage I/O circuits connected to the bonding pad in CMOS ICs are still requested to meet the electrostatic discharge (ESD) specifications in IC industry. For safe production of CMOS ICs, the ESD robustness

for commercial IC products was traditionally requested to sustain ESD levels of $\pm 2\text{kV}$ in the test standard of Human Body Model (HBM). How to design the on-chip ESD protection circuits to effectively protect the mixed-voltage I/O circuits realized by the nanoscale CMOS devices with thin gate oxide is a quite difficult challenge. Such on-chip ESD protection circuits for mixed-voltage I/O circuits should meet the gate-oxide reliability constraints and prevent the undesired leakage current paths during normal circuit operating condition. Under ESD zapping condition, the ESD protection circuit should be quickly triggered on to discharge ESD current.

In this Tutorial, the design of mixed-voltage I/O circuits realized with low-voltage CMOS devices is introduced, and then the on-chip ESD protection design for mixed-voltage I/O circuits without using the additional thick gate-oxide process is presented. Some advanced ESD protection designs by using high-voltage-tolerant power-rail ESD clamp circuits to protect mixed-voltage I/O circuits will be demonstrated with silicon verification in nanoscale CMOS technology. ESD protection for CMOS ICs is not only the process issue but also highly dependent to the design issue. Mixed-voltage I/O circuits and the corresponding ESD protection designs have become important reliability design issues in nanoscale CMOS IC products, wherefore the circuit designers need to watch.

Bio: Morris (Ming-Dou) Ker received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1993. He was ever worked as the Department Manager in the VLSI Design Division of the Computer and Communication Research Laboratories (CCL), Industrial Technology Research Institute (ITRI), Taiwan. Since 2004, he has been a Full Professor in the Department of Electronics Engineering, National Chiao-Tung University, Taiwan. He also served as the *Director of Master Degree Program* in the College of Electrical Engineering and Computer Science, National Chiao-Tung University; as well as the *Associate Executive Director* of National Science and Technology Program on System-on-Chip (NSoC), Taiwan. In 2008, he was rotated to I-Shou University, Kaohsiung, Taiwan, as Chair Professor and Vice President. In the field of reliability and quality design for

International Conference on IC Design & Technology

May 18 – May 20, 2009, Freescale Semiconductor, Austin, TX, U.S.A.; <http://www.ICICDT.org>

circuits and systems in CMOS technology, he has published over 360 technical papers in international journals and conferences. He has proposed many inventions to improve reliability and quality of integrated circuits, which have been granted with 138 U.S. patents and 144 Taiwan patents. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent prosthesis. Prof. Ker had been invited to teach or to consult reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC Industry.

Prof. Ker has served as member of the Technical Program Committee and Session Chair of numerous international conferences. He was selected as the *Distinguished Lecturers* in IEEE Circuits and Systems Society for 2006-2007, as well as, in IEEE Electron Devices Society for 2008-2009. He ever served as Associate Editor in *IEEE Trans. on VLSI Systems*. He was the President of Foundation in *Taiwan ESD Association*. In 2008, Prof. Ker was elevated as an IEEE Fellow with the citation of “*for contributions to electrostatic protection in integrated circuits, and performance optimization of VLSI micro-systems*”. In 2009, Prof. Ker was awarded as one of the top ten *Distinguished Inventors* in Taiwan, and also selected as one of top hundred *Distinguished Inventors* in China.

05: 15 p.m. **Adjourn**

International Conference on IC Design & Technology

May 19 – May 20, 2009, Freescale Semiconductor, Austin, TX, U.S.A.; <http://www.ICICDT.org>

Plenary & Workshop Sessions May 19 – May 20, 2009

May 19, 2009

08:00 a.m. **Registration & Breakfast (Included)**
08:30 a.m. **Opening Remarks: Koji Eriguchi, Kyoto University, Conference Chair,**
08:40 a.m. **Keynote Speech: A Sub 2W Low Power IA Processor for Mobile Internet Devices in 45nm Hi-K Metal Gate CMOS, Gianfranco Gerosa, Sr. PE, Intel, USA**

Session A: Low Power

Co-Chairs **Toshinari Takayanagi, Apple, USA & Geoffrey Yeap, Qualcomm, USA.**
09:30 a.m. **Invited: Custom Design in Low-Power/High-Performance ASIC World, Ty Garibay, Richard Reis, TI, USA**
09:40 a.m. **LLA: A Low-Latency Asynchronous Pipeline Control Circuit, Morteza Gholipour Geshnyani, Mehrdad Nourani, Ali Afzali-Kusha, Azad University of Behshahr, Iran**
09:50 a.m. **A Low-Power and Multi-Mode Design Approach for Reconfigurable MASH SDM, Hsin-Liang Chen and Jen-Shiun Chiang, Tamkang University, Taiwan**
10:00 a.m. **Invited: Implementation and Evaluation of Fine-grain Run-time Power Gating for a Multiplier, Kimiyoshi Usami, Mitsutaka Nakata, Toshiaki Shirai, Seidai Takeda², Naomi Seki¹, Hideharu Amano¹ and Hiroshi Nakamura², Shibaura Institute of Technology, ¹Keio University, ²The University of Tokyo, Japan**
10:10 a.m. **Improvement of LDO's PSRR Deteriorated By Reducing Power Consumption: Implementation and Experimental Results, Socheat HENG, Cong-Kha PHAM, UEC, Japan**
10:20 a.m. **Asynchronous Dual-Mode Buck Converter Design with Protection Circuits for Battery Applications, Jefferson A. Hora, Jiun-Chang Zeng, and Wan-Rone Liou, National Taipei University, Taiwan**
10:30 a.m. **Large Random Telegraph Noise in Sub-Threshold Operation of Nano-Scale nMOSFETs, J.P. Campbell, L.C. Yu, K.P. Cheung, J. Qin, J.S. Suehle, A. Oates, K. Sheng, National Institute of Standards and Technology, USA**

10:40 a.m. – 11:00 a.m. **Coffee Break**

Session B: ESD

Co-Chairs **Morris Ker, I-Shou University, Taiwan. &**

Chua Chin Wang, National Sun Yat-Sen University, Taiwan.
11:00 a.m. **Invited Paper: Low-Leakage Electrostatic Discharge Protection Circuit in 65-nm Fully-Silicided CMOS Technology, Prof. Ming-Dou (Morris) Ker et al., Taiwan**
11:10 a.m. **Invited Paper: ESD+RFIC Co-Design: Methodology, Optimization and Examples, Prof. Albert Wang, UC Riverside, USA**
11:20 a.m. **A 0.9 V to 5 V Mixed-Voltage I/O Buffer Using NMOS Clamping Technique, Prof. Chua-Chin Wang, Jen-Wei Liu, Ron-Chi Kuo, National Sun Yat-Sen University, Taiwan**

Session C: High Power

Co-chairs: **Jan Ackaert, On Semiconductor, Belgium & Thuy Dao, Freescale Semiconductor, USA**
11:30 a.m. **Invited Paper: Recent Advances in RF-LDMOS High Power IC Development, Wayne Burger, Freescale Semiconductor, USA**
11:40 a.m. **Through Silicon Via Stress Characterization, Thuy Dao, Dina H. Triyoso, Mike Petras, Freescale Semiconductor, and Michael Canonico, USA**
11:50 a.m. **A 30V Complementary Bipolar Technology for xDSL Line Drivers, J. Speyer, Thomas J. Krutsick, and John K. Moriarty, Zarlink Semiconductor, USA.**

12:00p.m. – 01:00 p.m. **Workshops A, B, C**

01:00p.m. – 02:00 p.m. **Lunch**

Session D: CAD

Co-chairs: **Ruchir Purir, IBM, USA & David Pan, UT of Austin, USA**
02:10 p.m. **Cell Merge: A Basic-Pre-Clustering Clustering Algorithm for Placement, X. Zhang, T. Takeuchi, M. Koyonaga, Kochi Univ, Japan**
02:20 p.m. **AKEBONO: A Novel Quick Incremental Placer, X. Zhang, T. Takeuchi, M. Koyonaga, Kochi Univ, Japan**
02:30 p.m. **Applications of Network Coding in Global Routing, N. Nemade, A. Spritson, J. Hu, Texas A&M Univ, TX**
02:40 p.m. **Timing Analysis of Dual-Edge-Triggered Flip-Flop Based Circuits with Clock Gating, Chungki Oh, Sangmin Kim, and Youngsoo Shin, KAIST, Korea**
02:50 p.m. **Timing yield estimation with clock network correlations by propagating discrete probability distributions, L.Yu, C. Shin, J.**

International Conference on IC Design & Technology

May 19 – May 20, 2009, Freescale Semiconductor, Austin, TX, U.S.A.; <http://www.ICICDT.org>

03:00 p.m. Liou, Y. Shin, KAIST Korea, National Tsing Hua Univ, Taiwan
03:10 p.m. **Network Flow Based BSM Assignment**, Hua Xiang, Haoxing Ren, Tingdong Zhou, IBM
03:20 a.m. – 03:35 p.m. **A Simple Fast Exact Density Calculation Algorithm**, Hua Xiang, C. Chiu, R. Puri, IBM, Iowa State Univ, IA.

Coffee Break

Session E: PID/high K

Co-chairs: **Koji Eriguchi, Kyoto University, Japan & Kin P. (Charles) Cheung, National Institute of Standards & Technology, USA.**
03:35 p.m. **Invited Paper: The Negative Bias Temperature Instability vs. High-Field Stress Paradigm**, J.P. Campbell¹, K.P. Cheung¹, J.S. Suehle¹, and A.S. Oates², ¹National Institute of Standards and Technology, USA, ²TSMC Ltd., Taiwan
03:45 p.m. **Invited Paper: Unified TDDDB Model for Stacked High-k Dielectrics** - Byoung Hun Lee, Gwangju Institute of Science and Technology, Korea
03:55 p.m. **Factors impacting stabilization of tetragonal phase in Hf_xZr_{1-x}O₂ high-k dielectrics**, D.H. Triyoso, R.I. Hegde, R. Gregory, G. Spencer, J.K. Schaeffer, and M. Raymond, Freescale Semiconductor, USA
04:05 p.m. **Impact of Gate-Oxide Breakdown on Power-Gated SRAM**, Hao-I Yang, Ching-Te Chuang, and Wei Hwang, National Chiao-Tung University, Hsinchu, Taiwan
04:15 p.m. **Simulation and Experimental Study on the Characteristics of Plasma-Induced Damage and Methodology for Accurate Damage Analysis**, Matsuda, Asahiko, Yoshinori Nakakubo, Riki Ogino, Hiroaki Ohta, Koji Eriguchi, and Kouichi Ono, Kyoto University, Kyoto, Japan
04:25 p.m. **Study of Plasma-Induced "Si Recess Structure" and Its Effects on Threshold Voltage Variability in Advanced MOSFETs**, Koji Eriguchi, Asahiko Matsuda, Yoshinori Nakakubo, Masayuki Kamei, Hiroaki Ohta, and Kouichi Ono, Kyoto University, Kyoto, Japan

Session F: SER

Co-chairs: **Eishi Ibe, Hitachi, Japan**
4:35 p.m. **Invited: SEE Characterization and Mitigation in Ultra-Deep Submicron Technologies**, David G. Mavis, Paul H. Eaton, and Michael D. Sibley, Microelectronics Research Development Corporation, New Mexico, USA

4:45 p.m. **Invited: Combined Altitude and Underground Real-Time SER Characterization of CMOS Technologies on the ASTEP-LSM Platform**
J.L. Autran, P. Roche, S. Sauze, G. Gasiot, D. Munteanu, P. Loaiza, M. Zampalo and J. Borel, Aix-Marseille University, France
5:05 p.m. **A 2.5 GHz Radiation Hard Fully Self-biased PLL using 0.25 μ m SOS-CMOS technology**, Partha Pratim Ghosh, E. Xiao, University of Texas at Arlington, Arlington, TX, USA
5:15 p.m. **Soft Error Estimates for Fabless Companies**, Anand Dixit, Raymond Heald, Sun Microsystems, Santa Clara, CA, USA

05:30 p.m. – 06:30 p.m. **Workshops C, D, E, F**

06:30 p.m. – 07:00 p.m. **Reception**

Rump Session

Chair **Marc Belleville, CEA, France**
07:00 p.m. - 8:00pm

May 20, 2009

08:00 a.m. **Registration & Breakfast (Included)**
08:30 a.m. **Opening remarks & announcements**
08:40 a.m. **Keynote Speech: QorIQ P4080 Communications Processor Design in 45nm SOI**, Greg Bartlett, VP, Design Technology, Freescale Semiconductor, USA

Session G: System on a Chip

Co-chairs: **Aurangzeb Khan, Everspin Technologies, USA & Dac Pham, Freescale Semiconductor, USA.**
09:30 a.m. **Invited Paper: A Low-Power Multi-Core Media Co-Processor for Mobile Application Processors**, Shuou Nomura, Fumihiko Tachibana, Tetsuya Fujita, Chen Kong Teh, Hiroyuki Usui, Fumiyuki Yamane, Yukimasa Miyamoto, Takahiro Yamashita, Hiroyuki Hara, Mototsugu Hamada, Yoshiro Tsuboi, Toshiba Corporation, Kawasaki, Japan
09:40 a.m. **Implementation of area efficient H.264/AVC CAVLC Decoder**, Byung-Sik Choi, Jong-Yeol Lee, Chonbuk University, South Korea.
09:50 a.m. **Implementation of Scalable Interconnect Networks for data reordering used in Discrete Trigonometric Transforms (DTT)**, Adel Hussein, Adnan Suleiman, Nabil Kerkiz¹, David Akopian, UTSA, USA, ¹Intel Corporation, Austin, TX, USA
10:00 a.m. **Semi-Custom Design Flow: Leveraging Place and Route Tools in Custom Circuit Design**,

International Conference on IC Design & Technology

May 19 – May 20, 2009, Freescale Semiconductor, Austin, TX, U.S.A.; <http://www.ICICDT.org>

10:10 a.m. Nadeem N. Eleyan, Ken Lin, Masud Kamal, Baker Mohammad, Paul Bassett, Qualcomm, Austin, TX, USA.
Invited Paper: Technology and Design Aspects of Ultra-Thin Silicon Chips for Bendable Electronics, Harald Richter, Horst Rempp, Joachim Burghartz, Mahadi-Ul Hassan, Christine Harendt, Nicoleta Wacker, Martin Zimmermann, Institute for Microelectronics, Stuttgart, Germany.

10:20 a.m. – 10:35 a.m. **Coffee Break**

Session H: Advance Transistors

Co-Chairs : **Bich Yen Nguyen, Soitec, USA & Dong-won Kim, Samsung, South Korea**

10:35 a.m. **Invited Paper : Jason Woo, UCLA, USA**

10:45 a.m. **Systematic Approach of FinFET based SRAM Bitcell Design for 32nm Node and Below**, S. C. Song, M. Abu-Rahma, B. M. Han, L. Ge, S. S. Yoon, J. Wang, W. Yang¹, D. Liu¹, C. Hu¹, and G. Yeap, Qualcomm, USA

10:55 a.m. **Stacked 3-Dimensional 6T SRAM Cell with Independent Double Gate transistors**, Marcus Weis, Andrzej Pfitzner, Dominik Kasprowicz, Rainer Emling, Thomas Fischer, Stephan Henzler, Wojciech Maly and Doris Schmitt-Landsiedel, Technical University Munich, Germany

11:05 a.m. **Dynamic Power Analysis for Custom Designs**, Stephen Bijansky, Bassam Mohd, and Baker Mohammad, Qualcomm, USA

11:15 a.m. **A Novel Poly-Si Thin-Film Transistor with Multi-Trenched Body by Using Isotropic-etching for Suppressing Off-State Leakage**, Hsien-Nan Chiu, Jyi-Tsong Lin, Yi-Chuen Eng, Po-Hiesh Lin, Tzu-Feng Chang, Chih-Hung Sun, Chih-Hao Kuo and Hsuan-Hsu Chen, Department of Electrical Engineering/National Sun Yat-Sen University, Taiwan

Session I: Memory

Co-chairs: **Hideto Hidaka, Renesas, Japan & Susumu Shuto, Toshiba, Japan.**

11:25 a.m. **Invited Paper: Embedded Non-Volatile Memory Technologies**, Kelly Baker, Freescale Semiconductor, USA

11:35 a.m. **Robust Multi-VT 4T SRAM Cell in 45nm Thin BOx Fully-Depleted SOI technology with Ground Plane**, J.-P. Noel, O. Thomas, C. Fenouillet-Beranger, M.-A. Jaud and A. Amara, CEA LETI, France

11:45 a.m. **Compact 6T SRAM cell with robust Read/Write stabilizing design in 45nm Monolithic 3D IC technology**, Olivier THOMAS, Maud VINET, Olivier ROZEAU,

Perrine BATUDE, Alexandre VALENTIAN, CEA, France

11:55 a.m. **Operation of Multi-Level Phase Change Memory Using Various Programming Techniques**, Jun-Tin Lin, Yi-Bo Liao, Meng-Hsueh Chiang, and Wei-Chou Hsu, National Ilan University, Taiwan

12:05 p.m. – 01:00 p.m. **Lunch**

01:00 p.m. – 2:00 p.m. **Workshops G, H, I**

Session J: DFM/DFT/DFR/DFY

Co-chairs: **Tanay Karnik, Intel, USA & Rouwaida Kanj, IBM, USA**

02:00 p.m. **Invited Paper: An On-Chip Process Control Monitor for Process Variability Measurements in Nanometer Technologies**, Fabian Klass, Ashish Jain, and Greg Hess, Apple Inc., Cupertino, CA

02:10 p.m. **Invited Paper: Statistical-Aware Designs for the nm Era**, Rajiv Joshi¹ and Rouwaida Kanj², IBM. ¹IBM TJ Watson Research Center, Yorktown Heights, NY, ²IBM Austin Research Labs, Austin, TX.

02:20 p.m. **Dynamic Cache Resizing Architecture for High Yield SOC**, Baker Mohammad¹, Muhammad Tauseef Rab^{1,3}, Khadir Mohammad², and M. Aater Suleman³
¹Qualcomm Incorporated, ²University of Texas at San Antonio, San Antonio, TX, ³University of Texas at Austin, Austin, TX.

02:30 p.m. **An Innovative Timing Slack Monitor for Variation Tolerant Circuits**, B. Rebaud¹, M. Belleville¹, E. Beigné¹, M. Robert², P. Maurine², and N. Azemard². ¹CEA, LETI, MINATEC, Grenoble, France, ²LIRMM - CNRS - Université Montpellier II, Montpellier, France.

02:40 p.m. **Machine Learning based Lithographic Hotspot Detection with Critical Feature Extraction and Classification**, Duo Ding, Xiang Wu, Joydeep Ghosh, and David Z. Pan
University of Texas at Austin, Austin, TX.

Session K: Emerging Technology

Co-chairs: **Simon Deleonibus, CEA, France**

2:50 p.m. **Invited: Semiconductor Nanowires: From Science to Technology**, Ali Javey, UC Berkeley, USA

3:00 p.m. **Invited: High K impact on device performance and Reliability**, Jack Lee, UT Austin, USA

3:10 p.m. **One-transistor bistable-body tunnel SRAM**, K. Karda, J. Brockman, S. Sutar, and A. Seabaugh, ND

International Conference on IC Design & Technology

May 19 – May 20, 2009, Freescale Semiconductor, Austin, TX, U.S.A.; <http://www.ICICDT.org>

3:20 p.m. **Complementary Nano-Electro-Mechanical Switches For Ultra-Low-Power Applications: Fabrication, Design and Simulation**, Khawla Alzoubi, Daniel G. Saab, and Massood Tabib-Azar, CWRU

3:30 p.m. - 3:45 p.m. **Coffee Break**

Session L: RF / Analog

Co-Chairs **Didier Berlot, STMicroelectronic, France & Marc Belleville, CEA, France**

3:45 p.m. **Design of a monolithic width programmable gaussian monocycle pulse generator for ultra wideband radar in cmos technology**, Olivier Lemaire, Tian Xia University of Vermont, United States of America

3:55 p.m. **A 1.8V 200mW 8-bit 1GSPS CMOS A/D Converter with a Cascaded-Folding and an Interpolation**, Jooho Hwang, Dongheon Lee, Sunghyun Park, Junho Moon, and Minkyu Song, Dongguk University, Seoul Korea

4:05 p.m. **An 8-bit 500MHz Two-Step ADC in 0.13-um SiGe BiCMOS**, Po-Hsin Chen and Martin Peckerar, University of Maryland, Taiwan

4:15 p.m. **A 10-bit 310μW 2MSPS Charge Redistributed D/A Converter**, Hyukbin Kwon, Hyosang Kim, Seunghoon Kim, Junho Moon, and Minkyu Song, Dongguk University, Korea

4:25 p.m. **Investigating the Linearity of MOSFET-only Switched-capacitor Delta-sigma Modulators Under Low-voltage Condition**, Farhad Alibeygi Parsan, Ahmad Ayatollahi, Adib Abrishamifar, Iran

4:35 p.m. **Closing Remarks**

4:50 p.m. – 5:50 p.m. **Workshops J, K, L**

5:50 p.m. **Adjourn**