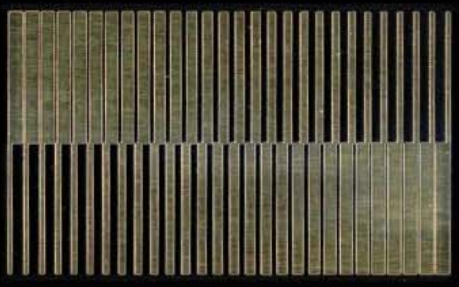

IEEE EDS

IEEE Electron Device Society
Central Texas Chapter
Austin, Texas

In Recognition and Appreciation as

2009 IEEE Electron Device Invited Speaker

Prof. Morris Ker

IEEE

IEEE Electron Device Chapter, Central Texas Section

Meeting Notice

May 21 2009 Presentation: EDS Distinguish Lecturer

Topic: ESD Protection Design for CMOS Mixed-Voltage I/O Circuits

Speaker: Prof. Morris (Ming-Dou) Ker, *IEEE Fellow*
Dept. of Electronic Engineering, I-Shou University,
Kaohsiung, Taiwan.

Abstract:

To improve circuit operating speed and performance, the device dimension of MOSFET has been shrunk in the advanced CMOS integrated circuits (ICs). With the scaled-down device dimension and thin gate oxide in the advanced nanoscale CMOS technology, the power supply voltage of normal circuit operation is also scaled down to reduce the power consumption and to meet the gate-oxide reliability. However, most microelectronic systems nowadays still consist of the semiconductor chips fabricated in different CMOS technologies. Therefore, the microelectronic systems often require the I/O interface circuits between semiconductor chips or sub-systems which have different power supply voltages. With the different power supply voltages in a microelectronic system, chip-to-chip I/O circuits must be designed to avoid electrical overstress across the gate oxide, to avoid hot-carrier degradation on the output devices, and to prevent the undesired leakage current paths between the chips. Therefore, some advanced mixed-voltage I/O circuits had been developed to handle the I/O signals of higher voltage level but only realized with low-voltage CMOS devices. However, except the different voltage levels of I/O signals in the mixed-voltage I/O circuits, such mixed-voltage I/O circuits connected to the bonding pad in CMOS ICs are still requested to meet the electrostatic discharge (ESD) specifications in IC industry. For safe production of CMOS ICs, the ESD robustness for commercial IC products was traditionally requested to sustain ESD levels of ±2kV in the test standard of Human Body Model (HBM). How to design the on-chip ESD protection circuits to effectively protect the mixed-voltage I/O

circuits realized by the nanoscale CMOS devices with thin gate oxide is a quite difficult challenge. Such on-chip ESD protection circuits for mixed-voltage I/O circuits should meet the gate-oxide reliability constraints and prevent the undesired leakage current paths during normal circuit operating condition. Under ESD zapping condition, the ESD protection circuit should be quickly triggered on to discharge ESD current. In this tutorial, a brief introduction to the mixed-voltage I/O circuits will be shown, and then an overview on the ESD protection designs for mixed-voltage I/O circuits without using the additional thick gate-oxide process is presented. Some advanced ESD protection designs by using high-voltage-tolerant power-rail ESD clamp circuits to protect mixed-voltage I/O circuits will be demonstrated with silicon verification in nanoscale CMOS technology. ESD protection for CMOS ICs is not only the process issue but also highly dependent to the design issue. On-chip ESD protection design is an important topic that the circuit designers need to watch.

Meeting Date: 5/21/09
Meeting time: 6:00-7:30PM
Meeting Location: Rio Grande Conference room at SVTC

Map: http://www.sematech.org/corporate/map.htm

Refreshments: 6:00-6:30PM

Please RSVP to Christian Catalan at Christian.Catalan@amd.com. We need accurate count to purchase refreshments.