



Presents to

**Prof. Ming-Dou Ker**

in Appreciation of Your Contribution as

An Invited Speaker

at the Semiconductor Manufacturing Forum 2009

November 20, 2009

**TY Wu, President**

Taiwan Semiconductor Industry Association



**Prof. Ming-Dou Ker**

IEEE Fellow

Dept. of Electronic Engineering,  
I-Shou University, Kaohsiung, Taiwan. .

Wednesday, October 27, 2009

Dear Prof. Ker:

Re: Invited Speech at Semiconductor Manufacturing Forum 2009

The Organizing Committee of Semiconductor Manufacturing Forum 2009 cordially invites your presence to deliver the Invited Speech at the Semiconductor Manufacturing Forum 2009 in Hsin Chu , Taiwan on November 19-20, 2009.

The Semiconductor Manufacturing Forum 2009 is organized by Taiwan Semiconductor Industry Association (TSIA) and opens to anyone who is interested in the topics.

Your presentation file will be converted to PDF format and posted at the event website for attendees' reference and download from 11/24 to 12/1, please provide a soft copy of your presentation in PowerPoint format no later than November 6, 2009. The Forum is a public meeting open to anyone who is interested in the topics. Please note that the material you submit must NOT be confidential. You will have 40 minutes for your presentation and your speech is scheduled at **9:40 - 10:20 AM November 20, 2009**; this includes both the presentation itself and the Question & Answer period.

The Forum is arranged at National Chiao Tung University Library International Conference Hall Room A  
(交通大學浩然國際會議廳 A 廳，新竹市大學路 1001 號)

Again, the Organizing Committee sincerely thanks you for agreeing to deliver the speech.

Sincerely yours,

YB Hsu, Chair of Technology Committee, TSIA

# **Invited Speech in Semiconductor Manufacturing Forum 2009**

## **1. Title of Talk :**

### **Charged-Device-Model (CDM) ESD Protection in CMOS Integrated Circuits**

Speaker: Prof. **Ming-Dou Ker** (柯明道), **IEEE FELLOW**

Dept. of Electronic Engineering, I-Shou University (義守大學), Kaohsiung, Taiwan.

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## **2. Abstract:**

The impacts of charged-device-model (CDM) electrostatic discharge (ESD) events on CMOS integrated circuit (IC) products are presented. The mechanism of chip-level CDM ESD event is introduced with some case studies on CDM ESD damages. Besides the chip-level CDM ESD event, the board-level CDM ESD event, which had been reported to cause damages in many customer-returned ICs, is also investigated in this talk. The chip-level and board-level CDM ESD levels of several test devices and test circuits fabricated in CMOS processes are characterized and compared. The experimental results have shown that the board-level CDM ESD level of the test circuit is much lower than the chip-level CDM ESD level, which indicates that the board-level CDM ESD test is more critical than the chip-level CDM ESD test in the field applications. In the nanoscale CMOS processes, the gate-oxide becomes thinner, which degrades the CDM ESD robustness of CMOS ICs. In high-speed or radio-frequency (RF) applications, large ESD protection devices can not be applied to the I/O pad due to the limitation on parasitic capacitance, which further increases the difficulty on CDM ESD protection design. Moreover, the die size becomes larger in SoC applications, which indicates that more charges can be stored in the substrate of chip. Consequently, CDM ESD issues, including chip-level and board-level CDM ESD events, will become more critical to the ICs products fabricated by nanoscale CMOS processes. How to design effective ESD protection against CDM ESD events is a quite difficult challenge to ICs products in nanoscale CMOS processes. On-chip ESD protection design is an important topic that the process, device, product, reliability, and circuit engineers have to watch.

### 3. Biography of Speaker:



**Ming-Dou Ker** (柯明道) received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1993.

He was ever worked as the Department Manager in the VLSI Design Division of the Computer and Communication Research Laboratories (CCL), Industrial Technology Research Institute (ITRI), Taiwan. Since 2004, he has been a Full Professor in the Department of Electronics Engineering, National Chiao-Tung University, Taiwan. During 2006 – 2008, he also served as the *Director of Master Degree Program* in the College of Electrical

Engineering and Computer Science, National Chiao-Tung University; as well as the *Associate Executive Director* of National Science and Technology Program on System-on-Chip (NSoC), Taiwan. In 2008, he was rotated to I-Shou University, Kaohsiung, Taiwan, as Chair Professor and Vice President. In the field of reliability and quality design for circuits and systems in CMOS technology, he has published over 370 technical papers in international journals and conferences. He has proposed many inventions to improve reliability and quality of integrated circuits, which have been granted with 150 U.S. patents and 145 Taiwan patents. Prof. Ker had been invited to teach or to consult reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC Industry. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent prosthesis.

Prof. Ker has served as member of the Technical Program Committee and Session Chair of numerous international conferences. He was selected as the *Distinguished Lecturer* in IEEE Circuits and Systems Society for 2006-2007, and in IEEE Electron Devices Society since 2008. He ever served as Associate Editor in *IEEE Trans. on VLSI Systems*. He was the President of Foundation in *Taiwan ESD Association*. In 2008, Prof. Ker was elevated as an *IEEE Fellow* with the citation of “*for contributions to electrostatic protection in integrated circuits, and performance optimization of VLSI micro-systems*”. In 2009, Prof. Ker was awarded as one of the top ten Distinguished Inventors in Taiwan, and also selected as one of top hundred Distinguished Inventors in China.