重庆大学 CHONGQING UNIVERSITY 光电工程学院 College of Optoelectronic Engineering

重庆大学光电工程学院
邀 请 函

尊敬的柯明道教授/ 義守大學研究副校長：

真诚邀请您来重庆大学传授设计经验，点拨集成电路设计中的疑难问题，讲解 ESD 抗静电保护设计和工艺技术课程。

1.讲课时间：2010 年 9 月 1 日至 2010 年 9 月 3 日。

2.重庆大学提供您往返台湾的机票费及酒店住宿费等。

重庆大学光电工程学院

2010-8-12

邀请人：重庆大学光电工程学院副院长 魏彪

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Prof. Ker's ESD Tutorial Course in
重庆大学 and 中国电子科技集团第二十四研究所

1. Title of Tutorial Course (课程名称):

先进 CMOS 集成电路 ESD 保护设计

(Advanced ESD Protection Design in CMOS Integrated Circuits)

Speaker: Prof. **Ming-Dou Ker** (柯明道), *IEEE FELLOW*

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Institute of Electronics, National Chiao-Tung University (交通大學), Hsinchu, Taiwan.

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2. Abstract (课程简介) :

As the increase of applications with more integrated circuits (ICs) products in our life, the reliability of IC products has become one of the most important issues. To reduce the weight of electronic products, to integrate more functions into the electronic products, as well as to reduce the power consumption of electronic products, the CMOS technology has been developed into nanometer scale to realize VLSI/SoC for electronic systems. With the transistors in the nano-scale dimension, the gate-oxide thickness of MOSFET is only 10~15Å for operating with sub-1V power supply. Such thinner gate oxide is very easily ruptured by electrostatic discharge (ESD) events, which frequently happen in our environments with the voltage level of hundreds or even thousands volts. The electronics products are typically weaker to sustain such ESD stresses during the assembly, testing, package, and the applications.

To verify the reliability and quality of IC products to ESD robustness for safe applications, there are already some industry ESD standards developed, such as Human Body Model (HBM) and Charged Device Model (CDM), to verify the ESD robustness of IC products. Typically, for safe production of ICs, the ESD robustness for commercial IC products has been requested to sustain the ESD levels of ±2kV in the HBM ESD test and ±1kV in the CDM ESD test. Besides, in the IEC 6100-4-2 standard, the electronic products are zapped by the ESD gun with ESD voltage of up to 15kV in the air-discharge mode. How to design the on-chip ESD protection circuits to effectively protect the integrated circuits realized by the nano-scale CMOS devices with very thin gate oxide is a quite difficult challenge to IC industry. The on-chip ESD protection circuit must be included in the beginning of chip design phase, and the ESD robustness must be verified among the IC products those will be used in all microelectronics systems. In the SoC, the power pins to

support many circuit blocks in a single chip are often separated into a lot of power domains or groups. With those separated power domains, the interface circuits between the circuit blocks are also often damaged by the ESD stresses zapping on the input, output, or power pins to cause the internal ESD failures beyond the I/O circuits. Such internal ESD damages are quite trouble to be fixed when the microelectronics systems become more complex or bigger.

To improve circuit operating speed and performance, the device dimension of MOSFET has been shrunk in the advanced CMOS integrated circuits (ICs). With the scaled-down device dimension and thin gate oxide in the advanced nanoscale CMOS technology, the power supply voltage of normal circuit operation is also scaled down to reduce the power consumption and to meet the gate-oxide reliability. However, most microelectronic systems nowadays still consist of the semiconductor chips fabricated in different CMOS technologies. Therefore, the microelectronic systems often require the I/O interface circuits between semiconductor chips or sub-systems which have different power supply voltages. With the different power supply voltages in a microelectronic system, chip-to-chip I/O circuits must be designed to avoid electrical overstress across the gate oxide, to avoid hot-carrier degradation on the output devices, and to prevent the undesired leakage current paths between the chips. Therefore, some advanced mixed-voltage I/O circuits had been developed to handle the I/O signals of higher voltage level but only realized with low-voltage CMOS devices. Besides the different voltage levels of I/O signals in the mixed-voltage I/O circuits, such mixed-voltage I/O circuits connected to the bonding pad in CMOS ICs are still requested to meet the electrostatic discharge (ESD) specifications in IC industry. For safe production of CMOS ICs, the ESD robustness for commercial IC products was traditionally requested to sustain ESD levels of ±2kV in the test standard of Human Body Model (HBM). How to design the on-chip ESD protection circuits to effectively protect the mixed-voltage I/O circuits realized by the nanoscale CMOS devices with thin gate oxide is a quite difficult challenge. Such on-chip ESD protection circuits for mixed-voltage I/O circuits should meet the gate-oxide reliability constraints and prevent the undesired leakage current paths during normal circuit operating condition. Under ESD zapping condition, the ESD protection circuit should be quickly triggered on to discharge ESD current.

In this Tutorial Course (three days), an introduction on ESD issue and standards to IC products is presented with some failure analysis pictures to demonstrate the impact of ESD on IC products. The basic design concept for on-chip ESD protection circuit will be presented. Some state-of-the-art ESD protection techniques, gate-driven design and substrate- triggered design, will be shown with real circuit implementations in I/O circuits of ICs. ESD protection for CMOS ICs is not only the process issue but stronger dependent to the design issue, which has been an important topic that the circuit designers must to watch. After the basic ESD protection introduction, the advanced ESD protection design will be provided, which are very helpful to the IC industry and academic researches. The system-level ESD issue is added into this talk. Besides the ESD topic, the transient-induced

latchup issue is also introduced in this course. ESD protection for CMOS ICs is not only the process issue but also highly dependent to the design issue. I/O circuits and the corresponding ESD protection designs have become important reliability issues in nanoscale CMOS IC products, wherefore the circuit designers need to watch.

3. Outlines of Course (课程大纲) :

1. **Introduction to ESD (Electrostatic Discharge).**
2. **Industrial ESD Standards and Transmission Line Pulse (TLP).**
3. **Basic On-Chip ESD Protection Concept.**
4. **Process and Layout Issues on ESD Robustness of CMOS ICs.**
5. **Circuit Techniques for On-Chip ESD Protection Design.**
6. **ESD Protection Design with SCR Devices.**
7. **Whole-Chip ESD Protection Scheme (Power-Rail ESD Clamp Circuit).**
8. **Whole-Chip ESD Protection Scheme (ESD Protection for Integrated Circuits with separated power domains).**
9. **ESD Protection Design for Mixed-Voltage I/O Circuits.**
10. **System Level ESD Protection Design in CMOS ICs.**
11. **Transient-Induced Latchup in CMOS ICs.**

4. Biography of Speaker:

Ming-Dou Ker (柯明道) received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1993.

He was worked as the Department Manager with the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. Since 2004, he has been a Full Professor with the Nanoelectronics and Gigascale Systems Laboratory, Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan. From 2008, he was rotated to be Chair Professor (講座教授) and Vice President (研究副校長) of I-Shou University, Kaohsiung, Taiwan. Now, he has been the Distinguished Professor in the Department of Electronics Engineering, National Chiao-Tung University, and also serves as the Executive Director of National Science and Technology Program on System-on-Chip (NSoC) in Taiwan. In the technical field of reliability and quality design for microelectronic circuits and systems, he has published over 400 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability and quality of integrated circuits, which have been granted with 165 U.S. patents and 148 Taiwan patents. He had been invited to teach and/or to consult the reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC industry. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent prosthesis.

Prof. Ker has served as a member of the Technical Program Committee and the Session Chair of numerous international conferences for many years. He ever served as the Associate Editor for the *IEEE TRANSACTIONS ON VLSI SYSTEMS*, 2006-2007. He was selected as the *Distinguished Lecturer* in the IEEE Circuits and Systems Society (2006–2007) and in the IEEE Electron Devices Society (2008-2010). He was the President of Foundation in Taiwan ESD Association. In 2008, he has been elevated as an ***IEEE Fellow*** “for his contributions to the electrostatic protection in integrated circuits and the performance optimization of VLSI Microsystems”. In 2009, he was awarded as one of the top ten Distinguished Inventors in Taiwan; and one of the top hundred Distinguished Inventors in China.