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柯明道教授惠鑒：

非常高興能邀請您到本系演講，這是本系極大的榮幸。謹附上有關的演講資料：

時間：11 月 29 日 (星期一) 下午二時

講題：Advanced On-Chip ESD Protection Design in CMOS Integrated Circuits(積體電路晶片之靜電放電防護設計技術)

地點：IB-101

若有任何不妥之處，請來電告知吳育欣(02-2730-3258)，俾利訂正。我們將備有電腦及投影設備，若您有其他需要，也請告知以便準備。最後我們誠摯的盼望您的蒞臨與指導，耑此敬頌

時　祺

系主任 陳省隆 敬啟

2010 年 8 月 9 日

備註：

一、 如須郵寄此紙本邀請函，敬請告知。

Prof. Ker's ESD Talk in
National Taiwan University of Science & Technology

1. Title of Talk:

積體電路之靜電放電防護設計技術
(Advanced ESD Protection Design in CMOS Integrated Circuits)

Speaker: Prof. **Ming-Dou Ker** (柯明道), *IEEE FELLOW*

(1) Distinguished Professor,
Institute of Electronics, National Chiao-Tung University (交通大學), Hsinchu, Taiwan.

(2) Chair Professor and Vice President,
Dept. of Electronic Engineering, I-Shou University (義守大學), Kaohsiung, Taiwan.
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2. Abstract:

As the increase of applications with more integrated circuits (ICs) products in our life, the reliability of IC products has become one of the most important issues. To reduce the weight of electronic products, to integrate more functions into the electronic products, as well as to reduce the power consumption of electronic products, the CMOS technology has been developed into nanometer scale to realize VLSI/SoC for electronic systems. With the transistors in the nano-scale dimension, the gate-oxide thickness of MOSFET is only 10~15Å for operating with sub-1V power supply. Such thinner gate oxide is very easily ruptured by electrostatic discharge (ESD) events, which frequently happen in our environments with the voltage level of hundreds or even thousands volts. The electronics products are typically weaker to sustain such ESD stresses during the assembly, testing, package, and the applications.

To verify the reliability and quality of IC products to ESD robustness for safe applications, there are already some industry ESD standards developed, such as Human Body Model (HBM) and Charged Device Model (CDM), to verify the ESD robustness of IC products. Typically, for safe production of ICs, the ESD robustness for commercial IC products has been requested to sustain the ESD levels of ±2kV in the HBM ESD test and ±1kV in the CDM ESD test. Besides, in the IEC 6100-4-2 standard, the electronic products are zapped by the ESD gun with ESD voltage of up to 15kV in the air-discharge mode. How to design the on-chip ESD protection circuits to effectively protect the integrated circuits realized by the nano-scale CMOS devices with very thin gate oxide is a quite difficult challenge to IC industry. The on-chip ESD protection circuit must be included in the beginning of chip design phase, and the ESD robustness must be verified among the IC products those will be used in all microelectronics systems. In the SoC, the power pins to support many circuit blocks in a single chip are often separated into a lot of power domains

or groups. With those separated power domains, the interface circuits between the circuit blocks are also often damaged by the ESD stresses zapping on the input, output, or power pins to cause the internal ESD failures beyond the I/O circuits. Such internal ESD damages are quite trouble to be fixed when the microelectronics systems become more complex or bigger.

In this Talk, an introduction on ESD issue and standards to IC products is presented with some failure analysis pictures to demonstrate the impact of ESD on IC products. The basic design concept for on-chip ESD protection circuit will be presented. Some state-of-the-art ESD protection techniques, gate-driven design and substrate-triggered design, will be shown with real circuit implementations in I/O circuits of ICs. ESD protection for CMOS ICs is not only the process issue but stronger dependent to the design issue, which has been an important topic that the circuit designers must to watch. After the basic ESD protection introduction, the system-level ESD protection will be presented, which are very helpful to the IC industry and academic researches. ESD protection for CMOS ICs is not only the process issue but also highly dependent to the design issue. I/O circuits and the corresponding ESD protection designs have become important reliability issues in nanoscale CMOS IC products, wherefore the circuit designers have to watch.

3. Outlines of Talk:

1. **ESD Events and ESD Models (Standards) in IC Industry.**
2. **On-Chip ESD Protection Design.**
3. **System-Level ESD Protection.**

4. Biography of Speaker:

Ming-Dou Ker (柯明道) received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1993.

He was ever worked as the Department Manager with the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. Since 2004, he has been a Full Professor with the Nanoelectronics and Gigascale Systems Laboratory, Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan. From 2008, he was rotated to be Chair Professor (講座教授) and Vice President (研究副校長) of I-Shou University, Kaohsiung, Taiwan. Now, he has been the Distinguished Professor (特聘教授) in the Department of Electronics Engineering, National Chiao-Tung University, and also serves as the Executive Director (執行長) of National Science and Technology Program on System-on-Chip (NSoC) in Taiwan (晶片系統國家型科技計畫). In the technical field of reliability and quality design for microelectronic circuits and systems, he has published over 400 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability and quality of integrated circuits, which have been granted with 172 U.S. patents and 148 Taiwan patents. He had been invited to teach and/or to consult the reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC industry. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent prosthesis.

Prof. Ker has served as a member of the Technical Program Committee and the Session Chair of numerous international conferences for many years. He ever served as the Associate Editor for the *IEEE TRANSACTIONS ON VLSI SYSTEMS*, 2006-2007. He was selected as the *Distinguished Lecturer* in the IEEE Circuits and Systems Society (2006–2007) and in the IEEE Electron Devices Society (2008-2010). He was the President of Foundation in Taiwan ESD Association. In 2008, he has been elevated as an ***IEEE Fellow*** “for his contributions to the electrostatic protection in integrated circuits and the performance optimization of VLSI Microsystems”. In 2009, he was awarded as one of the top ten Distinguished Inventors in Taiwan (台灣十大傑出發明家).

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義守大學網址: http://www.isu.edu.tw/pages/vicepresident_research.htm

Invited Talk in
National Taiwan University of Science & Technology

積體電路之靜電放電防護設計技術
(Advanced ESD Protection Design in CMOS Integrated Circuits)

Prof. Ming-Dou Ker (柯明道教授), *IEEE FELLOW*

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Outlines

1. ESD Events and ESD Models (Standards) in IC Industry.
2. On-Chip ESD Protection Design.
3. System-Level ESD Protection.

ESD = Electrostatic Discharge

⇨ The discharge current generated from the static charges often burned out the junction, contact, gate oxide, and even the metal lines in CMOS integrated circuits.