MEDIATEK

柯明道　研究副校長,您好:

謹代表聯發科技(股)公司 誠摯邀請您撥冗蒞臨本公司演講。

冀祈借重您在積體電路靜電放電防護技術領域多年研究之專精知識和豐富經驗，提供公司同仁最新的資訊與解惑。

在此，先向您說明此次演講課程安排：

演講時間：4 月 7 日(週四) 上午 10:00-12:00

聽講對象：聯發科技同仁

演講地點：聯發科技新竹總部二樓教育訓練教室

期待您的蒞臨演講及回覆，謝謝。

順頌　時祺

高崇武 2011.3.23

_____敬邀

演講摘要(@聯發科技, April 7, 2011)

1. Title of Talk:

ESD Protection: System-Level ESD Test vs. Chip-Level ESD Test

Speaker: Prof. **Ming-Dou Ker** (柯明道), *IEEE FELLOW*

(1) Distinguished Professor (特聘教授),
Institute of Electronics, National Chiao-Tung University (交通大學), Hsinchu, Taiwan.

(2) Chair Professor and Vice President (研究副校長),
Dept. of Electronic Engineering, I-Shou University (義守大學), Kaohsiung, Taiwan.
e-mail: mdker@ieee.org

2. Abstract:

The reliability of IC products has become one of major competitive issues in IC industry. Especially, the electrostatic discharge (ESD) events frequently cause the damage and/or malfunction in the microelectronics products. When the CMOS technology developed into nano-scale era, the gate-oxide thickness of MOSFET is only 10~15Å for operating with sub-1V power supply. Such thinner gate oxide is very easily ruptured by electrostatic discharge (ESD) events, which frequently happen in our environments with the voltage level of hundreds or even thousands volts. How to design the on-chip ESD protection circuits to effectively protect the integrated circuits realized by the nano-scale CMOS devices with thin gate oxide is a quite difficult challenge to IC industry.

To verify the ESD robustness of IC products in chip level, there are already some industry ESD standards developed, such as Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM). Typically, the ESD robustness for commercial IC products has been requested to sustain the ESD levels of ±2kV in the HBM ESD test, ±200V in the MM ESD test, and ±1kV in the CDM ESD test. Besides, when the ICs are inserted into a microelectronic products (such as cellular phone or a notebook), the microelectronic products are verified by the system-level ESD test with the IEC 61000-4-2 standard. In system-level ESD test, the microelectronic products are zapped by the ESD gun with ESD voltage of up to 8kV in the contact-discharge mode and 15kV in the air-discharge mode (for the specification of level 4). As comparing to these two main ESD tests (chip-level ESD test vs. system-level ESD test), the testing conditions and testing standards are totally different. But, the customers are often unclear to understand the big difference between these two ESD testing conditions. Therefore, the IC design houses were gotten the request to provide the system-level ESD specification in the chip-level ESD protection design. Recently, some ESD equipment providers even co-worked together to come out one new standard, Human Metal Model (HMM), in which the ESD gun of IEC 61000-4-2 standard is used to zap the metal trace on the PCB module that directly connected to the pins of ICs.

In summary, there are totally five ESD testing standards publicly announced in the IC industry, but the testing conditions and the ESD energy / specifications are quite different among them. In this talk, a whole view to well understand these five ESD tests is clearly presented. The useful solutions to overcome the different ESD test standards in the chip level, the board level, and the system level are suggested. Moreover, some ESD questions collected in advance from AE and customers will be answered.

3. Biography of Speaker:

Ming-Dou Ker (柯明道) received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1993.

He was ever worked as the Department Manager with the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. Since 2004, he has been a Full Professor with the Nanoelectronics and Gigascale Systems Laboratory, Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan. From 2008, he was rotated to be Chair Professor (講座教授) and Vice President (研究副校長) of I-Shou University, Kaohsiung, Taiwan. Now, he has been the Distinguished Professor (特聘教授) in the Department of Electronics Engineering, National Chiao-Tung University. He also serves as the Executive Director (執行長) of National Science and Technology Program on System-on-Chip (NSoC) in Taiwan (晶片系統國家型科技計畫) for 2010 ~ 2011; and also as the Executive Director (執行長) of National Science and Technology Program on Nano Technology (NPNT) in Taiwan (奈米國家型科技計畫) for 2011 ~ 2014. In the technical field of reliability and quality design for microelectronic circuits and systems, he has published over 400 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability and quality of integrated circuits, which have been granted with 179 U.S. patents and 153 Taiwan patents. He had been invited to teach and/or to consult the reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC industry. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent prosthesis.

Prof. Ker has served as a member of the Technical Program Committee and the Session Chair of numerous international conferences for many years. He ever served as the Associate Editor for the *IEEE TRANSACTIONS ON VLSI SYSTEMS*, 2006-2007. He was selected as the *Distinguished Lecturer* in the IEEE Circuits and Systems Society (2006–2007) and in the IEEE Electron Devices Society (2008-2011). He was the President of Foundation in Taiwan ESD Association. In 2008, he has been elevated as an ***IEEE Fellow*** “for his contributions to the electrostatic protection in integrated circuits and the performance optimization of VLSI Microsystems”. In 2009, he was awarded as one of the top ten Distinguished Inventors in Taiwan (台灣十大傑出發明家).

Invited Talk @聯發科技

ESD Protection: System-Level ESD Test vs. Chip-Level ESD Test

Prof. Ming-Dou Ker (柯明道教授), *IEEE FELLOW*

(1) Dept. of Electronics Engineering / Institute of Electronics, National Chiao-Tung University (交通大學), Hsinchu, Taiwan.

(2) Dept. of Electronic Engineering, I-Shou University (義守大學), Kaohsiung, Taiwan.

E-mail: *mdker@ieee.org*

April 7, 2011

Outlines

1. ESD Events and ESD Models (Standards) in IC Industry.
2. Chip-Level ESD Protection.
3. System-Level ESD Protection.