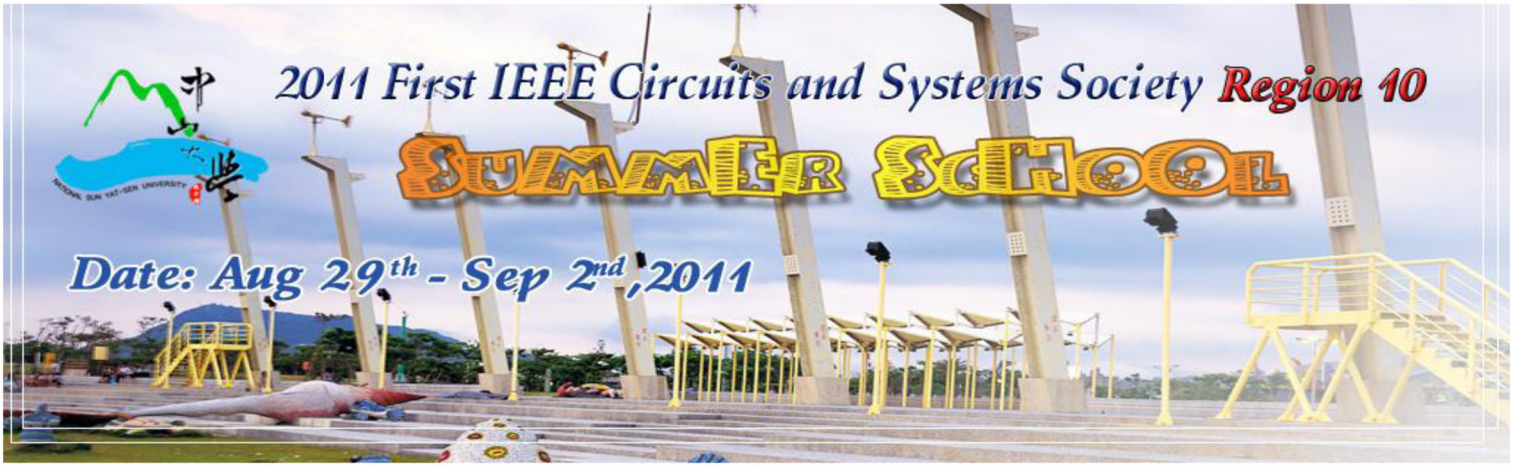

【2011 Summer School Background】

Since the circuit design has been widely recognized as the bed stone of emerging systems and new technology, it is an opportunity for IEEE Circuits and Systems (CASS) to introduce the basics and trends to those students who are interested in devoting their career in this area. This summer school is then encouraged and sponsored by IEEE CASS to carry out this mission. The first IEEE CASS Summer School aims to provide both an objective and clear overview and an in-depth analysis of the state-of-the-art research on a variety of circuit, architecture, and system designs. The lectures will be delivered by distinguished experts in these fields. The summer school also plays the role as a plat form for students, early-stage researchers and young scholars to get acquaintance with the experts who have been renowned for what they have achieved.

Dates: Aug. 29 – Sep. 2, 2011
Location: F6019, Dept. of EE, National Sun Yat-Sen University, Kaohsiung, Taiwan
Registration Fee: 100 USD or 3000 NTD (It will be fully refunded if the registered attendee sits in all 8 lectures.)
Registration website: **http://vlsi.ee.nsysu.edu.tw/sschool_2011**
Deadline: Aug. 20, 2011

❖ Organizing Co-Chairs

- **Chua-Ching Wang**
  National Sun Yat-Sen University
- **Rui Martins**
  University of Macau
- **Shyh-Jye Jou**
  National Chiao Tung University
- **Chung-Ho Chen**
  National Cheng Kung University

❖ Organizing Committees

- **Tong-Yu Hsieh**
  National Sun Yat-Sen University
- **Pui-In Mak**
  University of Macau
- **Soon-Jyh Chang**
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2011 IEEE CASS Summer School Region 10 Agenda

Date / Time	08/29 (Mon)	08/30 (Tue)	08/31 (Wed)	09/01 (Thu)	09/02 (Fri)
09h00 12h00	Pui-In Mak / Macao University, Macao	Katherine Shu-Ming Li / National Sun Yat-Sen University, Taiwan	Tours to NXP Semiconductors Taiwan Ltd.	Zhiyi Yu / Fudan University, China	Gwo Giun (Chris) Lee / National Cheng Kung University, Taiwan
Topic	High-/Mixed-Voltage Analog and RF Circuit Techniques for Nanoscale CMOS	Algorithm/Architecture Co-Design for Multiple Scan Trees and Physical Designs		High Performance and Energy-Efficient Many-core Processors for Domain Specific Applications	Algorithm/Architecture Co-Design for Signal Processing Systems
Session Chair	Chua-Chin Wang	Tzung-Je Lee		Tong-Yu Hsieh	Tong-Yu Hsieh
12h00 13h30	Lunch	Lunch	No Lunch	Lunch	Lunch
13h30 16h30	Ming-Dou Ker / National Chiao Tung University, Taiwan	Robert Rieger/ National Sun Yat-Sen University, Taiwan		Ke-Horng Chen / National Chiao Tung University, Taiwan	Donald Lie / Texas Tech University, USA
Topic	On-Chip ESD Protection Design in CMOS Integrated Circuits	Integrated Circuit Design for Low-power Biomedical Application		Embedded Power Management in System-on-a-chip (Soc) Applications Fabricated by Nano-meter Process	Design of High-Efficiency Si-Based Power Amplifier and Transmitters ICs for Mobile Broadband Wireless Communications
Session Chair	Katherine Shu-Ming Li	Katherine Shu-Ming Li		Tzung-Je Lee	Chua-Chin Wang

Note: Lunch will be served.

For detailed information, please visit the conference website:
http://vlsi.ee.nsysu.edu.tw/sschool_2011

Co-Sponsors

Prof. **Ming-Dou Ker**

School **National Chiao Tung University**

Topic **On-Chip ESD Protection Design in CMOS Integrated Circuits**

Time 13h30
16h30

Biography **Ming-Dou Ker** received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1993.
He ever worked as the Department Manager with the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. Since 2004, he has been a Full Professor with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan. From 2008, he was rotated to be Chair Professor and Vice President of I-Shou University, Kaohsiung, Taiwan. Now, he has been the Distinguished Professor in the Department of Electronics Engineering, National Chiao-Tung University, Taiwan. He ever served as the Executive Director of National Science and Technology Program on System-on-Chip (NSoC) in Taiwan during 2010 ~ 2011; and now as the Executive Director of National Science and Technology Program on Nano Technology (NPNT) in Taiwan during 2011 ~ 2014. In the technical field of reliability and quality design for microelectronic circuits and systems, he has published over 400 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability and quality of integrated circuits, which have been granted with 181 U.S. patents and 157 Taiwan patents. He had been invited to teach and/or to consult the reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC industry. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent prosthesis.

Prof. Ker has served as a member of the Technical Program Committee and the Session Chair of numerous international conferences for many years. He ever served as the Associate Editor for the *IEEE Transactions on VLSI Systems*, 2006-2007. He was selected as the *Distinguished Lecturer* in the IEEE Circuits and Systems Society (2006–2007) and in the IEEE Electron Devices Society (2008-present). He was the President of Foundation in Taiwan ESD Association. In 2008, he has been an ***IEEE Fellow*** "for his contributions to the electrostatic protection in integrated circuits and the performance optimization of VLSI Microsystems". In 2009, he was awarded as one of the top ten Distinguished Inventors in Taiwan.

Abstract As the increase of applications with more integrated circuits (ICs) products in our life, the reliability of IC products has become one of the most important issues. To reduce the weight of electronic products, to integrate more functions into the electronic products, as well as to reduce the power consumption of electronic products, the CMOS technology has been developed into nanometer scale to realize VLSI/SoC for electronic systems. With the transistors in the nano-scale dimension, the gate-oxide thickness of MOSFET is only 10~15A for operating with sub-1V power supply. Such thinner gate oxide is very easily ruptured by electrostatic discharge (ESD) events, which frequently happen in our environments with the voltage level of hundreds or even thousands volts. The electronics products are typically weaker to sustain such ESD stresses during the assembly, testing, package, and the applications.

To verify the reliability and quality of IC products to ESD robustness for safe applications, there are already some industry ESD standards developed, such as Human Body Model (HBM) and Charged Device Model (CDM), to verify the ESD robustness of IC products. Typically, for safe production of ICs, the ESD robustness for commercial IC products has been requested to sustain the ESD levels of ±2kV in the HBM ESD test and ±1kV in the CDM ESD test. Besides, in the IEC 6100-4-2 standard, the electronic products are zapped by the ESD gun with ESD voltage of up to 15kV in the air-discharge mode. How to design the on-chip ESD protection circuits to effectively protect the integrated circuits realized by the nano-scale CMOS devices is a quite difficult challenge to IC industry. The on-chip ESD protection circuit must be included in the beginning phase of chip design.

In this Talk, an introduction on ESD issue and standards to IC products is presented with some failure analysis pictures to demonstrate the impact of ESD on IC products. The basic design concept for on-chip ESD protection circuit will be presented. Some state-of-the-art ESD protection techniques, gate-driven design and substrate-triggered design, will be shown with real circuit implementations in I/O circuits of ICs. After the basic ESD protection introduction, the system-level ESD protection will be presented. ESD protection for CMOS ICs is not only the process issue but also highly dependent to the design issue. I/O circuits and the corresponding ESD protection designs have become important reliability issues in nanoscale CMOS IC products, which has been an important topic that the IC designers need to know.

Session Chair : Katherine Shu-Ming Li

Tutorial Talk for the 1st IEEE CASS Summer School in Region 10

On-Chip ESD Protection Design in CMOS Integrated Circuits

Prof. Ming-Dou Ker (柯明道教授), *IEEE FELLOW*

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(2) Dept. of Electronic Engineering, I-Shou University (義守大學), Kaohsiung, Taiwan.

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Outlines

1. ESD Events and ESD Models (Standards) in IC Industry.
2. Chip-Level ESD Protection.
3. System-Level ESD Protection.

ESD = Electrostatic Discharge

➡ The discharge current generated from the static charges often burned out the junction, contact, gate oxide, and even the metal lines in CMOS integrated circuits.