

Design of Ultra-Low-Leakage Power-Rail ESD Clamp Circuits in Nanoscale CMOS Technology

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Speaker

Distinguished Professor **Morris Ker**
柯明道特聘教授

IEEE Fellow

Institute of Electronics, National Chiao Tung University
國立交通大學

獲頒：台灣十大傑出青年

曾任：台灣 ESD 防護協會理事長 & 義守大學副校長

2009年，台灣十大發明人



Oct. 27 (Thu)	Topic	Host & Speaker
14:00-14:05	TSMC Univ. Shuttle Program & the Technical Forum	Director Bing Sheu
14:05-14:10	Speaker Introduction	Deputy Director Ming-Hsiang Sung
14:10-15:20	Ultra-Low-Leakage Power-Rail ESD Clamp Circuits	Professor Morris Ker
15:20-16:00	Q&A, and Discussions	All

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主辦單位 Host: RD/DTP University Program

Design of Ultra-Low-Leakage Power-Rail ESD Clamp Circuits in Nanoscale CMOS Technology

Prof. Morris (Ming-Dou) Ker / 柯明道教授^{1, 2}

¹ Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.
(交通大學 電子研究所 特聘教授)

² Dept. of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan.
(義守大學 電子工程學系 講座教授)

Outline

- Standards of ESD Testing
- On-Chip ESD Protection Design with Active Power-Rail ESD Clamp Circuit
- Low-Leakage Power-Rail ESD Clamp Circuits
- Summary

Prof. Ker's Talk in TSMC RD & DTP Technical Forum

1. Title of Talk:

Design of Ultra-Low-Leakage Power-Rail ESD Clamp Circuits in Nanoscale CMOS Technology

Speaker: Prof. Morris (Ming-Dou) Ker, *IEEE FELLOW*
Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.
e-mail: mdker@ieee.org

2. Abstract:

To verify the reliability and quality of IC products to ESD robustness for safe applications, there are already some industry ESD standards developed, such as Human Body Model (HBM) and Charged Device Model (CDM), to verify the ESD robustness of IC products. Typically, for safe production of ICs, the ESD robustness for commercial IC products has been requested to sustain the ESD levels of $\pm 2\text{kV}$ in the HBM ESD test and $\pm 1\text{kV}$ in the CDM ESD test. Besides, in the IEC 6100-4-2 standard, the electronic products are zapped by the ESD gun with ESD voltage of up to 15kV in the air-discharge mode. How to design the on-chip ESD protection circuits to effectively protect the integrated circuits realized by the nanoscale CMOS devices is a quite difficult challenge in IC industry. The on-chip ESD protection circuit must be included in the beginning phase of chip design. On-chip ESD protection design is not only the process issue but also highly dependent to the circuit design issue.

In this talk, we focus on the design methods to reduce the leakage current in the active power-rail ESD clamp circuit. The gate tunneling effect impacts drastically in the leakage current of the traditional power-rail ESD clamp circuit realized with the RC-based ESD detection circuit in the nanoscale CMOS technology. The leakage current of the traditional power-rail ESD clamp circuit could be scaled up to several hundred microamperes, as reported in some articles that were verified in 65-nm CMOS technology. Circuit design techniques can successfully reduce the leakage current of the power-rail ESD clamp circuit to the nanoamperes (nA) order, without significant area overhead, and also without decreasing ESD robustness. The methods to reduce the leakage current among the power-rail ESD clamp circuits are reviewed in this talk, which include (1) using the thick gate oxide (dual gate-oxide process), (2) using the high-k / metal gate, (3) using the parasitic capacitance (between metal layers), (4) reducing the voltage drop across the MOS capacitor, (5) reducing the gate area of the MOS capacitor, (6) capacitor-less design, (7) using SCR (no gate structure) as main ESD clamp device.

Speaker Biography



Morris (Ming-Dou) Ker received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1993. He ever worked as the Department Manager with the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. Since 2004, he has been a Full Professor with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan. During 2008 ~ 2011, he was rotated to be Chair Professor and Vice President of I-Shou University, Kaohsiung, Taiwan. Now, he has been the Distinguished Professor in the Department of Electronics Engineering, National Chiao-Tung University, Taiwan. He ever served as the Executive Director of National Science and Technology Program on System-on-Chip (NSoC) in Taiwan during 2010 ~ 2011; and currently as the Executive Director of National Science and Technology Program on Nano Technology (NPNT) in Taiwan (2011 ~ 2014). In the technical field of reliability and quality design for microelectronic circuits and systems, he has published over 400 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability and quality of integrated circuits, which have been granted with 186 U.S. patents and 162 Taiwan patents. He had been invited to teach and/or to consult the reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC industry. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent prosthesis.

Prof. Ker has served as a member of the Technical Program Committee and the Session Chair of numerous international conferences for many years. He ever served as the Associate Editor for the *IEEE TRANSACTIONS ON VLSI SYSTEMS*, 2006-2007. He was selected as the *Distinguished Lecturer* in the IEEE Circuits and Systems Society (2006–2007) and in the IEEE Electron Devices Society (2008–present). He was the President of Foundation in Taiwan ESD Association. In 2008, he has been an *IEEE Fellow* “for his contributions to the electrostatic protection in integrated circuits and the performance optimization of VLSI Microsystems”. In 2009, he was awarded as one of the top ten Distinguished Inventors in Taiwan.