Tutorials

Tutorial 1

Professor Kaushik Roy
IEEE Fellow

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Error Resilient and Low-Energy Computing

The scaling of technology and the limitations of photolithography has led to large variations of device parameters, worse device electrostatics, increased leakage current, power density, and reduced yield. Traditional design techniques usually takes a-worst case design approach. However, such an approach may lead to very high power consumption and over-design in sub 50nm process technology. Hence, there is a need for change in design paradigm to address the above issues. In this tutorial I address various techniques (design time and run-time) to simultaneously improve power consumption and error resiliency under severe parameter variations for both logic and memory. Finally, I will present recent technology developments and approaches to energy scavenging techniques – in particular, I will focus on thermo-electric devices and solar cells.

Tutorial 2

Professor Ming-Dou Ker
IEEE Fellow

Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan

Ming-Dou Ker received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1993. He ever worked as the Department Manager with the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. Since 2004, he has been a Full Professor with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan. During 2008 ~ 2011, he was rotated to be Chair Professor and Vice President of I-Shou University, Kaohsiung, Taiwan. Now, he has been the Distinguished Professor in the Department of Electronics Engineering, National Chiao-Tung University, Taiwan. He ever served as the Executive Director of National Science and Technology Program on System-on-Chip (NSoC) in Taiwan during 2010 ~ 2011. Since 2011, he is working as the Executive Director of National Science and Technology Program on Nano Technology (NPNT) in Taiwan. In the technical field of reliability and quality design for microelectronic circuits and systems, he has published over 400 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability of integrated circuits and/or microelectronic systems, which have been granted with 185 U.S. patents and 157 Taiwan patents. He had been invited to teach and/or to consult the reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC industry. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent prosthesis. Prof. Ker has served as the member of Technical Program Committee and the Session Chair of numerous international conferences for many years. He ever served as the Associate Editor for the *IEEE Transactions on VLSI Systems*, 2006-2007. He was selected as the *Distinguished Lecturer* in the IEEE Circuits and Systems Society (2006–2007) and in the IEEE Electron Devices Society (2008-2012). He was the President of Foundation in Taiwan ESD Association. In 2008, he has been an ***IEEE Fellow*** “for the contributions to the electrostatic protection in integrated circuits and the performance optimization of VLSI Microsystems”. In 2009, he was awarded as one of the top ten Distinguished Inventors in Taiwan.

Advanced ESD Protection Design in CMOS Integrated Circuits

As the increase of applications with more integrated circuits (ICs) products in our life, the reliability of IC products has become one of the most important issues. To reduce the weight of electronic products, to integrate more functions into the electronic products, as well as to reduce the power consumption of electronic products, the CMOS technology has been continually scaled into nanometer scale to realize VLSI/SoC for microelectronic systems. With the transistors in the nano-scale dimension, the gate-oxide thickness of MOSFET is only 10~15Å for operating with sub-1V power supply. Such thinner gate oxide is very easily ruptured by electrostatic discharge (ESD) events, which frequently happen in our environments with the voltage level of hundreds or even thousands volts. The electronics products are typically weaker to sustain such ESD stresses during the assembly, testing, package, and the applications.

To verify the ESD reliability of IC products for safe applications, there are already some industry standards developed, such as Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM), to investigate the chip-level ESD robustness of IC products. Typically, for safe production of ICs, the ESD robustness for commercial IC products has been requested to sustain the ESD levels of ±2kV in the HBM ESD test and ±1kV in the CDM ESD test. Besides, in the IEC 61000-4-2 standard of system-level ESD test, the electronic products are zapped by the ESD gun with ESD voltage of up to 15kV (level 4) in the air-discharge mode. ESD protection for CMOS ICs is not only the process issue but also highly dependent to the design issue. How to design the effective ESD protection circuits to meet the ESD specifications is a quite difficult challenge, which has been an important topic that the IC designers need to know.

NANYANG TECHNOLOGICAL UNIVERSITY

Certificate of Appreciation

awarded to

Prof. Ming-Dou Ker

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for his contribution as a

Tutorial Speaker

at the

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12 – 14 December 2011, Singapore SICEC

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Tutorial Talk in
2011 International Symposium on Integrated Circuits (ISIC), Singapore.

Advanced ESD Protection Design in CMOS Integrated Circuits

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Outlines

1. ESD Models (Standards) in IC Industry.
2. Chip-Level ESD Protection Design.
3. Low-Leakage Power-Rail ESD Clamp Circuits.
4. ESD Protection in HV Process.
5. System-Level ESD Protection.

ESD = Electrostatic Discharge

➡ The discharge current generated from the static charges often burned out the junction, contact, gate oxide, and even the metal lines in CMOS integrated circuits.

International Symposium on Integrated Circuits 2011 (ISIC-2011)

Call for Papers

13 - 14 December 2011, Singapore

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The 13th International Symposium on Integrated Circuits (ISIC) dates back to 1985 and is now recognized as one of the major conferences in the highly important field of theory, design, and implementation of integrated circuits and systems. The ISIC-2011 will offer a rich program of the highest quality with distinguished invited speakers from all over the world and provide a broad forum of exchanges for researchers and IC designers.

Indeed these are exciting times in the electronic industry. New growth areas in the electronics sector are emerging. The rise in awareness of energy efficiency has led to a demand for green electronics products and energy harvesting solutions. As the developed world ages, there will be a need for faster and less invasive ways to deliver these solutions. In green electronics, for example, we can leverage on our capabilities in integrated circuit (or IC) design to develop energy-efficient solutions for applications such as computing, automotive and lighting systems.

It is important now that universities and the industries work hand in hand to create this platform to bring this progress to the next level. ISIC 2011 is focused on creating this platform to bring the academics closer with the industry. We would like to welcome you to the next ISIC 2011 in Singapore.

The Proceedings of the Symposium will be listed in the Engineering Index (EI). More information can be found at: http://www.ISIC2011.org.

High-quality contributions from prospective authors are solicited in the following topics including, but not limited to:

A. INTEGRATED CIRCUITS • Analog IC • Digital IC • Mixed-Signal IC • RF/MM-Wave IC	**B. DEVICE AND IC TECHNOLOGY** • Semiconductor Devices • Fabrication and Assembly • Testing and Yield Enhancement • Reliability and Failure Analysis
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Tentative Schedule (to be confirmed in the later date on the conference website):

Deadline for submission of special session proposals:	01 May 2011
Notification of acceptance of special session proposal:	15 May 2011
Deadline for submission of papers in Regular Sessions:	01 Jun 2011
Deadline for submission of tutorial proposals:	01 Jun 2011
Deadline for submission of papers in Special Sessions:	01 Jul 2011
Notification of paper acceptance:	01 Sep 2011
Submission of camera-ready papers:	15 Oct 2011

About Singapore:

Located at the tip of the Malay Peninsula, Singapore's tropical climate welcomes both leisure and business travelers year round. The island republic's excellent infrastructure enables visitors to enjoy its many sites and attractions in a safe, clean and green environment. Award winning Changi Airport provides airlinks to major cities around the world. The train and subway systems are clean, fast and efficient. In addition, its state-of-the-art cruise terminal has established Singapore as one of the premier cruising centers of South East Asia and an exciting port of call on any Asian cruise itinerary. In the city, there is no need for a car. Public transportation is excellent and walking is a good way to explore the city. All major attractions are also accessible by tour bus. Since the city is only 60 miles (100k) from the equator, the tropical temperatures do not vary much. Rainfall is fairly evenly distributed through the year. No matter when you choose to visit, warm weather will be abundantly available. The visitor is struck immediately by Singapore's abundance of parks, nature reserves, and lush, tropical greenery.

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