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## SEMINAR

### TRANSIENT-INDUCED LATCHUP (TLU) IN CMOS INTEGRATED CIRCUITS

**14 DEC 2011, 8.15am – 5 pm**

**SIMTech Auditorium, Tower Block, Level 3**

#### Introduction

Transient-induced latchup (TLU) has become an increasingly critical reliability issue in complementary oxide semiconductor oxide (CMOS) integrated circuits (IC) products due to the requirement of strict electromagnetic compatibility (EMC) regulations. Although latchup can be overcome by process solutions such as using epitaxial wafer, retrograde well, silicon-on-insulator (SOI) and trench isolation, it still remains as a significant reliability issue in CMOS IC products because of the reduced spacing between devices, multiple power supplies, low-doped substrate for high-voltage applications, and other cost reduction processing and design practices. This is especially true for TLU-induced failure. In response, the standard practice to evaluate the robustness of CMOS ICs against TLU was established and released (ANSI/ESD SP5.4-2004: Transient Latch-up Testing — Component Level Supply Transient Stimulation, 2004. ESD Association Standard Practice). It is common for TLU to occur in CMOS ICs in electrical equipment during system-level ESD tests. Resolving TLU requires a good understanding of the TLU physical mechanisms as well as methodologies for TLU characterization and extraction of layout design rules that are latchup-robust and yet compact and cost efficient, especially for high-pin-count CMOS ICs.

This discussion will cover the mechanisms, testing, preventive methods, case studies of latchup and TLU. In particular, it will include the phenomenon and basic physical mechanisms of latchup; critical factors affecting latchup susceptibility; experimental methodologies for extracting area-efficient compact layout design rules, including layout rules for I/O cells, core circuits and between I/O and core circuits; and characterization techniques for TLU, including an efficient component-level TLU measurement setup with bipolar under-damped sinusoidal trigger. Unexpected latchup issues can still exist even though an IC layout is in compliance with the latchup design guidelines. This is due to the existence of unexpected latchup paths between two different power domains, between power-pins and grounded N+/N-well, between two adjacent I/O cells, etc. The solutions to these unexpected latchup issues will be discussed. A case study to evaluate the latchup immunity of a high-voltage (HV) CMOS process will be presented.

The seminar will also feature talks by other ESD researchers.

Detailed seminar notes will be given out to the participants.

This seminar is jointly brought to you by the Singapore Institute of Manufacturing Technology (SIMTech), Singapore Semiconductor Industry Association (SSIA) and the Singapore Workforce Development Agency (WDA).

#### Programme

8.15 am	Registration & Morning Refreshment
9.00 am	Welcome Address by SIMTech
9.05 am	Address by SSIA
9.10 am	Robustness and Reliability Study of Electrostatic Protection Devices Under VF-TLP Stress by Dr Lai Weng Hong, SIMTech
9.40 am	Surface Charge Density Measurements and Electrostatic Meter (ESM) Calibrations

	by Dr Jing Tao, National Metrology Centre
10.10 am	Break
10.30 am	<b>Transient-Induced Latchup in CMOS Integrated Circuits (Part I) by Prof Ker Ming-Dou</b>
12.00 pm	Lunch and Networking
1.00 pm	Address by WDA
1.10 pm	<b>Transient-Induced Latchup in CMOS Integrated Circuits (Part II) by Prof Ker Ming-Dou</b>
2.40 pm	Break & Afternoon Refreshment
3.00 pm	<b>Transient-Induced Latchup in CMOS Integrated Circuits (Part III) by Prof Ker Ming-Dou</b>
4.30 pm	ESD Lab Tour
5.00 pm	End of Seminar

## Abstracts

### **Transient-Induced Latchup in CMOS Integrated Circuits**

Transient-induced latchup (TLU) has become an increasingly critical reliability issue in complementary oxide semiconductor (CMOS) integrated circuits (IC) products due to the requirement of strict electromagnetic compatibility (EMC) regulations. Although latchup can be overcome by process solutions such as using epitaxial wafer, retrograde well, silicon-on-insulator (SOI) and trench isolation, it still remains as a significant reliability issue in CMOS IC products because of the reduced spacing between devices, multiple power supplies, low-doped substrate for high-voltage applications, and other cost reduction processing and design practices. This is especially true for TLU-induced failure. In response, the standard practice to evaluate the robustness of CMOS ICs against TLU was established and released (ANSI/ESD SP5.4-2004: Transient Latch-up Testing — Component Level Supply Transient Stimulation, 2004. ESD Association Standard Practice). It is common for TLU to occur in CMOS ICs in electrical equipment during system-level ESD tests. Resolving TLU requires a good understanding of the TLU physical mechanisms as well as methodologies for TLU characterization and extraction of layout design rules that are latchup-robust and yet compact and cost efficient, especially for high-pin-count CMOS ICs.

This discussion will cover the mechanisms, testing, preventive methods, case studies of latchup and TLU. In particular, it will include the phenomenon and basic physical mechanisms of latchup; critical factors affecting latchup susceptibility; experimental methodologies for extracting area-efficient compact layout design rules, including layout rules for I/O cells, core circuits and between I/O and core circuits; and characterization techniques for TLU, including an efficient component-level TLU measurement setup with bipolar under-damped sinusoidal trigger. Unexpected latchup issues can still exist even though an IC layout is in compliance with the latchup design guidelines. This is due to the existence of unexpected latchup paths between two different power domains, between power-pins and grounded N+/N-well, between two adjacent I/O cells, etc. The solutions to these unexpected latchup issues will be discussed. A case study to evaluate the latchup immunity of a high-voltage (HV) CMOS process will be presented.

### **Surface Charge Density Measurements and Electrostatic Meter (ESM) Calibrations**

Surface charge accumulation plays an important role in electrostatic discharge. It worsens the pre-breakdown insulation conditions and influences the discharge dynamics. This talk introduces the principle of using a capacitive probe to determine surface charge densities. Various calibration techniques will be covered. The design of a calibration system for widely-used ESMs, the analysis of the affecting factors and the evaluation of measurement uncertainty in calibration will also be introduced.

### **Robustness and Reliability Study of Electrostatic Protection Devices Under VF-TLP Stress**

Electrostatic discharge (ESD) qualification is essential for all the ICs before shipment. However, standard

qualification tests focuses on the robustness of the protection devices. In this work, we found that a robust ESD protection device may not be reliable in the sense that it may not be able to protect the IC after certain number of repeated ESD pulses.

### About the Speakers

**Ker Ming-Dou** received his Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan in 1993. Prof. Ker worked as the Department Manager with the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. Since 2004, he has been a Full Professor with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan. From 2008 to 2011, he was Vice President of I-Shou University, Kaohsiung, Taiwan. He is now the Distinguished Professor in the Department of Electronics Engineering, National Chiao-Tung University, Taiwan. He served as the Executive Director of National Science and Technology Programme on System-on-Chip (NSoC) in Taiwan from 2010 to 2011. He will be the Executive Director of National Science and Technology Programme on Nano Technology (NPNT) in Taiwan from 2011 to 2014.

In the field of reliability and quality design for microelectronic circuits and systems, Prof. Ker published over 450 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability of integrated circuits and microelectronic systems, among of which have been granted 187 US patents and 162 Taiwan patents. He has been invited to teach and consult on the reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC industry. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomedical circuits and systems for intelligent prosthesis.

Prof. Ker has served as the member of Technical Program Committee and the Session Chair of numerous international conferences for many years. He served as the Associate Editor for the *IEEE TRANSACTIONS ON VLSI SYSTEMS* from 2006 to 2007. He was selected as the *Distinguished Lecturer* by the IEEE Circuits and Systems Society from 2006 to 2007, and IEEE Electron Devices Society from 2008 to date. He was also the President of Foundation in Taiwan ESD Association. In 2008, he was awarded **IEEE Fellow** "for contributions to the electrostatic protection in integrated circuits and the performance optimization of VLSI Microsystems". In 2009, he was named as one of the top ten Distinguished Inventors in Taiwan.

**Jing Tao** received his Ph.D. from Delft University of Technology, the Netherlands, and has worked as a lecturer, a research fellow and a metrologist in the areas of high voltage technology and electrical metrology. Dr Jing published more than ten papers and a book on the mechanisms and detection of charge accumulations, and patented an instrument of his invention. He designed and built the standard high voltage laboratory in the Singapore National Metrology Centre (NMC) and designed and established a calibration system for ESMs. As the lead of the Electrical Laboratory of the NMC, his current research interests include insulation design, flashover failure analysis, electrostatic charge control, and metrology development in DC and low frequency regimes. He was a member of the international advisory committee for the International Conference on Properties and Applications of Dielectric Materials. He is a senior member of the IEEE.

**Lai Weng Hong** holds a Ph.D. in Electrical Engineering and B.Eng. (Hons) in Electrical Engineering from the National University of Singapore (NUS). Dr Lai is the author of one invited paper, author and co-author of 11 research papers and two patents. His research interest is in ESD design, modeling, testing and failure analysis. Prior to joining SIMTech, he has more than 13 years of cross-disciplinary experience in the semiconductor industry in wafer processing, device modeling, and IO/ESD library development across various technology nodes.

### Who Should Attend

Design, QRA and ESD Programme Managers, Engineers, Researchers, Academic Staff and Students.

## Registration

Seminar Fee: S\$100.00 per participant. Singaporeans and Permanent Residents can enjoy 50% funding from the Singapore Workforce Development Agency (WDA).

Please register via [secretariat@ssia.org.sg](mailto:secretariat@ssia.org.sg) with the following details:

Name :  
Company :  
Job Title :  
NRIC :  
Residence Status : Citizen/Permanent Resident/Foreigner  
Contact Number :  
Email :  
Age :  
Qualification :

Participants have to provide the full information to qualify for funding from the WDA. Any incomplete information provided may disqualify them from the funding.

The closing date for registration is **7 Dec 2011**. All participants will be sent a confirmation note upon registration. Please register early as vacancies are limited.

Payment is to be made prior to the seminar strictly by cheque or bank transaction.

All cheques should be made payable to 'SSIA', crossed and marked 'A/C payee only'. The seminar title should be written on the back of the cheque. Cheques are to be mailed to:

SSIA Secretariat  
1003 Bukit Merah Central  
#02-10  
Singapore 159836  
(Attention: ESD Seminar)

Payment by transaction:

Beneficiary Name: Singapore Semiconductor Industry Association  
Bank Name : DBS Bank, 257 Holland Avenue, Singapore 278984  
Bank Code : 7171 Branch Code : 008  
Account No : 008-900764-5 Swift Code : DBSSSGSG

## Contact Us

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# Prof. Ker's Talk in SIMTech ESD Seminar

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## 1. Title of Talk:

### **Transient-Induced Latchup in CMOS Integrated Circuits**

Speaker: Prof. Morris (Ming-Dou) Ker, *IEEE FELLOW*

Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.

e-mail: mdker@ieee.org

## 2. Abstract:

Transient-induced latchup (TLU) has been increasingly a primary reliability issue in CMOS integrated circuits (IC) products, due to the strict demands of electromagnetic compatibility (EMC) regulations. Although latchup could be overcome by some process solutions such as epitaxial wafer, retrograde well, silicon-on-insulator (SOI), trench isolation, etc, latchup still remains a significant issue in IC products because of the reduced spacing between devices, multiple power supplies, low-doped substrate for high-voltage applications, and the cost-down consideration. Many failure returns reveal that transient-induced latchup (TLU) is increasingly important in CMOS ICs, and thus the standard practice to evaluate the robustness of CMOS ICs against TLU has been established and released (*ANSI/ESD SP5.4-2004: Transient Latch-up Testing— Component Level Supply Transient Stimulation*, 2004. ESD Association Standard Practice). The occurrence of TLU under the system-level ESD test is commonly found in CMOS ICs within the electronic equipments. Such TLU issues would be a tough challenge due to the tight requirements of electromagnetic compatibility (EMC) regulations. As a result, the clarification of TLU physical mechanism and the development of TLU measurement setup are necessary. Additionally, safe and compact layout rules for latchup prevention are also crucial to design the latchup-robust CMOS ICs. Not only can the latchup layout rules ensure the latchup-robust layout plans, but also save more chip layout area for the cost-down objective, especially in high-pin-count CMOS ICs.

In this talk, the technical contents include (1) Principle of CMOS Latchup, (2) Latchup Testing, (3) Methods of Latchup Prevention, (4) Testkeys to Extract Compact Latchup Rules, (5) Transient-Induced Latchup, (6) Latchup Case Study, and (7) Latchup in HV Process. The phenomenon and the basic physical mechanism of latchup are introduced. Critical factors that make latchup an issue in CMOS technologies are also discussed. Moreover, the experimental methodologies to extract area-efficient compact layout rules for latchup prevention are introduced, including layout rules for I/O cells, for internal circuits, and for between I/O and internal circuits. TLU induced by the system-level ESD stresses is an important reliability issue due to

the strict-demanded specifications of the system-level ESD test. The background of TLU and its related experimental techniques for characterizations will be also introduced. To evaluate the immunity of IC against TLP, an efficient component-level TLU measurement setup with bipolar (underdamped sinusoidal) trigger is presented. Besides, unexpected latchup issues still potentially exist, even though the IC's layout designs are fully in compliance with the foundry-supported latchup design guidelines. These unexpected latchup paths can exist between two different power domains, between power-pins and grounded N+/N-well, between two adjacent I/O cells, etc. Neglecting these layout issues could draw the unanticipated latchup risks. The corresponding solutions to these unexpected latchup issues are also given. Finally, some case study due to latchup failure and the latchup concern in HV CMOS process are presented.

### 3. Speaker Biography



**Morris (Ming-Dou) Ker** received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1993.

He ever worked as the Department Manager with the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan.

Since 2004, he has been a Full Professor with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan. During 2008 ~ 2011, he was rotated to be Chair Professor and Vice President of I-Shou University, Kaohsiung, Taiwan. Now, he has been the Distinguished Professor in the Department of Electronics Engineering, National Chiao-Tung University, Taiwan. He ever served as the Executive Director of National Science and Technology Program on System-on-Chip (NSoC) in Taiwan during 2010 ~ 2011; and currently as the Executive Director of National Science and Technology Program on Nano Technology (NPNT) in Taiwan (2011 ~ 2014). In the technical field of reliability and quality design for microelectronic circuits and systems, he has published over 440 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability and quality of integrated circuits, which have been granted with 187 U.S. patents and 162 Taiwan patents. He had been invited to teach and/or to consult the reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC industry. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent

prosthesis.

Prof. Ker has served as a member of the Technical Program Committee and the Session Chair of numerous international conferences for many years. He ever served as the Associate Editor for the *IEEE TRANSACTIONS ON VLSI SYSTEMS*, 2006-2007. He was selected as the *Distinguished Lecturer* in the IEEE Circuits and Systems Society (2006–2007) and in the IEEE Electron Devices Society (2008–present). He was the President of Foundation in Taiwan ESD Association. In 2008, he has been an *IEEE Fellow* “for his contributions to the electrostatic protection in integrated circuits and the performance optimization of VLSI Microsystems”. In 2009, he was awarded as one of the top ten Distinguished Inventors in Taiwan.

# Transient-Induced Latchup in CMOS Integrated Circuits

Prof. Morris (Ming-Dou) Ker, *IEEE FELLOW*

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Hsinchu, Taiwan.
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Kaohsiung, Taiwan.

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## OUTLINE

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4. Testkeys to Extract Compact Latchup Rules.
5. Transient-Induced Latchup.
6. Latchup Case Study.
7. Latchup in HV Process.
8. Summary.

Ref.: Ming-Dou Ker and Sheng-Fu Hsu, *Transient-Induced Latchup  
in CMOS Integrated Circuits*, John Wiley & Sons, 2009.  
(ISBN: 978-0-470-82407-8)