STATE KEY LAB OF ANALOG AND MIXED-SIGNAL VLSI - SCIENCE SERIES

Second Distinguished Lectures 22 and 24 March 2012

22-Mar-2012

Venue: HG01, Ho Yin Convention Center, UM

09:00 The world of analog micro-power

Franco Maloberti

University of Pavia, Italy

10:10 Wearable Healthcare (Bio-Medical CMOS IC System Design)

Hoi-Jun Yoo

Korea Advanced Institute of Science and Technology (KAIST), Korea

11:20 Coffee

11:45 Low Power, High Bandwidth and Ultra-Small Memory Module Design

Jacob Baker

Bram Nauta

Boise State University, USA

14:30 N-Path Filters

University of Twente, Netherlands

15:30 Low cost, high efficiency Power Management IC Design

Hong Zhiliang

Fudan University, China

16:30 **Coffee**

17:00 Medical electronics - the next big engine for semiconductor industry

Wang Zhihua

Tsinghua University, China

Open to Public, For enquiry:

State Key Laboratory of Analog and Mixed-Signal VLSI, R317, JLG212

Tel: (853) 8397-8796 Website: www.fst.umac.mo/en/lab/ans_vlsi/























STATE KEY LAB OF ANALOG AND MIXED-SIGNAL VLSI - SCIENCE SERIES

Second Distinguished Lectures 22 and 24 March 2012

24-Mar-2012

Venue: HG01, Ho Yin Convention Center, UM

109:00 Talk 1: Low energy and low voltage ADC design strategy

Talk 2: Proposing an interpolated pipeline ADC

Akira Matsuzawa

Tokyo Institute of Technology, Japan



10:30 **Coffee**

11:00 What you Don't Know About Miller Compensation Chris Mangelsdorf

Analog Devices



12:00 New Design Considerations on ESD Clamp Circuit in Nanoscale CMOS Technology

Ming-Dou Ker

National Chiao-Tung University, Taiwan



Open to Public, For enquiry:

State Key Laboratory of Analog and Mixed-Signal VLSI, R317, JLG212
Tel: (853) 8397-8796 Website: www.fst.umac.mo/en/lab/ans_vlsi/











DL Talk in Macau University

New Design Considerations On ESD Clamp Circuits in Nanoscale CMOS Technology

Prof. Morris (Ming-Dou) Ker / 柯明道教授 1,2

- ¹ Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan. (交通大學 電子研究所 特聘教授)
- ² Dept. of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan. (義守大學電子工程學系講座教授)

M.-D. Ker March 24, 2012

Outline

- Standards of ESD Testing
- On-Chip ESD Protection
 Design with Active Power-Rail ESD Clamp Circuit
- Low-Leakage Power-RailESD Clamp Circuits
- Summary



M.-D. Ker

(Talk@TSMC)

2