Tutorials - Sunday, April 15 and Monday, April 16

Elyse Rosenbaum, Chairperson

Sunday Morning				
Room				
8:30 a.m. - 10:00 a.m.	Probability and Statistics for the IC Reliability Engineer	Front-end of Line (FEOL) Reliability in CMOS Technologies	On-Chip ESD Protection Design for CMOS ICs	Failure Analysis: Applications and Challenges
	Tony Oates, TSMC	Andreas Kerber and William McMahon, GLOBALFOUNDRIES	Ming-Dou Ker, NCTU	Yong-Fen Hsieh, MA-Tek
30 min Break				
10:30 a.m. 12:00 p.m.	**Probability and Statistics for the IC Reliability Engineer (continued)**	**Front-end Reliability in CMOS Technologies (continued)**	**On-Chip ESD Protection Design for CMOS ICs (continued)**	Reliability of Advanced Packaging Technologies
	Tony Oates, TSMC	Andreas Kerber and William McMahon, GLOBALFOUNDRIES	Ming-Dou Ker, NCTU	Jennifer Muncy, IBM
Lunch				
Sunday Afternoon				
1:00 p.m. - 2:30 p.m.	Challenges in Accelerated Testing Due to Technology Scaling	Reliability Physics of High-k/Metal Gate Stacks	System-Level ESD Reliability from an IC Perspective	Reliability of Cu/Low-k Interconnect Structures
	Patrick Justison, GLOBALFOUNDRIES, and Richard Wong, Cisco	Eduard Cartier, IBM	Jonathan Brodsky, TI	Paul Ho, UT-Austin, Martin Gall-Fraunhofer Institute for Nondestructive Testing in Dresden
30 min Break				
3:00 p.m. - 4:30 p.m.	Reliability Considerations for Ultra-Low Power Applications: Medical and Space		Reliability Issues in Automotive Microelectronic Components and Systems	System-level Approach to Thermo-Electro-Mechanical Reliability in TSV-Based 3D ICs
	Mark Porter, Medtronic, and Mark White, JPL		Werner Kanert and Michael Nelhiebel, Infineon	Sung Kyu Lim, Georgia Tech
Monday Morning				
Room				
8:30 a.m. - 10 a.m.	Circuit-level Reliability	Advanced Experimental Techniques for BTI Characterization	Hot Carrier Degradation in High Voltage Devices	Soft Errors in Modern SRAMs
	Keith Bowman, Intel, and Yu Cao, ASU	Ben Kaczer, imec	Dhanoop Varghese, TI	Helmut Puchner, Cypress
30 min Break				
10:30 a.m. - 12:00 p.m.	**Circuit-level Reliability (continued) -- ends approx. 11 a.m.**	Random Telegraph Noise – Measurement, Analysis, and Consequences	Reliability of Gallium Nitride HEMTs	Trap-related Reliability Issues in NAND Flash Memory
	Keith Bowman, Intel, and Yu Cao, ASU	David Frank, IBM	Gaudenzio Meneghesso, Univ. of Padova	Hiroshi Watanabe, NCTU

Green: Introductory level tutorial

Yellow: Advanced level tutorial

On-Chip ESD Protection Design for CMOS Integrated Circuits

In advanced CMOS technologies, the MOSFET gate-oxide thickness of MOSFET is only 10~15Å for operating with a sub-1V power supply. Such thin gate oxide is very easily ruptured by electrostatic discharge (ESD) events that occur during assembly, testing, and packaging.

To verify the ESD reliability of IC products, there exist ESD test standards, such as the Human Body Model (HBM) and Charged Device Model (CDM) tests. How to design the on-chip ESD protection circuits to effectively protect integrated circuits realized by the nano-scale CMOS devices is a quite difficult challenge for the IC industry. The on-chip ESD protection circuit must be included in the beginning phase of chip design.

In this tutorial, an introduction to the ESD issue and test standards for IC products will be presented. Failure analysis pictures from real IC products will be used to demonstrate the impact of ESD on IC products. The basic design concept for on-chip ESD protection circuits will be presented, including the operation principle of ESD devices and the corresponding layout considerations. Some useful ESD protection techniques, e.g., gate-driven design and substrate-triggered design, will be shown with circuit implementations.

Whole-chip ESD protection may be achieved by using the active power-rail ESD clamp circuit. Special considerations for the design of active power-rail ESD clamp circuits in nanoscale CMOS processes will be addressed. ESD protection design for high-speed I/O and RF circuits will also be covered.

Following the presentation on component-level ESD protection, the subject of system-level ESD protection will be briefly introduced.

Biography: Ming-Dou Ker received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1993. He then worked in the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. He currently is a Distinguished Professor in the Department of Electronics Engineering, National Chiao-Tung University, Taiwan.

Prof. Ker has published over 450 technical papers in international journals and conferences in the field of reliability and quality design for microelectronic circuits and systems. He has been granted 188 U.S. patents and 163 Taiwan patents, most of these are relevant to the ESD protection topic. His ESD protection solutions have been implemented in the I/O cell libraries provided by foundries in several different CMOS generations, and his ESD protection principles are incorporated in the foundry design rules.

Prof. Ker has been invited to teach and/or to consult by hundreds of design houses and semiconductor companies in the worldwide IC industry. He has published one book on the topic of transient-induced latchup in CMOS ICs. Prof. Ker has served as a member of the Technical Program Committee and the Session Chair of numerous international conferences for many years. He served as the Associate Editor for the *IEEE Transactions on VLSI Systems* during 2006-2007.

Tutorial Talk in *2012 IEEE International Reliability Physics Symp.*

On-Chip ESD Protection Design for CMOS Integrated Circuits

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Outlines

1. Introduction with ESD Models (Standards).
2. Chip-Level ESD Protection Design.
3. Power-Rail ESD Clamp Circuits.
4. System-Level ESD Issue.