IEEE Electron Devices Society

March 5th, 2012

Ming-Dou Ker
Professor, Department of Electronics Engineering
National Chiao-Tung University, Taiwan
E-Mail: mdker@alab.ee.nctu.edu.tw

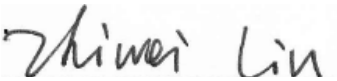
RE: Invitation for 2012 IEEE Electron Devices Mini-Colloquium, Chengdu

Dear Prof. Ker,

The IEEE Electron Devices Society (EDS) Chapter in Chengdu, China, will organize an EDS sponsored mini-colloquium (MQ) on April 26-28 in Chengdu, China. Because of your great expertise in the field of electrostatic discharge protection design, I would like to invite you to give a talk at this mini-colloquium (MQ) of IEEE Electron Devices Society.

We look forward to seeing you in Chengdu in April. Thanks.

Sincerely,



Dr. Zhiwei Liu, Associate Professor
University of Electronic Science and Technology China
Vice Chair, IEEE Electron Devices Society Chengdu Chapter

University of
Electronic Science and Technology of
China

IEEE Electron Devices Mini Colloquium

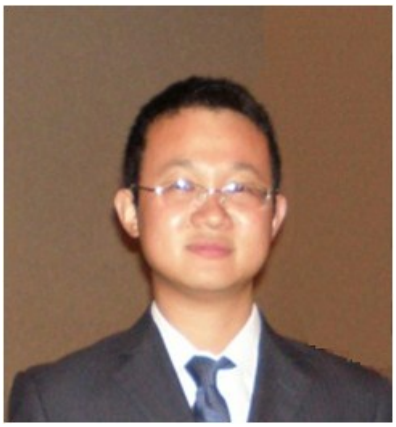
April 26-27, 2012

UESTC, Chengdu

ELECTRON DEVICES SOCIETY

HANWA

Welcome



On behalf of the IEEE Electron Device Society (EDS) Chengdu Chapter, I would like to welcome you to the IEEE ED Mini-Colloquium. The technical program consists of twelve talks given by internationally recognized lecturers in the field of electron devices. The topics include electrostatic discharge protection design, process reliability, film bulk acoustic resonator, E-beam Lithography, high-voltage integration, and silicon photonic technology.

This colloquium will provide an excellent opportunity for UESTC graduate and undergraduate students to learn about the state of the art in micro/nanoelectronics, to interact and exchange ideas with the speakers, and to discuss research activities.

At this time, I would like to thank all the sponsors of this event: IEEE Electron Devices Society, Graduate School of UESTC, State Key Laboratory of Electronic Thin Films and Integrated Devices, Science and Technology on Analog Integrated Circuit Laboratory and HANWA Electronic Ind.Co.,Ltd . I would also like to thank Dr. Juin J. Liou, EDS Vice-President of Regions/Chapters for his guidance. Last, but not the least, I thank all the lecturers for taking the time off their work to come to Chengdu and participate in this event.

It is again my great honor and pleasure to extend a warm wel-

Welcome

come to everyone. It is my hope that this colloquium is an intellectually enriching experience for all who attend.

Dr. Zhiwei Liu
Associate professor, UESTC
Vice Chair, IEEE EDS Chengdu Chapter

Program

Thursday, April 26th , 2012

Teaching Building One, Room 104, UESTC (Shahe Campus)

8:30 - 9:00	Dean's Message —
8:40 - 8:50	Welcome Note — Dr. Zhiwei Liu (Vice Chair, IEEE EDS Chengdu Chapter)
8:50 - 9:00	Opening Speech — Dr. Juin J. Liou (IEEE EDS Vice-President of Regions/Chapters)
9:00 - 10:00	Dr. Juin J. Liou (UCF) — Electrostatic Discharge (ESD) Protection of Integrated Circuits.
10:00 - 11:00	Dr. Steven H. Voldman (Dr. Steven H Voldman, LLC) — ESD and Latchup in Three Dimensional (3-D) Semiconductor Memory Chip Systems.
11:00 - 12:00	Dr. Ming-Dou Ker (National Chiao-Tung University) — Design of Ultra-Low-Leakage Power-Rail ESD Clamp Circuits in Nanoscale CMOS Technology.
12:00 - 13:00	**Buffet Lunch**
14:00 - 15:00	Mr. Teruo Suzuki (Fujitsu Semiconductor) — Introduc-tion of the solutions to the problems due to the Electro-static Discharge (ESD).
15:00 - 16:00	Dr. Zhenghao Gan and Dr. Waisum Wong (SMIC) — Process Reliability on Deep SubMicron Technology Nodes (40nm and Beyond) — Challenges and Opportunities.
16:00 - 17:00	Dr. Shurong Dong (Zhejiang University) — Recently Development of Film bulk acoustic resonator (FBAR)
18:00 - 20:00	**Banquet Dinner (By Invitation Only)**

Program

Friday, April 27th, 2012

Teaching Building One, Room 104, UESTC (Shahe Campus)

8:30 – 9:30	Dr. Charvaka Duvvury (TI) — Future ESD Challenges for IC Components and Systems
9:30 – 10:30	Dr. Jiang Yan (IMECAS) — E-beam Lithography Application for 22nm and below
10:30 – 10:50	Mr. Masanori Sawada (HANWA) — Study of FI-CDM Discharge Waveform
10:50 – 11:50	Mr. Yonghai Hu (CSMC) — High-Voltage integration and its related problems
12:00 – 13:00	**Buffet Lunch**
14:00 – 15:00	Mr. Yasuhiro Fukuda (Samsung Electronics) — ESD Failure Phenomena and Protection
15:00 – 16:00	Dr. Hei Wong (City University of Hong Kong) — Development of Silicon Photonic Technology for Micro-electronic Optical Interconnects Applications.
16:00 – 16:30	**Lab Visiting**
18:00 – 20:00	**Banquet Dinner (By Invitation Only)**

Dr. Ming-Dou Ker

Ming-Dou Ker received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1993.

He ever worked as the Department Manager with the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. During 2008 ~ 2011, he was rotated to be a Vice President of I-Shou University, Kaohsiung, Taiwan. Now, he has been the Distinguished Professor in the Department of Electronics Engineering, National Chiao-Tung University, Taiwan. In the technical field of reliability and quality design for microelectronic circuits and systems, he has published over 450 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability and quality of integrated circuits, which have been granted with 190 U.S. patents and 165 Taiwan patents. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent prosthesis.

Prof. Ker has served as the Session Chair of numerous international conferences for many years. He ever served as the Associate Editor for the *IEEE TRANSACTIONS ON VLSI SYSTEMS*, 2006-2007. He was selected as the *Distinguished Lecturer* in the IEEE Circuits and Systems Society (2006–2007) and in the IEEE Electron Devices Society (2008–present). He was the President of Foundation in Taiwan ESD Association. In 2008, he has been an *IEEE Fellow* "for his contributions to the electrostatic protection in integrated circuits and the performance optimization of VLSI Microsystems". In 2009, he was awarded as one of the top ten Distinguished Inventors in Taiwan.

“Design of Ultra-Low-Leakage Power-Rail ESD Clamp Circuits in Nanoscale CMOS Technology”

To verify the reliability and quality of IC products to ESD robustness for safe applications, there are already some industry ESD standards developed, such as Human Body Model (HBM) and Charged Device Model (CDM), to verify the ESD robustness of IC products. Typically, for safe production of ICs, the ESD robustness for commercial IC products has been requested to sustain the ESD levels of ±2kV in the HBM ESD test and ±1kV in the CDM ESD test. Besides, in the IEC 61000-4-2 standard, the electronic products are zapped by the ESD gun with ESD voltage of up to 15kV in the air-discharge mode. How to design the on-chip ESD protection circuits to effectively protect the integrated circuits realized by the nanoscale CMOS devices is a quite difficult challenge in IC industry. The on-chip ESD protection circuit must be included in the beginning phase of chip design. On-chip ESD protection design is not only the process issue but also highly dependent to the circuit design issue.

In this talk, we focus on the design methods to reduce the leakage current in the active power-rail ESD clamp circuit. The gate tunneling effect impacts drastically in the leakage current of the traditional power-rail ESD clamp circuit realized with the RC-based ESD detection circuit in the nanoscale CMOS technology. The leakage current of the traditional power-rail ESD clamp circuit could be scaled up to several hundred microamperes, as reported in some articles that were verified in 65-nm CMOS technology. Circuit design techniques can successfully reduce the leakage current of the power-rail ESD clamp circuit to the nanoamperes (nA) order, without significant area overhead, and also without decreasing ESD robustness. The methods to reduce the leakage current among the power-rail ESD clamp circuits are reviewed in this talk, which include (1) using the thick gate oxide (dual gate-oxide process), (2) using the high-k / metal gate, (3) using the parasitic capacitance (between metal layers), (4) reducing the voltage drop across the MOS capacitor, (5) reducing the gate area of the MOS capacitor, (6) capacitor-less design, (7) using SCR (no gate structure) as main ESD clamp device.

Colloquium Committee

Zhiwei Liu
Wei Li
Yiwen Wang
Jizhi Liu
Yulong Zhu
Ruzhang Li
Yi Liu
Linfeng He

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Graduate School of UESTC

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Science and Technology on Analog Integrated Circuit Laboratory

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Dr. Zhiwei Liu
Associate Professor, UESTC
Vice Chair, IEEE EDS Chengdu Chapter
E-MAIL: zliu@uestc.edu.cn
TEL: (86)-28-83207701