F6: Mixed-Signal/RF Design and Modeling in Next-Generation CMOS

Organizer/Chair: **Boris Murmann,** *Stanford University, Stanford, CA*

Committee: **Jafar Savoj,** *Xilinx, San Jose, CA*
Piet Wambacq, imec*, Heverlee, Belgium*
Jieh-Tsorng Wu, *National Chiao-Tung University, Hsinchu, Taiwan*

Technology awareness and modeling is important in all areas of mixed-signal and RF design. This Forum intends to provide, for next-generation CMOS, a holistic overview and discussion spanning a variety of important aspects of device modeling, reliability, and simulation. It begins with an analog/RF-centric comparison between FinFET and ultra-thin-body SOI technology. The next two talks then venture into bias stress and Electrostatic Discharge Protection (ESD), which are two issues of ever-increasing importance for future scaling. The fourth presentation discusses the latest developments surrounding the popular BSIM transistor model, and explains how this new model can be efficiently coupled to the analog/RF design process. Motivated by their increasing significance in integrated RF transceivers, the next talk outlines a future roadmap for passive components in scaled technologies. Then, we expand upon modeling challenges that arise when components are stacked in three dimensions. Finally, this series of modeling talks is rounded up by two comprehensive presentations that summarize key challenges from the foundry and EDA-tool-vendor perspectives.

Agenda

Time	Topic
08:00	Breakfast
08:20	**Introduction** **Boris Murmann,** *Stanford University, Stanford, CA*
08:30	**FinFET versus UTBB SOI for RF/Analog Applications** **Tsu-Jae King Liu,** *University of California, Berkeley, CA*
09:20	**Reliability Modeling for nm-Scale Components** **Praveen Raghavan,** *imec, Heverlee, Belgium*
10:10	Break
10:35	**ESD-Protection Design in Nanometer CMOS** **Ming-Dou Ker,** *National Chiao-Tung University, Hsinchu, Taiwan*
11:25	**The BSIM6 MOSFET Compact Model and Its Use for Analog and RF Design** **Christian Enz,** *CSEM, Neuchâtel, Switzerland*
12:15	Lunch
13:20	**Development of Passives in Advanced CMOS: A Key Enabler for RF Applications up to mm-Wave** **Frédéric Gianesello,** *STMicroelectronics, Crolles, France*
14:10	**3D Stacking, the Best of Both Worlds: Modeling Issues in an Optimized Heterogeneous (Analog/Digital) Stacked Design** **Liam Madden,** *Xilinx, San Jose, CA*
15:00	Break
15:20	**Foundry Perspectives on Analog/RF Challenges in Next-Generation CMOS** **Sally Liu,** *TSMC, Hsinchu, Taiwan*
16:10	**Next-Generation Analog/RF EDA Tools** **Li-Da Huang,** *Synopsys, Austin, TX*
17:00	Closing Remarks (Chair)

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FinFET versus UTBB SOI for RF/Analog Applications

Tsu-Jae King Liu, *University of California, Berkeley, CA*

Tsu-Jae King Liu received her B.S., M.S., and Ph.D. degrees in Electrical Engineering from Stanford University, Stanford, CA. From 1992 to 1996, she was a Member of the Research Staff at Xerox Palo Alto Research Center (Palo Alto, CA). In August 1996, she joined the University of California, Berkeley, where she is currently the Conexant Systems Distinguished Professor of Electrical Engineering and Computer Sciences (EECS), Associate Chair of the EECS and EE Division Chair. Her awards include the DARPA Significant Technical Achievement Award (2000) for development of FinFETs; IEEE Fellow (2007); the IEEE Kiyo Tomiyasu Award (2010) for contributions to nanoscale MOS transistors, memory devices, and MEMS devices; and the Intel Outstanding Researcher in Nanotechnology Award (2012). She has authored or co-authored over 400 publications and holds over 80 U.S. patents. Her research activities are presently in nanometer-scale logic and memory devices, and technology for energy-efficient electronics. She has served on committees for many technical conferences, including the IEEE International Electron Devices Meeting and the IEEE Symposium on VLSI Technology, and served as an Editor for the IEEE Electron Devices Letters from 1999 to 2004.

Reliability Modeling for nm-Scale Components

Praveen Raghavan, *imec, Heverlee, Belgium*

Praveen Raghavan received his B.S. in Electrical Engineering from the Regional Engineering College in Trichy, India, his M.S. in Electrical Engineering from Arizona State University, Tempe, and his Ph.D. from KU Leuven in 2009. In 2007, he was a visiting researcher at the Berkeley Wireless Research Center (BWRC), University of California, Berkeley. He is currently a Principal Scientist in circuits and systems for the ICT group at IMEC, where he is the lead processor architect for IMEC's next-generation 4G software-defined radio platform. He also leads a team of Ph.D. students working on energy-efficient architectures in scaled technologies. His research interests include processor architectures, the impact of deeply scaled technology on architectures/systems, reliability, variability, low-power design, and software-defined radios. He has published over 80 conference and journal papers in this area and holds more than 30 patents.

ESD-Protection Design in Nanometer CMOS

Ming-Dou Ker, *National Chiao-Tung University, Hsinchu,Taiwan*

Ming-Dou Ker received his Ph.D. from National Chiao-Tung University, Hsinchu, Taiwan, in 1993 and subsequently worked in the Industrial-Technology Research Institute (ITRI), Hsinchu, Taiwan. At present, he is a Distinguished Professor in the Department of Electronics Engineering, National Chiao-Tung University, Taiwan; as well as a Chair Professor of I-Shou University, Kaohsiung, Taiwan. In the technical field of reliability and quality design for microelectronic circuits and systems, he has proposed many solutions to improve the reliability and quality of integrated circuits, which have resulted in hundreds of U.S. and Taiwan patents. He has been invited to teach and/or to consult in the area of reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies worldwide. He has served as member of the Technical Program Committee and Session Chair for numerous international conferences. He has served as the Associate Editor for the IEEE Transactions on VLSI Systems (2006 to 2007); a Distinguished Lecturer of the IEEE Circuits and Systems Society (2006 to2007); and a Distinguished Lecturer of the IEEE Electron Devices Society (2008 to2012). He is the Founding President of Taiwan ESD Association. Currently, he is the Editor of the IEEE Transactions on Device and Materials Reliability. Since 2012, he has been the Dean of the College of Photonics, National Chiao-Tung University, Taiwan. He is a Fellow of the IEEE.

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The BSIM6 MOSFET Compact Model and Its Use for Analog and RF Design

Christian Enz, *CSEM, Neuchâtel, Switzerland*

Christian Enz received his Ph.D. from the Swiss Federal Institute of Technology (EPFL) in 1989. He joined the Swiss Center for Electronics and Microtechnology (CSEM) in Neuchâtel, Switzerland, where he is VP of the Integrated and Wireless Systems Division. Since 1999, he has been a Professor at EPFL, where he works in the field of analog and RFIC design. Prior to joining CSEM, he was Principal Senior Engineer at Conexant (formerly Rockwell Semiconductor Systems), Newport Beach, CA, where he was responsible for the modeling and characterization of MOS transistors for RF applications. His technical interests and expertise are in the field of wireless sensor networks, very-low-power and low-voltage analog and RFIC design, and semiconductordevice modeling. He is one of the developers of the EKV MOS transistor model and author of the book "Charge-Based MOS Transistor Modeling - The EKV Model for Low-Power and RF IC Design" (Wiley, 2006). He is the author and co-author of more than 150 scientific papers and has contributed to numerous conference organization committees, presentations, and advanced engineering courses.

Development of Passives in Advanced CMOS: A Key Enabler for RF Applications up to mm-Wave

Frédéric Gianesello, *STMicroelectronics, Crolles, France*

Fred Gianesello received his B.S. and M.S. in electronics engineering from the Institut National Polytechnique de Grenoble (Grenoble, France) in 2003 (Editor's note: both in the same year?), and his Ph.D. in electrical engineering from the Joseph Fourier University (Grenoble, France) in 2006. Since 2006, he has been with STMicroelecetronics (Crolles, France), where he currently leads the development of electromagnetic devices integrated on advanced RF CMOS/BiCMOS and packaging technologies. He has authored and coauthored more than 80 refereed journal and conference technical articles. His current work deals with high-performance passive-component development in advanced bulk and SOI RF CMOS technologies, RF and mm-wave antenna design, 3D integration packaging technology, and silicon photonic passive-component development.

3D Stacking, the Best of Both Worlds: Modeling Issues in an Optimized Heterogeneous (Analog/Digital) Stacked Design

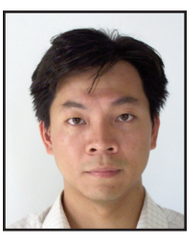
Liam Madden, *Xilinx, San Jose, CA*

Liam Madden is Corporate Vice-President, FPGA Development and Silicon Technology at Xilinx. He graduated with a B.E. from University College Dublin in 1979, and an M.Eng. from Cornell University in 1990. He oversees all FPGA hardware development at Xilinx. Prior to joining Xilinx, he worked primarily in the microprocessor field, and was a member of the team that delivered the first Alpha and StrongArm microprocessors at DEC. He has also led design teams at MIPS Technologies, Microsoft (XBOX-360), and AMD.

Foundry Perspectives on Analog/RF Challenges in Next-Generation CMOS

Sally Liu, *TSMC, Hsinchu, Taiwan*

Sally Liu is the Technical Director of Mixed-Signal RF Solutions Division at TSMC, Hsinchu, Taiwan. She joined TSMC in 2004. Prior to this, she spent fifteen years at AT&T Bell Laboratories, six years at Conexant/Rockwell Semiconductors, and two years at RF Integrated Corporation. She has a broad interest in semiconductors and integrated circuits, including emerging nanometer devices, 3D IC, mixed-signal/-analog and RF device characterization, low- and high-frequency noise in devices, device compact modeling and simulation, circuit simulation and optimization, statistical modeling and design centering, circuit verification, IP characterization and EDA framework. She received her B.S. in physics and M.S. in applied physics from National Tsing-Hua University, Hsinchu Taiwan, and her Ph.D. in electrical engineering and computer science from the University of California, Berkeley, CA.



Next-Generation Analog/RF EDA Tools

Li-Da Huang, *Synopsys, Austin, TX*

Li-Da Huang received his Ph.D. in computer science from the University of Texas, Austin, in 2003. From 2000 to 2006, he was a Senior Mixed-Signal IC Designer with Texas Instruments, Austin, TX. From 2006 to 2010, he led the development of the router in design for manufacturing with Magma Design Automation. From 2010 to 2012, he was the Director of Product Engineering in the Customer Design Business Unit of Magma Design Automation. He has been in charge of analog design optimization and device modeling. Currently, he is with the Analog Mixed-Signal Group at Synospys. His research interests include circuit design, design automation, and signal processing. He has published more than 20 papers. Several papers are regarded as pioneer works in design for manufacturing in OPC-friendly routing, redundant via insertion, and antenna effects in routing. Recently, he has focused on analog design automation and modeling. He is a member of Upsilon-Pi-Epsilon, the international honor society for the computing and information disciplines, and has been an IEEE Senior Member since 2005.

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ESD-Protection Design in Nanometer CMOS

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Anantha Padmanabhan

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