

NOTICE

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THE DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE, ECE DIVISION



Presents the Summer 2013 EECS Seminar Series

Dr. Ming-Dou Ker
National Chiao-Tung University

"ESD Protection Design in Nanometer CMOS"
Thursday, July 25, 2013 • 2:00 p.m. • HEC 356

The nanometer CMOS integrated circuits are very vulnerable to electrostatic discharge (ESD) events, which frequently happen in our environments with the voltage level of hundreds or even thousands volts. To verify the ESD reliability of IC products for safe applications, some industry ESD test standards had been already developed, such as Human Body Model (HBM) and Charged Device Model (CDM). In addition, the IEC 61000-4-2 standard is used to verify the system-level ESD robustness of the electronic products by the ESD gun with ESD voltage of even up to 15kV. How to design the on-chip ESD protection circuits to effectively protect the integrated circuits realized by the nano-scale CMOS devices is a quite difficult challenge to IC industry. *In this talk*, a brief introduction on ESD issue and test standards to IC products is presented with some failure analysis pictures from real IC products to demonstrate the impact of ESD on IC products. The basic design concept for on-chip ESD protection circuit will be presented. Some useful ESD protection designs for high-speed I/O and RF circuits will be mentioned. To achieve the whole-chip ESD protection by using the active power-rail ESD clamp circuit will be emphasized. Additional consideration on the active power-rail ESD clamp circuit realized in the nano-scale CMOS processes will be addressed. After the component-level ESD protection, the system-level ESD protection design will be briefly discussed. ESD protection for CMOS ICs is not only the process issue but also highly dependent to the design issue, which has been an important topic that the IC designers need to know.

BIOGRAPHY

Ming-Dou Ker received the Ph.D. degree from National Chiao-Tung University, Hsinchu, Taiwan, in 1993. He ever worked in the Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. Now, he has been the Distinguished Professor in the Department of Electronics Engineering, National Chiao-Tung University, Taiwan; as well as the Chair Professor of I-Shou University, Kaohsiung, Taiwan. In the technical field of reliability and quality design for microelectronic circuits and systems, he has proposed many solutions to improve the reliability and quality of integrated circuits, which have been granted with hundreds of U.S. patents and Taiwan patents. He had been invited to teach and/or to consult the reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC industry. Prof. Ker has served as member of the Technical Program Committee and the Session Chair of numerous international conferences for many years. He ever served as the Associate Editor for the *IEEE TRANSACTIONS ON VLSI SYSTEMS* (2006-2007); the *Distinguished Lecturer* of IEEE Circuits and Systems Society (2006-2007); and the *Distinguished Lecturer* of IEEE Electron Devices Society (2008-2013). He was the Founding President of Taiwan ESD Association. Currently, he is the Editor of *IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY*. Since 2012, he has been the Dean of the College of Photonics, National Chiao-Tung University, Taiwan. Prof. Ker is a Fellow of the IEEE.

26/07/2013

DEPARTMENT OF ELECTRICAL ENGINEERING & COMPUTER SCIENCE

DL Talk to:

IEEE EDS Orlando Chapter, University of Central Florida.

ESD Protection Design in Nanometer CMOS

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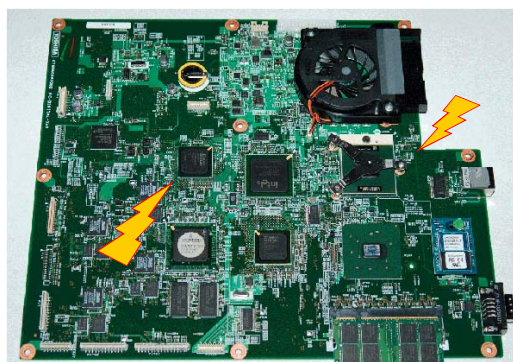
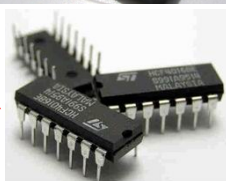
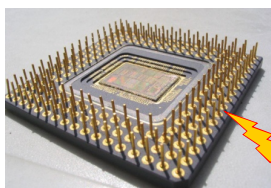
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Outlines

1. ESD Models (Standards).
2. Chip-Level ESD Protection.
3. Board-Level ESD Protection.
4. System-Level ESD Protection.



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