2019

13th International Electrostatic Discharge Workshop

March 31 - April 4, 2019

IEW

Setting the Global Standards for Static Control!

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ESD ASSOCIATION

Invited Talk 2

Cost-Efficient Methods for Latch-up Prevention in CMOS Integrated Circuits

Professor Ming-Dou Ker, Institute of Electronics, National Chiao-Tung University

In CMOS ICs, latch-up is formed by the parasitic p-n-p-n structure between power lines of VDD and VSS. Such parasitic p-n-p-n structure is inherent in the bulk CMOS technology. The parasitic p-n-p-n structure could be accidentally triggered on by external glitches or transient noises to generate a low-impedance path between the power lines. When latch-up was triggered on, CMOS ICs were often burned out seriously by the latch-up-generated heat. Therefore, latch-up presentation is one of major reliability topics in CMOS ICs, especially realized in bulk CMOS technology. In this talk, a brief background of latch-up in CMOS ICs is given. The methodology to extract compact layout rules used to prevent latch-up occurrence on the I/O cells is introduced. Even if the I/O cells of a CMOS IC are free from latch-up, the core circuits in the CMOS ICs will be still sensitive to latch-up issue. The reasons to cause latch-up occurrence on the core circuits are explained, including the transient-induced latch-up during system-level ESD or FET testing. To further improve latch-up immunity of CMOS ICs but without enlarging the spacing/distance in the chip layout, a novel concept of “active guard ring” and its corresponding circuit implementation will be addressed. Additional latch-up events on the circuits with different power domains, such as HV and LV blocks, I/O PMOS and core PMOS, PMOS and varactor, will be discussed. Finally, the low holding voltage of the on-chip ESD protection device used in the power-rail ESD clamp may also cause latch-up-like failure. The solutions to overcome such latch-up-like issue, especially in HV applications, will be mentioned. Latch-up prevention in CMOS ICs is not only the process issue but also highly dependent to the layout and design issue, which has been an important topic that the IC designers need to know.

Ming-Dou Ker received the Ph.D. degree from National Chiao-Tung University, Hsinchu, Taiwan, in 1993. He ever worked as the Department Manager with the VLSI Design Division, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. From 2012 to 2015, he was the Dean of the College of Photonics, National Chiao-Tung University (NCTU), Taiwan. Now, he has been the Distinguished Professor in the Institute of Electronics, National Chiao-Tung University, Taiwan. Currently, he is also serving as the Director of the Biomedical Electronics Translational Research Center (BETRC), NCTU, working on biomedical electronics translational projects.

In the technical field of reliability and quality design for microelectronic circuits and systems, he has published over 560 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability and quality of integrated circuits, which have been granted with hundreds of U.S. patents. He had been invited to teach and/or to consult the reliability and quality design by hundreds of design houses and semiconductor companies in the worldwide IC industry. His current research interests include the circuits and systems for biomedical applications, as well as circuit-related reliability issue.

Prof. Ker has served as member of the Technical Program Committee and the Session Chair of numerous international conferences for many years, including IEEE Symp. on VLSI Circuits and IEEE International Solid-State Circuits Conference. He ever served as the Associate Editor for the IEEE Transactions on VLSI Systems, 2006-2007. He served as the Distinguished Lecturer in the IEEE Circuits and Systems Society (2006–2007) and in the IEEE Electron Devices Society (2008–2018). He was the Founding President of Taiwan ESD Association. Currently, he is serving as an Editor for the IEEE Transactions on Device and Materials Reliability, and an Associate Editor for the IEEE Transactions on Biomedical Circuits and Systems. Prof. Ker has been a Fellow of the IEEE since 2008.

Schedule continued

11:15-12:30 pm	Poster Session B
12:30-1:30 pm	Lunch
1:30-2:50 pm	Discussion Groups B DG B.1 - Future CDM Testing: Problems and Solution Options Moderator: Nathan Jack DG B.2 - Latch-up Data Analysis & Real World Relevance Moderator: Marty Johnson, Texas Instruments
2:50 pm	Free Time & Dinner Off-Site (Not hosted by ESDA)
Wednesday	**April 3**
7:30-9:00 am	Breakfast
9:00-10:00 am	Invited Talk 2 - Cost-Efficient Methods for Latch-up Prevention in CMOS Integrated Circuits Speaker: Ming-Dou Ker, Institute of Electronics, National Chiao-Tung University
10:00-10:30 am	Break (Refreshments Provided)
10:30-11:30 am	Seminar 3 - JESD78: Status, Challenges, and the Future Speaker: Scott Ruth, NXP Semiconductors
11:30-12:10 pm	Reports on Discussion Groups A and B
12:10-12:30 pm	Industry Council Report
12:30-1:00 pm	Break/Free Time
1:00-2:30 pm	IRPS Lunch with Distinguished Lecturer (For more information, please visit https://irps.org/program/distinguished-lecturer/)
2:30-5:25 pm	IRPS ESD/LU Technical Session (For more information, please visit https://irps.org/program/technical-program/)
6:00-9:00 pm	IRPS & IEW Joint Poster Session + Reception (For more information, please visit https://irps.org/program/poster-session-reception/)
Thursday	**April 4**
7:30-9:00 am	Breakfast
8:45-9:00 am	Closing

2019 International ESD Workshop (IEW)

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Hyatt Regency Monterey

One Old Golf Course Road, Monterey CA, USA

13th Annual International Electostatic Discharge Workshop

Now in its 13th year, the IEW continues to provide a relaxed, invigorating atmosphere to present new work and engage in discussions about the latest issues confronting the ESD and EOS communities. This year, IEW will co-locate with the International Reliability Physics Symposium (IRPS)! In addition to everything IEW provides, IEW registrants will can also attend the IRPS technical sessions on ESD and latch-up as well as a joint evening poster reception showcasing works from both conferences. Thus, submissions to IEW will receive exposure to a much broader audience. IEW attendees will also be exposed to work from a wider range of reliability topics from IRPS and will have access to IRPS keynotes. IRPS registrants will have access to IEW keynote and invited talks (but not the other unique elements of IEW). IEW will retain those elements which make it the unique experience it is: invited speakers & seminars, discussion groups, and some down time to network and explore the area.

DON'T MISS THE DEADLINE!

December 3rd, 2018

CO-LOCATING WITH IRPS

People's Choice Award will be presented to a poster chosen by attendees.

Submission Instructions

Submission instructions and an abstract template are available at https://www.esda.org/index.php/events/iew/. The submission is in PowerPoint format and should be no longer than 6 slides. Submissions are due **December 3, 2018** to iew@esda.org. The IEW does not publish proceedings, even for IEW-registered posters presented during joint IRPS/IEW poster session. **Do not submit the same work to both IRPS and IEW**; please choose only one conference for consideration. Walk-on posters are also permitted at IEW with no prior review, but only those works which are submitted for review and acceptance will be included in the five-minute teaser presentation sessions.

FOCUS TOPICS FOR IEW 2019

New Developments in Latch-Up

Emerging product trends such as technology scaling (e.g. FinFet versus planar CMOS), increasing product complexity, and more demanding operation environments (e.g. automotive; high junction temperature; radiation-induced latch-up; etc.) all lead to the stark reality that latch-up will be a major reliability threat for the foreseeable future. There are active teams in the industry working to consolidate learning and best practices for latch-up EDA tools as well to test and qualify the increasingly complex products that are being produced. The IEW welcomes you to share your experience and perspective on this important topic.

System ESD

Cable Discharge Event (CDE) - test methods, applicability, design impact, potential standardization. System ESD design - co-design between system board and the component (SEED). System ESD simulation methods and component modeling, new stress models. On-chip design methods for improving system ESD. System ESD related failure modes and cases studies. Test methods for validating ESD on the board level - is test standardization of component robustness under system ESD feasible?

Electrical Overstress (EOS)

EOS continues to be one of the largest causes of customer returns in the semiconductor industry. Have you recently completed root-cause analysis on a failure with an electrical induced physical damage (EIPD) signature? There is no defined procedure to determine absolute maximum ratings (AMR) for a product. Do you have a methodology for defining AMR for a product, and verifying it for different timescales? Are you an FA engineer with experience on case studies identifying EOS damage mechanisms and the ensuing physical evidence? Finding sources of EOS can be a challenge. Do you have experience auditing a manufacturing site for sources of EOS? Bring your work to the IEW and share it with your colleagues.

Other topics and areas to consider for abstract submissions including but not limited to:

Anomalous/Unresolved ESD Issues
Random and unrepeatable ESD failures, case histories, ESD tester correlation issues, and unique window failures.

Automotive Applications ESD/EMC
The electronic content of automobiles is increasing, leading to more complex electronic modules and system design. Integration of ICs and discrete devices is demanding, considering the module level EMC testing and reliability requirements. The IEW invites contributions that address ESD and EMC challenges in automotive systems design, including complying with standards such as bulk current injection (BCI), direct power injection (DPI), IEC-61000-4-2, ISO-10605, and ISO-7637.

ESD Big Data
Summarizing and viewing large ESD and latch-up tester datasets. Viewing CDM waveform parameter statistics. Mapping design data to ESD and latch-up test programs.

System-Level ESD Issues
On- and off- chip IEC protection clamps, component/system ESD co-design case studies, cable discharge clamps, transient latch-up, design of system-level clamp circuits, system-level ESD test issues and scan techniques, and ESD-induced soft errors.

Failure Analysis Techniques
Locating failure sites, in particular for CDM, imaging techniques, correlating FA identified damage site with ESD stress, distinguishing EOS-like failures from ESD failures, and unusual failure modes.

Technology Integration Issues
ESD sensitivity with technology transfers, 3D IC ESD design issues, qualification challenges for different fabs, unusual problems of process interaction with ESD, process monitor methods, and technology scaling issues.

EDA Tools
EDA verification and simulation tools; techniques, design-flows, best practices, experiences with foundry rule decks, commercial tools, and custom tooling.

ESD Control
As technologies continue to change, we need to consider the control methods being used and continually review the standards and methodologies being used to ensure the best practices are being followed. Case in point, to provide industry with the best standards possible, S20.20/625B working groups are looking at harmonizing these documents. We also need to consider whether there are any weak points in today's processes which may require updates to the Control standards or perhaps new standards to cover new technologies. The use of discharge detectors as a tool for analyzing problem areas within assembly have proven to be very useful. Should analysis tools like discharge detectors become standard in the Control process.

Novel On-Chip Protection Clamps and Circuit Configurations
New clamp devices and clamp configurations, methods to increase the failure threshold of protected devices, high voltage clamps for automotive and power amplifiers, new chip protection concepts, and low-capacitance clamps for RF and high speed interfaces.

ESD Test Characterization, Methods, and Issues
TLP & VF-TLP debug and device characterization methods, correlation of TLP & VF-TLP tests with standard qualification tests, HBM and CDM tester artifacts, unresolved test results and failures, issues relating test qualification levels to real-world exposure, test chip methodology, cable discharge test methods, and test standards issues.

Mark Your Calendar!

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