IEEE Electron Devices Society

June 9th, 2017

Prof. Ming-Dou Ker

Department of Electronics Engineering, National Chiao Tung University, Taiwan

E-Mail: mdker@ieee.org

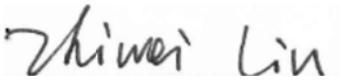
RE: Invitation for 2017 IEEE Electron Devices Mini-Colloquium, Chengdu

Dear Prof. Ker,

The IEEE Electron Devices Society (EDS) Chapter in Chengdu, China will organize an EDS sponsored mini-colloquium (MQ) on July 4th in Chengdu, China. Because of your expertise in the field of electronic devices, I would like to invite you to give a talk at the MQ cordially.

We look forward to seeing you in Chengdu in July. Thanks.

Sincerely,



Dr. Zhiwei Liu, Associate Professor
University of Electronic Science and Technology China
Vice Chair, IEEE Electron Devices Society Chengdu Chapter

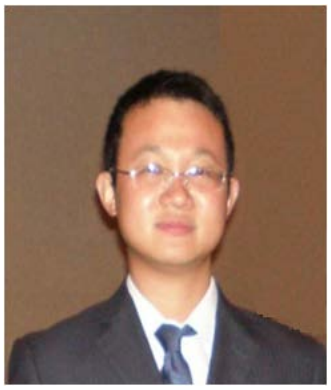
IEEE Electron Devices Society, Chengdu Chapter
Address: No. 4, Section 2, North Jianshe Road, Chengdu City, Sichuan Province, P.R. China.
Zip Code: 610054

IEEE EDS Mini-Colloquium

IEEE Electron Devices Society

July 4th, 2017
Chengdu

Welcome



On behalf of the IEEE Electron Device Society (EDS) Chengdu Chapter, I would like to welcome you to the IEEE EDS Mini-Colloquium. The technical program consists of five talks given by internationally recognized lecturers in the field of electron devices. The topics include electrostatic discharge protection design, integrated technology, failure analysis, nanometer device, memory device.

This colloquium will provide an excellent opportunity for UESTC graduate and undergraduate students to learn about the state of the art in micro/ nanoelectronics, to interact and exchange ideas with the speakers, and to discuss research activities.

At this time, I would like to thank all the sponsors of this event: IEEE Electron Devices Society, Graduate School of UESTC. I would also like to thank Dr. Juin J. Liou for his guidance. Last, but not the least, I thank all the lecturers for taking the time off their work to come to Chengdu and participate in this event.

It is again my great honor and pleasure to extend a warm welcome to everyone. It is my hope that this colloquium is an intellectually enriching experience for all who attend.

Dr. Zhiwei Liu

Associate professor, UESTC

Vice Chair, IEEE EDS Chengdu Chapter

Program

Tuesday, July 4th, 2017
Room 137, Weigu Building, UESTC

9:30-10:20	**Steve S. Chung** National Chiao Tung University **A Logic CMOS Compatible NVM Feasible for Embedded Applications**
10:20-10:25	Break
10:25-11:15	**Hei Wong** City University of Hong Kong **Some Issues of None-ideal Characteristics of Nanowire Transistors**
11:15-12:05	**Xing Zhou** Nanyang Technological University **Future III-V/CMOS Co-Integrated Technology and Hybrid Circuit Design**
12:05-13:30	Lunch
14:00-14:50	**Ming-Dou Ker** National Chiao Tung University **Challenge on ESD Protection for SOC with Separated Power Domains**
14:50-15:40	**Cher Ming Tan** Chang Gung University **Finite element analysis for the understanding of physics of failure in Microelectronics**

Dr. Ming-Dou Ker

Ming-Dou Ker received the Ph.D. degree from National Chiao-Tung University, Hsinchu, Taiwan, in 1993. He ever worked as the Department Manager with the VLSI Design Division, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. Since 2004, he has been a Full Professor with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan. During 2008~2011, he was rotated to be Chair Professor and Vice President of I-Shou University, Kaohsiung, Taiwan. Now, he has been the Distinguished Professor in the Institute of Electronics, National Chiao-Tung University, Taiwan. He ever served as the Executive Director of National Science and Technology Program on System-on-Chip (NSoC) in Taiwan during 2010~2011; and the Executive Director of National Science and Technology Program on Nano Technology (NPNT) in Taiwan (2011~2015). During 2012~ 2015, he was the Dean of the College of Photonics, National Chiao-Tung University (NCTU), Taiwan. Currently, he is serving as the Director of the Biomedical Electronics Translational Research Center (BETRC), NCTU, working on biomedical electronics translational projects.

In the technical field of reliability and quality design for microelectronic circuits and systems, he has published over 500 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability and quality of integrated circuits, which have been granted with hundreds of U.S. patents and Taiwan patents. He had been invited to teach and/or to consult the reliability and quality design by hundreds of design houses and semiconductor companies in the worldwide IC industry. His current research interests include the circuits and systems for biomedical applications, as well as circuit-related reliability issue.

Prof. Ker has served as member of the Technical Program Committee and the Session Chair of numerous international conferences for many years, including the IEEE Symposium on VLSI Circuits. He ever served as the Associate Editor for the IEEE Transactions on VLSI Systems, 2006-2007. He was selected as the Distinguished Lecturer in the IEEE Circuits and Systems Society (2006–2007), and in the IEEE Electron Devices Society (2008–2015). He was the Founding President of Taiwan ESD Association. Currently, he is the Editor of IEEE Transactions on Device and Materials Reliability. Prof. Ker has been a Fellow of the IEEE since 2008. In 2015, Prof. Ker received the Award for Outstanding Science and Technology Contribution, the Executive Yuan, Taiwan.

Challenge on ESD Protection for SOC with Separated Power Domains

To reduce the weight of electronic products, to integrate more functions into the electronic products, as well as to reduce the power consumption of electronic products, the CMOS technology has been developed into nanometer scale to realize SOC for electronic systems. With the transistors in the nano-scale dimension, the gate-oxide thickness of MOSFET is only ~15Å for operating with sub-1V power supply. Such thinner gate oxide is very easily ruptured by electrostatic discharge (ESD) events, which frequently happen in our environments with the voltage level of hundreds or even thousands volts. The integrated circuits (ICs) are weaker to sustain such ESD stresses during the assembly, testing, package, and the applications. Therefore, the on-chip ESD protection circuits must be equipped on the ICs against ESD stresses, including the Human Body Model (HBM) and Charged Device Model (CDM). How to design the on-chip ESD protection circuits to effectively protect the integrated circuits realized by the nano-scale CMOS devices is a quite difficult challenge to IC industry, especially in the SOC with separated power domains. In this talk, the ESD issue on SOC with separated power domains will be discussed and shown with some failure cases. The successful ESD protection design to overcome such issue will be presented. ESD protection for CMOS ICs is not only the process issue but also highly dependent to the design issue, which has been an important topic that the IC designers need to know.