國立交通大學

NATIONAL CHIAO-TUNG UNIVERSITY

Noise and Reliability in Silicon Electronics

Monday, Nov. 13rd 2017　13:30~18:30

國立交通大學工程四館B26室

Room B26, Engineering Building 4, NCTU

Featured Keynote and Plenary Speakers


T. Ohguro (Toshiba)

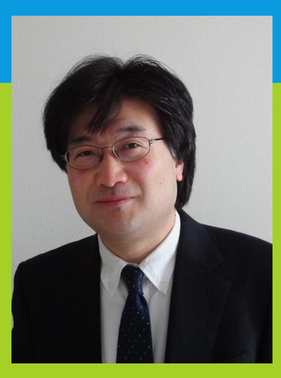

A. Teramoto (Tohoku Univ.)


Po-Jui Lin (NCTU)


Y. Akasaka (TEL)


Yung-Yueh Chiu (NCTU)


Ming-Dou Ker (NCTU)


N. Sano (Tsukuba Univ.)

Abstract

The latest studies on noise and reliability in silicon electronic devices will be addressed. Accurate understanding for the various behaviors of carriers has been increasingly important in advanced nano-devices. 1/f noise, random telegraph noise and discrete impurity model will be reported in detail. In addition to some breakthroughs in state-of-the-art process technologies, reliability related issues in memory/logic LSIs will be presented. In the seminar the prospects for future technology development will be discussed from the viewpoint of device and process.

(Moderator: H. S. Momose)

The organizer：National Chiao Tung University

The co-organizer：Electrical and Computer Engineering (ECE), NCTU
International College of Semiconductor Technology (ICST), NCTU

Report: The seminar on "Noise and Reliability in Silicon Electronics"

The seminar on *"Noise and Reliability in Silicon Electronics"* was held at Room B26 of Engineering Building #4 at the afternoon on November 13, 2017. More than 50 audience including many students and researchers/engineers from institutes or companies were attended.

At opening, Dr. Hisayo S. Momose, who is a visiting professor of *International College of Semiconductor Technology, NCTU,* explained the purpose of the seminar as a Chair. She said that in the seminar, the latest studies focused on noise and reliability would be reviewed. In addition, it was described that various phenomena related to carriers would be explained in detail and that some problems to be solved before LSI applications would be discussed from the viewpoint of device and process technologies.

The program consisted of seven presentations by excellent speakers who are famous authorities in silicon electronics from Japan and NCTU.

The first speaker was Mr. Tatsuya Ohguro, who is a Chief Specialist in *Toshiba Electronic Devices & Storage Corporation, Ishikawa, Japan.* He is one of the leading experts in the research area of noise characteristics in CMOS devices. His presentation was entitled *"Study of Low Frequency Noise of CMOS."* He lectured the origin of low frequency noise in MOSFETs and reported about the dependences of noise on device structures and process conditions, including high-k gate, FINFET and deuterium annealing.

The next speaker, Prof. Akinobu Teramoto talked about random telegraph noise. He is a professor at *New Industry Creation Hatchery Center, Tohoku University, Sendai, Japan,* who is very famous world-wide especially in the

research area of noise analysis. In these years, he has done many interesting works for accurate evaluation and analysis of the noise. He talked to us about *"Statistical Evaluation of Random Telegraph Noise in MOSFETs."* In his talk, the drain current dependence of RTN, which were evaluated statistically by using a low noise measurement system, was reported. The traps to the percolation path and the probability were also explained in detail.

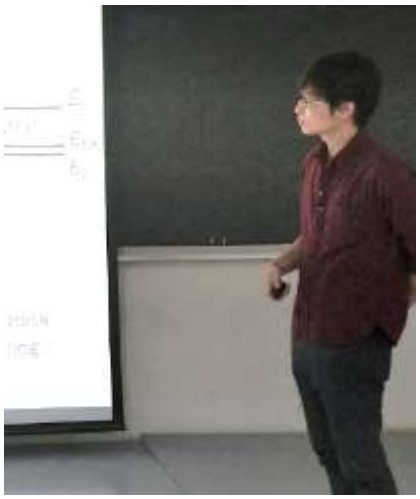
Mr. Po-Jui Lin, who is currently pursuing his Ph. D. degree in *the Institute of Communications Engineering at NCTU,* was talked on *"Localized Tunneling Phenomena of Nano-meter Scaled High-K Gate Stack."* He reported the results regarding the tunneling phenomena of nano-meter scaled high-K gate stack, which was obtained using unified transient simulation introducing 3D real-space path integral. He explained in detail that it is sensitive to single electron phenomena via local trap in high-K.

Mr. Ohguro (Toshiba)

Prof. Teramoto (Tohoku Univ.)

The latter half of the seminar started from Dr. Yasushi Akasaka's presentation. He is Vice President of *Process Integration Center, Tokyo Electron Technology Solutions Ltd. in Yamanashi, Japan,* who is in charge of integration, clean technology, metrology, and analysis. He talked about *"Process Integration from the Viewpoints of Material Selection."* In the talk, some breakthroughs in state-of-the-art process technologies including high-k film, gate materials and advanced deposition processes, were explained in detail. In addition, he described about various integration technologies needed for the realization of 3D devices, such as 3D NAND Flash and 3D RRAM.

Dr. Yung-Yueh Chiu, who received Ph.D. degrees from *NCTU* in 2017, presented on *"Impact of String Pattern on the Threshold-Voltage Spread of Program Inhibited Cell in NAND Flash."* He reported about the HCI effect caused by the NAND string pattern. In his work, the threshold voltage spread due to FN tunneling and HCI effect were statistically investigated in program inhibited cell.



Mr. Po-Jui Lin (NCTU)

Dr. Akasaka (TEL)

Dr. Yung-Yueh Chiu (NCTU)

Dr. Ming-Dou Ker is a distinguished professor of *the Institute of Electronics at NCTU.* Currently, he is serving as the Director of *Biomedical Electronics Translational Research Center, NCTU*, working on biomedical electronics translational projects. He is a very famous professor not only in the circuits and systems for biomedical applications, but also in circuit-related reliability issue. His presentation at this seminar was on *"Transient-Induced Latchup in CMOS Integrated Circuits."* He clearly explained the mechanism of latchup phenomenon in logic LSIs and the difference in each generation. He also reported the guard ring structures in order to improve latchup immunity.

Final speaker was prof. Nobuyuki Sano, who is a professor of *Applied Physics and Provost of the School of Science and Engineering at University of Tsukuba, Japan.* He is an authority in theoretical simulation for nanoscale devices. He has been working on the theory of quantum and semiclassical electron transport under nanoscale semiconductor structures and the fundamental aspects of various device simulation schemes applicable to nanoscale devices. He talked to us about *"Fundamental Aspects of Discrete Impurity Model for Nano-Scale Device Simulations."* He lectured on the physical background of the model in detail, including theoretical analysis of electron transport phenomena in nanoscale semiconductor devices.

Prof. Ming-Dou Ker (NCTU)

Prof. Sano (Tsukuba Univ.)

In closing, Prof. Riichiro Shirota, who is a professor of *Department of Electrical Engineering, NCTU,* concluded the seminar was timely and extremely useful for all of us. They were really informative, provocative and stimulating. He expressed our appreciation to the speakers for their excellent presentations and fruitful discussions and the audience for the attentions.

The seminar was successfully finished, as described above. We would like to express our sincere thanks to Prof. Edward Yi Chang, who is a Vice President and a Dean of Research and Development & Chair Professor, *NCTU,* for his great encouragement and support through this seminar. We are also grateful to Mr. Chi-Feng Lin, who is an assistant of the *International College of Semiconductor Technology, NCTU* for his great help in arranging this seminar.

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