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(54) **SELF-BALANCED DIODE DEVICE**

(56) **References Cited**

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U.S. PATENT DOCUMENTS

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9,117,669 B2	8/2015	Lin et al.	
9,368,484 B1 *	6/2016	Chen	H01L 27/0248
9,614,086 B1 *	4/2017	Yeo	H01L 29/7849
2007/0045736 A1	3/2007	Yagishita	
2014/0131831 A1 *	5/2014	Wei	H01L 21/77 257/506

FOREIGN PATENT DOCUMENTS

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TW	201419490 A	5/2014
TW	201423952 A	6/2014
TW	201503377 A	1/2015
TW	1496216 B	8/2015

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\* cited by examiner

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(21) Appl. No.: **15/241,469**

(57) **ABSTRACT**

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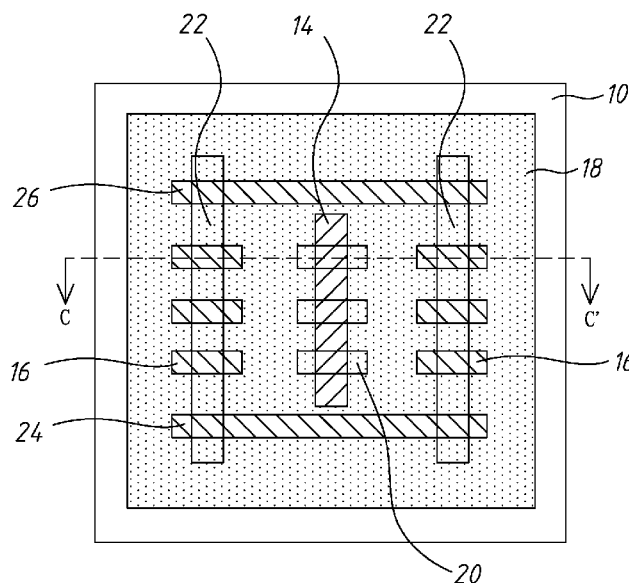
A self-balanced diode device includes a substrate, a doped well, at least one first conductivity type heavily doped fin and at least two second conductivity type heavily doped fins. The doped well is arranged in the substrate. The first conductivity type heavily doped fin is arranged in the doped well, arranged in a line along a first direction, and protruded up from a surface of the substrate. The second conductivity type heavily doped fins is arranged in the doped well, arranged in a line along a second direction intersecting the first direction, respectively arranged at two opposite sides of the first conductivity type heavily doped fin, and protruded up from the surface of the substrate. Each second conductivity type heavily doped fin and the first conductivity type heavily doped fin are spaced at a fixed interval.

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**H01L 27/06** (2006.01)  
**H01L 27/092** (2006.01)  
**H01L 29/861** (2006.01)

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(58) **Field of Classification Search**  
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See application file for complete search history.

**7 Claims, 4 Drawing Sheets**



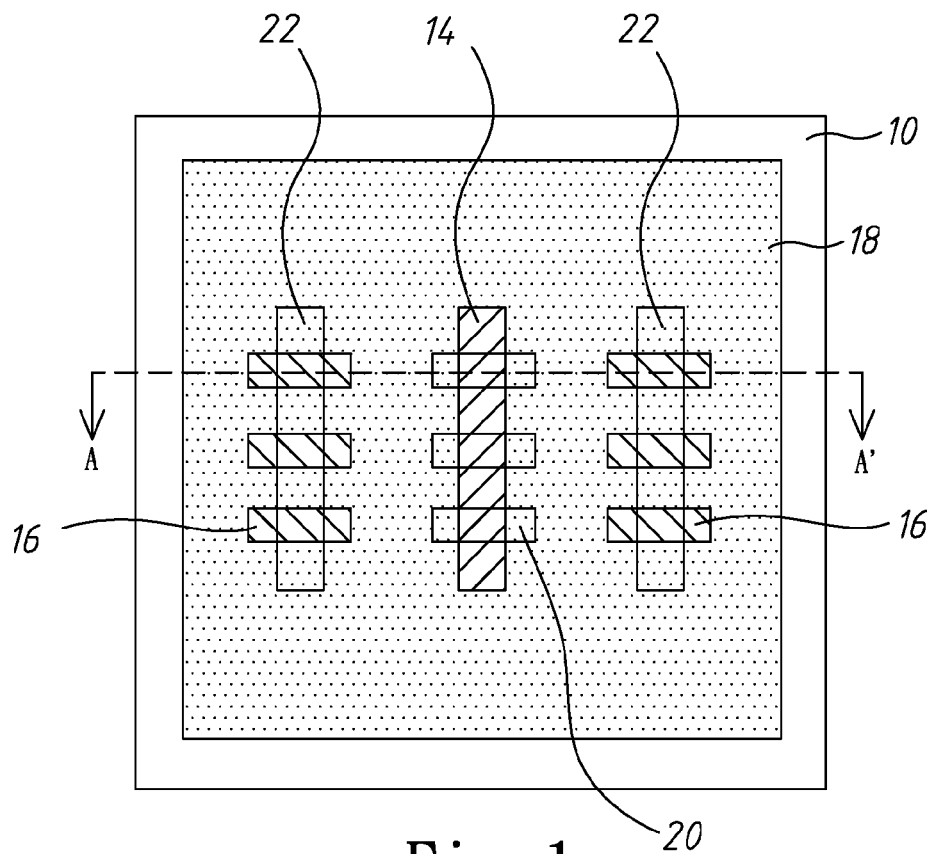


Fig. 1

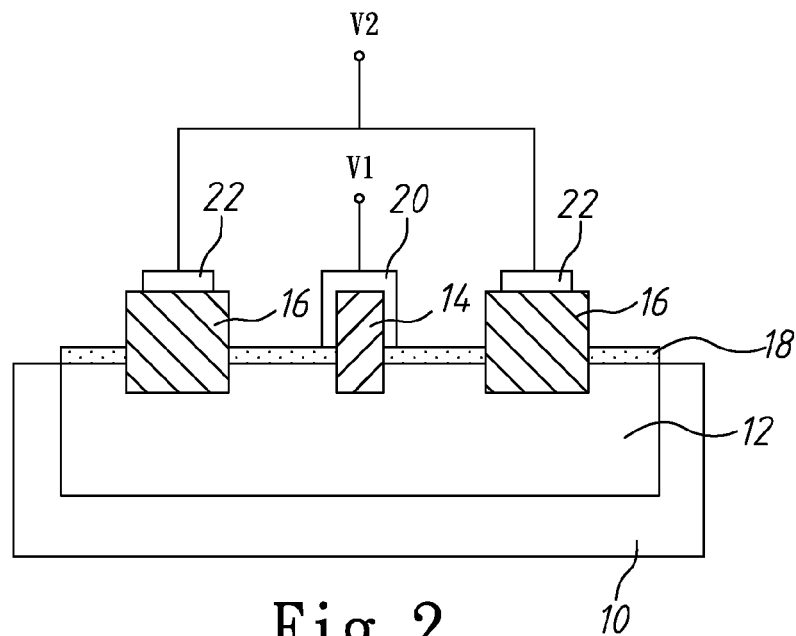


Fig. 2

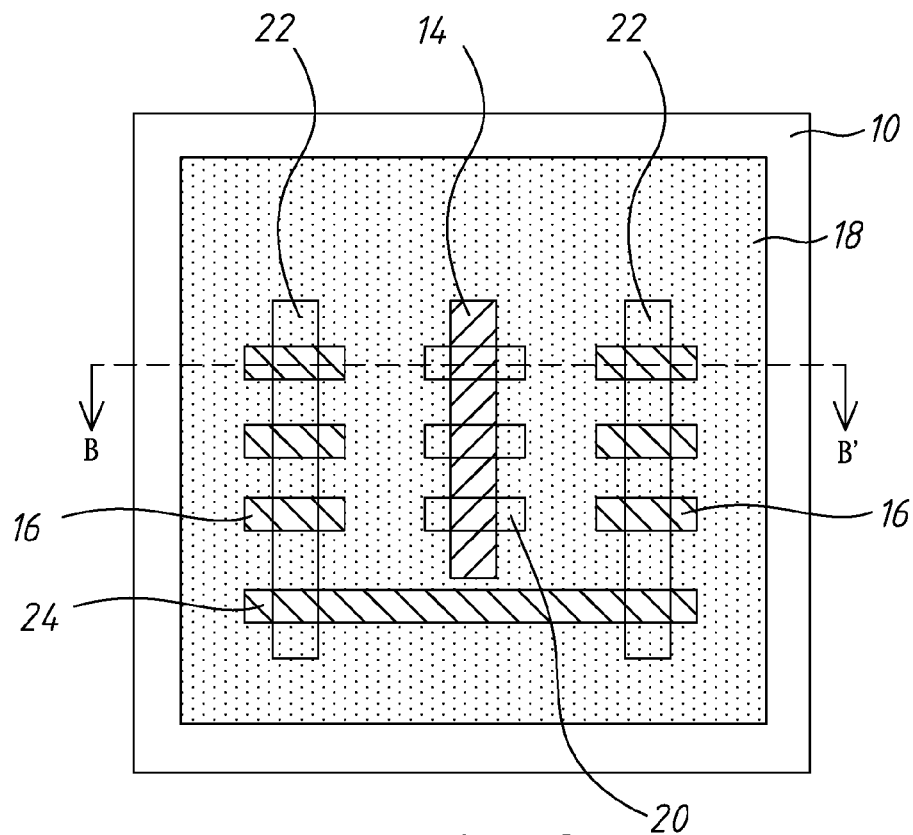


Fig. 3

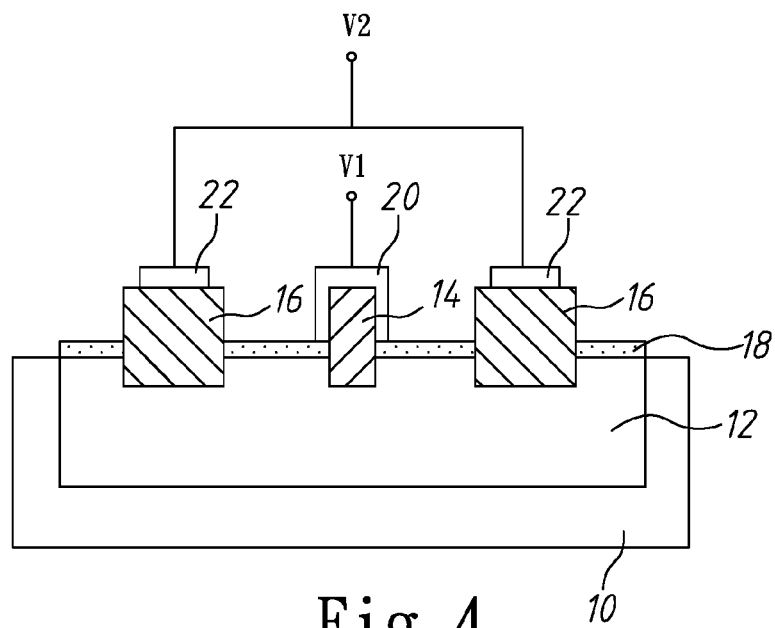


Fig. 4

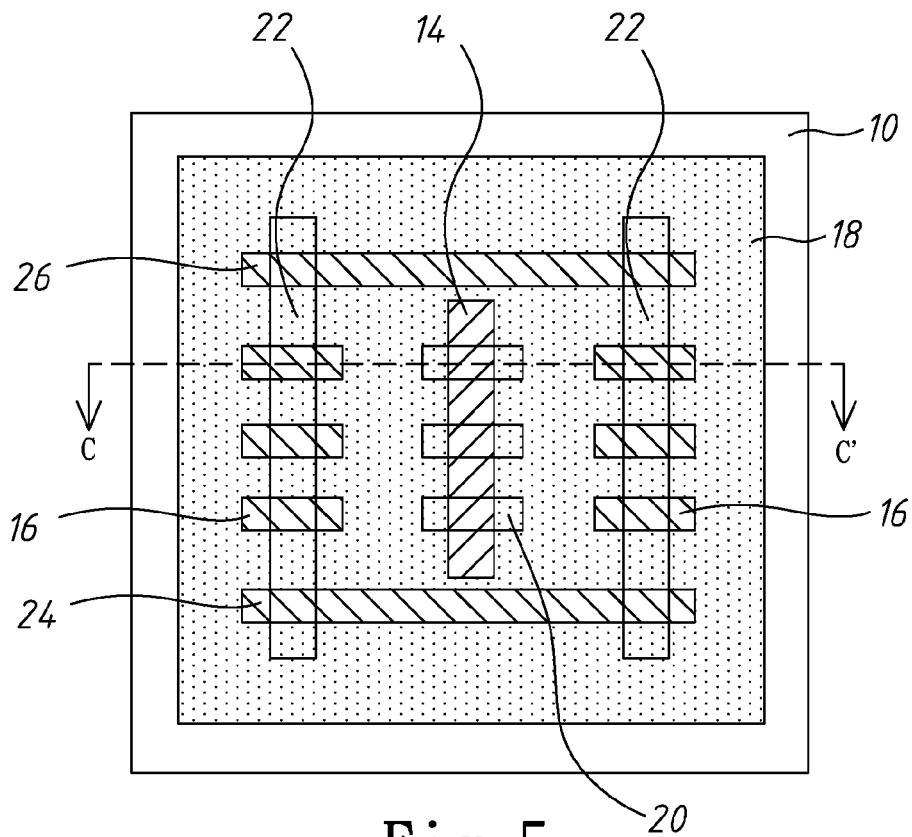


Fig. 5

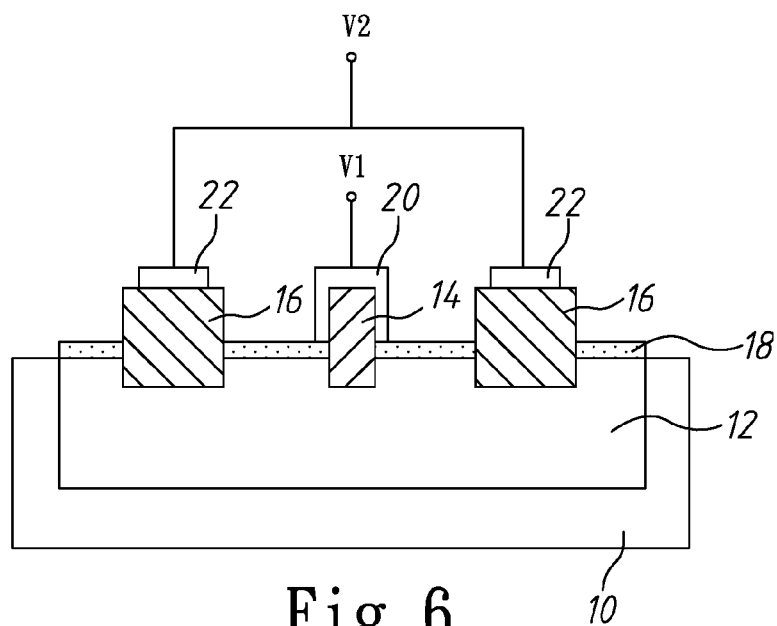


Fig. 6

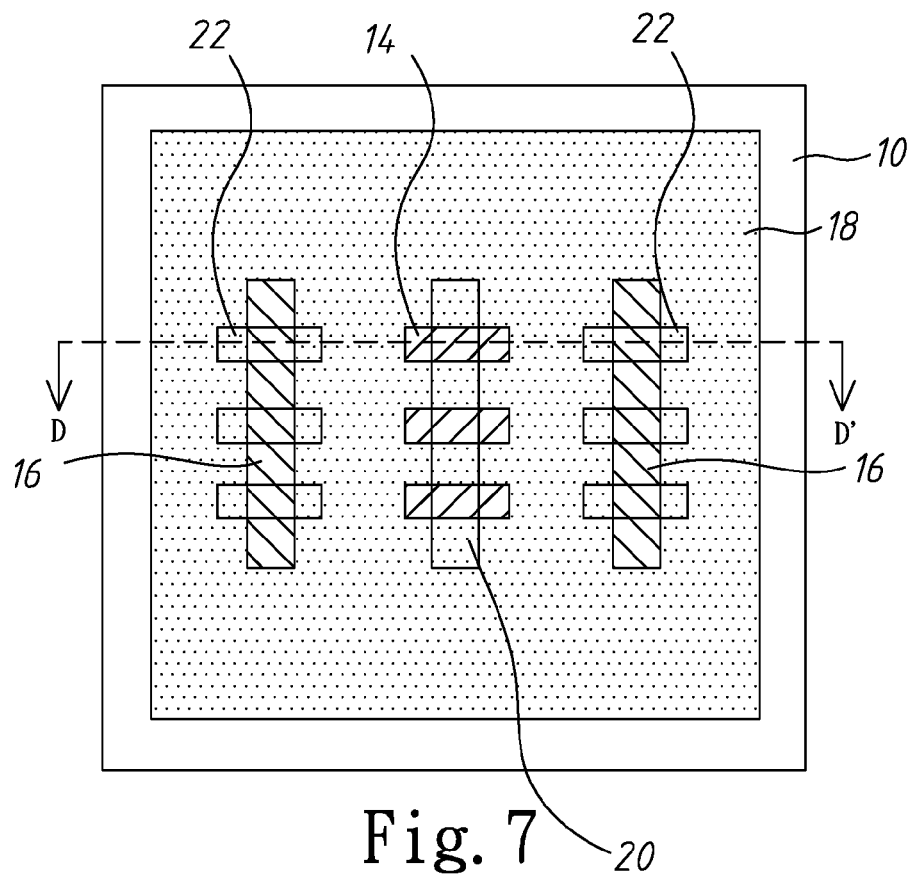


Fig. 7

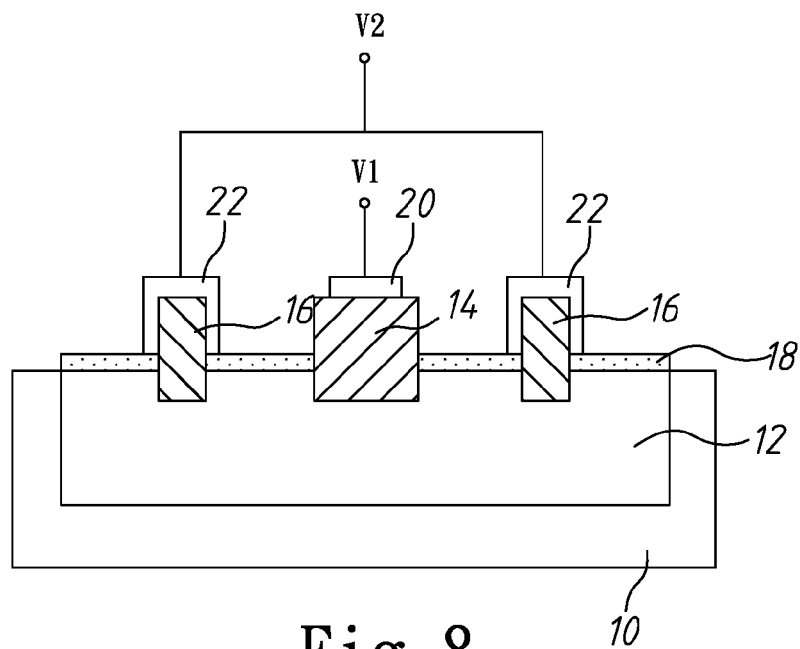


Fig. 8

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**SELF-BALANCED DIODE DEVICE****BACKGROUND OF THE INVENTION****Field of the Invention**

The present invention relates to a diode device, particularly to a self-balanced diode device.

**Description of the Related Art**

The semiconductor industry has experienced rapid growth due to continuous improvements in the integration density of a variety of electronic components (e.g., transistors, diodes, resistors, capacitors, etc.). For the most part, this improvement in integration density has come from repeated reductions in minimum feature size, which allows more components to be integrated into a given area. However, the smaller feature size may lead to more leakage current. As the demand for even smaller electronic devices has grown recently, there has grown a need for reducing leakage current of semiconductor devices.

As semiconductor technologies evolve, fin field effect transistors (FinFETs) have emerged as an effective alternative to further reduce leakage current in semiconductor devices. In a FinFET, an active region including the drain, the channel region and the source protrudes up from the surface of the semiconductor substrate upon which the FinFET is located. The active region of the FinFET, like a fin, may be rectangular in shape from a cross section view. In addition, the gate structure of the FinFET wraps the active region around three sides like an upside-down U. As a result, the gate structure's control of the channel has become stronger. The short channel leakage effect of conventional planar transistors has been reduced. As such, when the FinFET is turned off, the gate structure can better control the channel so as to reduce leakage current. Semiconductor devices including FinFETs are susceptible to extremely high voltage spikes such as an electrostatic discharge (ESD) transient. ESD is a rapid discharge that flows between two objects due to the built-up of static charge. ESD may destroy semiconductor devices because the rapid discharge can produce a relatively large current. For example, the US patent No. 20070045736 disclosed a semiconductor device including a gate electrode, a first transistor and a second transistor, wherein the first transistor and the second transistor respectively have a first active region and a second active region. The first active region is arranged in a direction perpendicular to the gate electrode. The second active region is arranged in a direction inclined relative to the gate electrode. The first active region and the second active region can improve the mobility of holes and electrons. However, there is no ESD protection element installed in the semiconductor device. The US patent is silent with ESD protection.

To overcome the abovementioned problems, the present invention provides a self-balanced diode device, so as to solve the afore-mentioned problems of the prior art.

**SUMMARY OF THE INVENTION**

A primary objective of the present invention is to provide a self-balanced diode device, which uses at least one first conductivity type heavily doped fin arranged in a line along a first direction and at least two second conductivity type heavily doped fins arranged in a line along a second direction intersecting the first direction to establish at least two

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diodes which discharge uniform electrostatic discharge (ESD) currents, so as to reduce the semiconductor failures due to ESD.

To achieve the abovementioned objectives, the present invention provides a self-balanced diode device, which comprises a substrate, a doped well, at least one first conductivity type heavily doped fin, at least two second conductivity type heavily doped fins and an insulation layer. The substrate is a semiconductor substrate. The doped well is a P-type doped well or an N-type doped well. The doped well is arranged in the substrate. The first conductivity type heavily doped fin is arranged in the doped well, arranged in a line along a first direction, and protruded up from a surface of the substrate. The second conductivity type heavily doped fins are arranged in the doped well, arranged in a line along a second direction intersecting the first direction, respectively arranged at two opposite sides of the first conductivity type heavily doped fin, and protruded up from the surface of the substrate. For example, the first direction is perpendicular to the second direction. Each second conductivity type heavily doped fin and the first conductivity type heavily doped fin are spaced at a fixed interval. The doped well, the first conductivity type heavily doped fin and the second conductivity type heavily doped fins form at least two diodes. The insulation layer is arranged on the surface of the substrate and arranged between the first conductivity type heavily doped fin and each second conductivity type heavily doped fin. The first conductivity type heavily doped fin is coupled to a first voltage terminal, and the second conductivity type heavily doped fins are coupled to a second voltage terminal, and voltages of the first voltage terminal and the second voltage terminal forward bias the diodes to generate at least two uniform electrostatic discharge (ESD) currents through the diodes. The first conductivity type heavily doped fin is an N-type heavily doped fin, and the second conductivity type heavily doped fins are P-type heavily doped fins, and the first voltage terminal and the second voltage terminal are respectively a low voltage terminal and a high voltage terminal. Alternatively, the first conductivity type heavily doped fin is a P-type heavily doped fin, and the second conductivity type heavily doped fins are N-type heavily doped fins, and the first voltage terminal and the second voltage terminal are respectively a high voltage terminal and a low voltage terminal.

In the first embodiment, there are a plurality of second conductivity type heavily doped fins, a plurality of diodes and a plurality of ESD currents, and the insulation layer is arranged between the neighboring second conductivity type heavily doped fins. A plurality of first contacts is arranged on sidewalls and a top of the first conductivity type heavily doped fin and the insulation layer, arranged in a line along the second direction, and coupled to the first voltage terminal. Two second contacts are respectively arranged on sidewalls and tops of the second conductivity type heavily doped fins at the two opposite sides of the first conductivity type heavily doped fin, arranged on the insulation layer, arranged in a line along the first direction, and coupled to the second voltage terminal. An amount of the first contacts is equal to an amount of the second conductivity type heavily doped fins at each side of the first conductivity type heavily doped fin.

Compared with the first embodiment, the second embodiment further comprises a first heavily doped clamping fin. The first heavily doped clamping fin and the second conductivity type heavily doped fin belong to an identical conductivity type. The first heavily doped clamping fin is arranged in the doped well, is arranged in a line along the

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second direction, separates from the first conductivity type heavily doped fin, and is protruded up from the surface of the substrate. The first conductivity type heavily doped fin has a first end and a second end, and the first heavily doped clamping fin neighbors the first end and two the second conductivity type heavily doped fins nearest to it, and the insulation layer is arranged between the first heavily doped clamping fin and the second conductivity type heavily doped fin neighboring thereto and arranged between the first conductivity type heavily doped fin and the first heavily doped clamping fin, and the second contacts are arranged on sidewalls and a top of the first heavily doped clamping fin.

Compared with the second embodiment, the third embodiment further comprises a second heavily doped clamping fin. The second heavily doped clamping fin and the second conductivity type heavily doped fin belong to an identical conductivity type. The second heavily doped clamping fin is arranged in the doped well, is arranged in a line along the second direction, separates from the first conductivity type heavily doped fin, and is protruded up from the surface of the substrate. The second heavily doped clamping fin neighbors the second end and two the second conductivity type heavily doped fins nearest to it, and the insulation layer is arranged between the second heavily doped clamping fin and the second conductivity type heavily doped fin neighboring thereto and arranged between the first conductivity type heavily doped fin and the second heavily doped clamping fin, and the second contacts are arranged on sidewalls and a top of the second heavily doped clamping fin.

In the fourth embodiment, there are a plurality of first conductivity type heavily doped fins, a plurality of diodes and a plurality of ESD currents, and the insulation layer is arranged between the neighboring first conductivity type heavily doped fins. A first contact is arranged on sidewalls and tops of the first conductivity type heavily doped fins and the insulation layer, arranged in a line along the second direction, and coupled to the first voltage terminal. A plurality of second contacts is uniformly arranged on sidewalls and tops of the second conductivity type heavily doped fins at the two opposite sides of the first conductivity type heavily doped fins, arranged on the insulation layer, arranged in a line along the first direction, and coupled to the second voltage terminal. An amount of the first conductivity type heavily doped fins is equal to an amount of the second contacts at each side of the first conductivity type heavily doped fin.

Below, the embodiments are described in detail in cooperation with the drawings to make easily understood the technical contents, characteristics and accomplishments of the present invention.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a layout schematically showing a self-balanced diode device according to the first embodiment of the present invention;

FIG. 2 is a sectional view taken along Line A-A' of FIG. 1;

FIG. 3 is a layout schematically showing a self-balanced diode device according to the second embodiment of the present invention;

FIG. 4 is a sectional view taken along Line B-B' of FIG. 3;

FIG. 5 is a layout schematically showing a self-balanced diode device according to the third embodiment of the present invention;

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FIG. 6 is a sectional view taken along Line C-C' of FIG. 5;

FIG. 7 is a layout schematically showing a self-balanced diode device according to the fourth embodiment of the present invention; and

FIG. 8 is a sectional view taken along Line D-D' of FIG. 7.

#### DETAILED DESCRIPTION OF THE INVENTION

The self-balanced diode device of the present invention is used as an electrostatic discharge (ESD) protection structure needed for integrated circuits. In ESD protection, an ESD circuit is formed near integrated circuit terminals such as input and output pads, and also for power supply terminals. ESD protection circuits may provide a current discharge path so as to reduce the semiconductor failures due to ESD.

Refer to FIG. 1 and FIG. 2. The first embodiment of the self-balanced diode device of the present invention is introduced as below. The first embodiment comprises a substrate 10, a doped well 12, at least one first conductivity type heavily doped fin 14, at least two second conductivity type heavily doped fins 16, an insulation layer 18, a plurality of first contacts 20 and two second contacts 22. The doped well 12, the first conductivity type heavily doped fin 14 and the second conductivity type heavily doped fins 16 can form at least two diodes to discharge at least two uniform ESD currents. In the first embodiment, an amount of the first conductivity type heavily doped fin 14 is one, and there are a plurality of second conductivity type heavily doped fins 16, a plurality of diodes and a plurality of ESD currents.

The substrate 10 is a semiconductor substrate. The doped well 12 is a P-type doped well or an N-type doped well. The doped well 12 is arranged in the substrate 10. The first conductivity type heavily doped fin 14 is arranged in the doped well 12, arranged in a line along a first direction, and protruded up from a surface of the substrate 10. The second conductivity type heavily doped fins 16 are arranged in the doped well 12, arranged in a line along a second direction intersecting the first direction, respectively arranged at two opposite sides of the first conductivity type heavily doped fin 14, and protruded up from the surface of the substrate 10. For example, the first direction is perpendicular to the second direction. Each second conductivity type heavily doped fin 16 and the first conductivity type heavily doped fin 14 are spaced at a fixed interval. The insulation layer 18 is arranged on the surface of the substrate 10, arranged between the first conductivity type heavily doped fin 14 and each second conductivity type heavily doped fin 16, and arranged between the neighboring second conductivity type heavily doped fins 16. The first contacts 20 are arranged on sidewalls and a top of the first conductivity type heavily doped fin 14 and the insulation layer 18, arranged in a line along the second direction, and coupled to a first voltage terminal V1. The first conductivity type heavily doped fin 14 is coupled to the first voltage terminal V1 through the first contacts 20. The second contacts 22 are respectively arranged on sidewalls and tops of the second conductivity type heavily doped fins 16 at the two opposite sides of the first conductivity type heavily doped fin 14, arranged on the insulation layer 18, arranged in a line along the first direction, and coupled to a second voltage terminal V2. The second conductivity type heavily doped fins 16 are coupled to the second voltage terminal V2 through the second contacts 22. An amount of the first contacts 20 is equal to an

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amount of the second conductivity type heavily doped fins 16 at each side of the first conductivity type heavily doped fin 14.

Voltages of the first voltage terminal and the second voltage terminal forward bias the diodes to generate the uniform ESD currents through the diodes, so as to reduce the semiconductor failures due to ESD. As a result, the first conductivity type heavily doped fin 14 is an N-type heavily doped fin, and the second conductivity type heavily doped fins 16 are P-type heavily doped fins, and the first voltage terminal V1 and the second voltage terminal V2 are respectively a low voltage terminal and a high voltage terminal. Alternatively, the first conductivity type heavily doped fin 14 is a P-type heavily doped fin, and the second conductivity type heavily doped fins 16 are N-type heavily doped fins, and the first voltage terminal V1 and the second voltage terminal V2 are respectively a high voltage terminal and a low voltage terminal.

Refer to FIG. 3 and FIG. 4. The second embodiment of the self-balanced diode device of the present invention is introduced as below. Compared with the first embodiment, the second embodiment further comprises a first heavily doped clamping fin 24. The first heavily doped clamping fin 24 and the second conductivity type heavily doped fin 16 belong to an identical conductivity type. The first heavily doped clamping fin 24 is arranged in the doped well 12, is arranged in a line along the second direction, separates from the first conductivity type heavily doped fin 14, and is protruded up from the surface of the substrate 10. The first conductivity type heavily doped fin 14 has a first end and a second end, and the first heavily doped clamping fin 24 neighbors the first end and two the second conductivity type heavily doped fins 16 nearest to it, and the insulation layer 18 is arranged between the first heavily doped clamping fin 24 and the second conductivity type heavily doped fin 16 neighboring thereto and arranged between the first conductivity type heavily doped fin 14 and the first heavily doped clamping fin 24, and the second contacts 22 are arranged on sidewalls and a top of the first heavily doped clamping fin 24. The first heavily doped clamping fin 24 is coupled to the second voltage terminal V2 through the second contacts 22. In the second embodiment, the doped well 12, the first conductivity type heavily doped fin 14, the second conductivity type heavily doped fins 16 and the first heavily doped clamping fin 24 can form a plurality of diodes to discharge a plurality of uniform ESD currents, so as to reduce the semiconductor failures due to ESD.

Refer to FIG. 5 and FIG. 6. The third embodiment of the self-balanced diode device of the present invention is introduced as below. Compared with the second embodiment, the third embodiment further comprises a second heavily doped clamping fin 26. The second heavily doped clamping fin 26 and the second conductivity type heavily doped fin 16 belong to an identical conductivity type. The second heavily doped clamping fin 26 is arranged in the doped well 12, is arranged in a line along the second direction, separates from the first conductivity type heavily doped fin 14, and is protruded up from the surface of the substrate 10. The second heavily doped clamping fin 26 neighbors the second end and two the second conductivity type heavily doped fins 16 nearest to it, and the insulation layer 18 is arranged between the second heavily doped clamping fin 26 and the second conductivity type heavily doped fin 16 neighboring thereto and arranged between the first conductivity type heavily doped fin 14 and the second heavily doped clamping fin 26, and the second contacts 22 are arranged on sidewalls and a top of the second heavily doped clamping fin 26. The

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second heavily doped clamping fin 26 is coupled to the second voltage terminal V2 through the second contacts 22. In the third embodiment, the doped well 12, the first conductivity type heavily doped fin 14, the second conductivity type heavily doped fins 16, the first heavily doped clamping fin 24 and the second heavily doped clamping fin 26 can form a plurality of diodes to discharge a plurality of uniform ESD currents, so as to reduce the semiconductor failures due to ESD.

Refer to FIG. 7 and FIG. 8. The fourth embodiment of the self-balanced diode device of the present invention is introduced as below. The fourth embodiment comprises a substrate 10, a doped well 12, a plurality of first conductivity type heavily doped fins 14, two second conductivity type heavily doped fins 16, an insulation layer 18, a first contact 20 and a plurality of second contacts 22. The doped well 12, the first conductivity type heavily doped fins 14 and the second conductivity type heavily doped fins 16 can form a plurality of diodes to discharge a plurality of uniform ESD currents.

The substrate 10 is a semiconductor substrate. The doped well 12 is a P-type doped well or an N-type doped well. The doped well 12 is arranged in the substrate 10. The first conductivity type heavily doped fins 14 are arranged in the doped well 12, arranged in a line along a first direction, and protruded up from a surface of the substrate 10. The second conductivity type heavily doped fins 16 are arranged in the doped well 12, arranged in a line along a second direction intersecting the first direction, respectively arranged at two opposite sides of the first conductivity type heavily doped fins 14, and protruded up from the surface of the substrate 10. For example, the first direction is perpendicular to the second direction. Each second conductivity type heavily doped fin 16 and the first conductivity type heavily doped fin 14 are spaced at a fixed interval. The insulation layer 18 is arranged on the surface of the substrate 10, arranged between each first conductivity type heavily doped fin 14 and each second conductivity type heavily doped fin 16, and arranged between the neighboring first conductivity type heavily doped fins 14. The first contact 20 is arranged on sidewalls and tops of the first conductivity type heavily doped fins 14 and the insulation layer 18, arranged in a line along the second direction, and coupled to the first voltage terminal V1. The first conductivity type heavily doped fin 14 is coupled to the first voltage terminal V1 through the first contacts 20. The second contacts 22 are uniformly arranged on sidewalls and tops of the second conductivity type heavily doped fins 16 at the two opposite sides of the first conductivity type heavily doped fins 14, arranged on the insulation layer 18, arranged in a line along the first direction, and coupled to the second voltage terminal V2. The second conductivity type heavily doped fins 16 are coupled to the second voltage terminal V2 through the second contacts 22. An amount of the first conductivity type heavily doped fins 14 is equal to an amount of the second contacts 22 at each side of the first conductivity type heavily doped fin 14.

Voltages of the first voltage terminal and the second voltage terminal forward bias the diodes to generate the uniform ESD currents through the diodes, so as to reduce the semiconductor failures due to ESD. As a result, the first conductivity type heavily doped fin 14 is an N-type heavily doped fin, and the second conductivity type heavily doped fins 16 are P-type heavily doped fins, and the first voltage terminal V1 and the second voltage terminal V2 are respectively a low voltage terminal and a high voltage terminal. Alternatively, the first conductivity type heavily doped fin 14



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is a P-type heavily doped fin, and the second conductivity type heavily doped fins **16** are N-type heavily doped fins, and the first voltage terminal **V1** and the second voltage terminal **V2** are respectively a high voltage terminal and a low voltage terminal.

In conclusion, the present invention uses the first conductivity type heavily doped fin arranged in a line along a first direction and the second conductivity type heavily doped fins arranged in a line along a second direction intersecting the first direction to establish uniform ESD currents, so as to reduce the semiconductor failures due to ESD.

The embodiments described above are only to exemplify the present invention but not to limit the scope of the present invention. Therefore, any equivalent modification or variation according to the shapes, structures, features, or spirit disclosed by the present invention is to be also included within the scope of the present invention.

What is claimed is:

1. A self-balanced diode device comprising:

a substrate;

a doped well arranged in said substrate;

at least one first conductivity type heavily doped fin arranged in said doped well, arranged in a line along a first direction, and protruded up from a surface of said substrate; and

a plurality of second conductivity type heavily doped fins arranged in said doped well, arranged in a line along a second direction perpendicular to said first direction, arranged at two opposite sides of said first conductivity type heavily doped fin, and protruded up from said surface of said substrate, and each said second conductivity type heavily doped fin and said first conductivity type heavily doped fin are spaced at a fixed interval, and said doped well, said first conductivity type heavily doped fin and said second conductivity type heavily doped fins form a plurality of diodes;

an insulation layer arranged on said surface of said substrate, arranged between said first conductivity type heavily doped fin and each said second conductivity type heavily doped fin, and arranged between neighboring said second conductivity type heavily doped fins;

a plurality of first contacts arranged on sidewalls and a top of said first conductivity type heavily doped fin and said insulation layer, and arranged in a line along said second direction; and

two second contacts respectively arranged on sidewalls and tops of said second conductivity type heavily doped fins at said two opposite sides, arranged on said insulation layer, and arranged in a line along said first direction, and said first conductivity type heavily doped fin is coupled to a first voltage terminal through said first contacts, and said second conductivity type heavily doped fins are coupled to a second voltage terminal through said second contacts, and voltages of said first voltage terminal and said second voltage terminal forward bias said diodes to generate a plurality of uniform electrostatic discharge (ESD) currents through said diodes.

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2. The self-balanced diode device according to claim 1, wherein said doped well is a P-type doped well or an N-type doped well.

3. The self-balanced diode device according to claim 1, wherein when said first conductivity type heavily doped fin is an N-type heavily doped fin and said second conductivity type heavily doped fins are P-type heavily doped fins, said first voltage terminal and said second voltage terminal are respectively a low voltage terminal and a high voltage terminal; and when said first conductivity type heavily doped fin is a P-type heavily doped fin and said second conductivity type heavily doped fins are N-type heavily doped fins, said first voltage terminal and said second voltage terminal are respectively a high voltage terminal and a low voltage terminal.

4. The self-balanced diode device according to claim 1, wherein an amount of said first contacts is equal to an amount of said second conductivity type heavily doped fins at each said side of said first conductivity type heavily doped fin.

5. The self-balanced diode device according to claim 1, further comprising a first heavily doped clamping fin, and said first heavily doped clamping fin and said second conductivity type heavily doped fin belong to an identical conductivity type, and said first heavily doped clamping fin is arranged in said doped well, is arranged in a line along said second direction, separates from said first conductivity type heavily doped fin, and is protruded up from said surface of said substrate, and said first conductivity type heavily doped fin has a first end and a second end, and said first heavily doped clamping fin neighbors said first end and two said second conductivity type heavily doped fins nearest to it, and said insulation layer is arranged between said first heavily doped clamping fin and said second conductivity type heavily doped fin neighboring thereto and arranged between said first conductivity type heavily doped fin and said first heavily doped clamping fin, and said second contacts are arranged on sidewalls and a top of said first heavily doped clamping fin.

6. The self-balanced diode device according to claim 5, further comprising a second heavily doped clamping fin, and said second heavily doped clamping fin and said second conductivity type heavily doped fin belong to an identical conductivity type, and said second heavily doped clamping fin is arranged in said doped well, is arranged in a line along said second direction, separates from said first conductivity type heavily doped fin, and is protruded up from said surface of said substrate, and said second heavily doped clamping fin neighbors said second end and two said second conductivity type heavily doped fins nearest to it, and said insulation layer is arranged between said second heavily doped clamping fin and said second conductivity type heavily doped fin neighboring thereto and arranged between said first conductivity type heavily doped fin and said second heavily doped clamping fin, and said second contacts are arranged on sidewalls and a top of said second heavily doped clamping fin.

7. The self-balanced diode device according to claim 1, wherein said substrate is a semiconductor substrate.

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